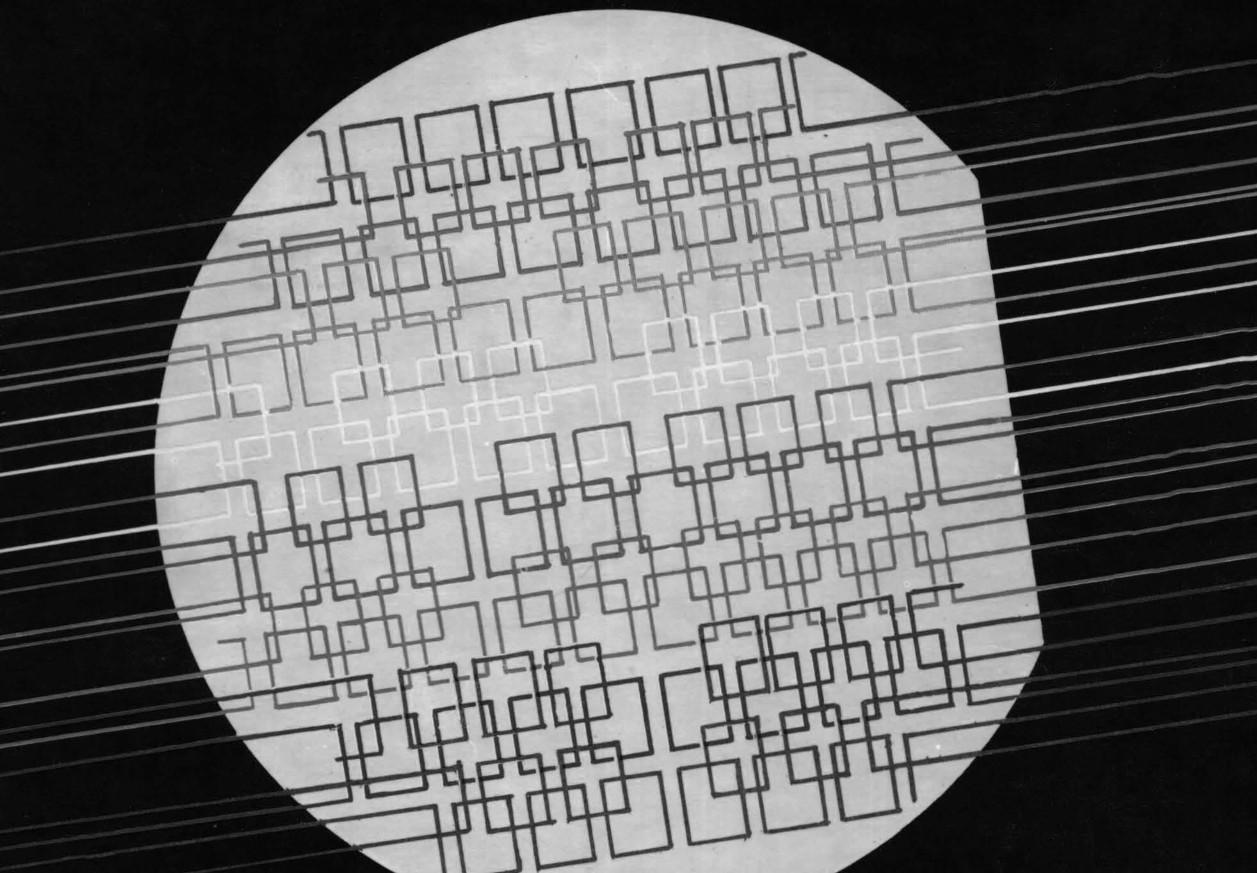
DATA BOOK



MICROELECTRONICA

microelectronica

DATA BOOK

MOS INTEGRATED CIRCUITS

SECOND EDITION - 1989

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MICROELECTRONICA PRODUCT INDEX

CMOS 4000 SERIES

1

SPECIAL CMOS

MEMORIES

NMOS ICs

PMOS ICs

MICROELECTRONICA 4000 SERIES INFORMATION

MICROELECTRONICA CMOS 4000 series meets the industry standardized specifications. The specifications for static parameters are primarily applicable to gates, inverters, high current (inverting) drivers and devices with Medium Scale Integration.
MICROELECTRONICA 4000 types have the following Absolute Maximum Ratings:

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

The Recommended Operating Conditions are specified as follows:

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

MMC 4000 SERIES FEATURES

The principal features of the MMC 4000 series are as follows:
- Operating range for G and H types 3—18 V; E and F types 3—15 V
- Rationalised range of quiescent leakage current (I_L) specifications coresponding to gate, buffer, and flip-flop, and Medium Scale Integration products.
- Maximum input leakage current (I_{IH}, I_{IL}) of $\pm 1\ \mu A$ at $V_{DD} = 18$ V for G and H types, 15 V for E and F types with $V_i = 0$ to 18 V for G and H types, 0 to 15 V for E and F types over the full temperature range.
- Input and output logic levels completely independent of temperature.
- Input voltage levels which define a very high DC noise immunity (45% V_{DD} typical).
- Noise margin of 1 V min at 5 V V_{DD}
  2 V min at 10 V V_{DD}
  2,5 V min at 15 V V_{DD}
- Low (400 ohm typical) and constant output impedance in both logical states givng fixed and equal output transition times.
- Output current capable of driving
  a) two low power TTL loads
  b) one low power Schottky TTL load
  c) two HLL loads
  over the rated temperaturerange.
- Output current and input threshold independent of the number of inputs paralleled together.
- Square transfer voltage characteristics.

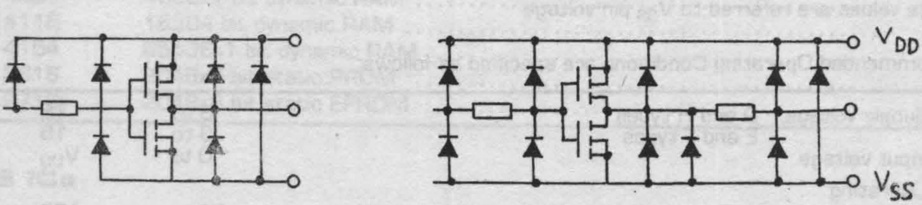
GENERAL CMOS CHARACTERISTICS

The main advantages offered by CMOS devices over corresponding bipolar devices (DTL, LPS, TTL, ECL, HLL) are:
- very low quiescent power dissipation (typically 10 nW/gate, 10 μW/MSI)
- wide operating voltage range (3 to 18 V for G and H devices; 3—15 V for E and F devices)
- high input impedance (typically 10^{12} ohms)
- high DC noise immunity (typically 45% of supply voltage).

This digital family however has slower switching speeds than most bipolar families. For exemple the typical propagation times for CMOS and other logic families are:

	CMOS	ECL	LPS	TTL	DTL	HLL
Prop. delay times(ns)	35	2	5	10	30	110

Moreover, due to the high input impedance of the MOS gate, C,OS devices require greater care in handling. Overvoltage protection networks are therefore used for the inputs of CMOS device. The level of protection for MMC 4000 products has been raised to 4 kV.
The following figure show the input protection network for a basic inverter.



In CMOS as in Linear Integrated Circuits a „latch-up" phenomenon may appear. This is caused by an electrical pulse which, acting on an SCR structure of parasitic bipolar transistoris inside CMOS devices, produces a low resistance path between supply voltage and ground that remains after the pulse has ceased leading rapidly to device destruction.
This phenomenon will occur either when V_{DD} is more then the maximum rating and approaches the breakdown voltage of the SCR structure or when the following conditions are verified:
a) the product of the two parasitic transistors is greater than or equal to unity;
b) the base-emitter junction of bith transistors is forward biased;
c) supply voltage and input circuits are able to deliver a current equal to the holding current of the SCR
In particular, condition (b) may be caused by:
1) voltages induced through the oxide by based metallization;
2) lateral voltage drops between substrate and P-well due to photo current generated by radiation. These drops can forward bias the gate-cathode junction of the parasitic SCR.

This effect is particularly significant in buffers wich are devices most subject to latch-up due to the combination of large geometry and low silicon resistivity.
For these reasons voltage transiensts or large output current surges occuring during operation near the maximum rating should be avoided.

MMC 4000 series dynamic switching parameters

The dynamic electrical characteristics are specified at $T_{amb} = 25°C$ under the following conditions:

— load capacitance (C_L) of 50 pF and load resistance (R_L) of 2000 kohm

— input pulse amplitude equal to supply voltage (V_{DD});

— input rise and fall time of 20 ns;

— propagation delay times measured from 50% the point of the input voltage to the 50% point of the output voltage;

— transition times measured from 10% to 90% of the supply voltage (V_{DD})

In some device other parameters are also specified:

a) Set up time

b) Hold time

c) Removal time

d) Tri-state disable delay times.

The figures below show the meaning of these parameters:

Fig.D

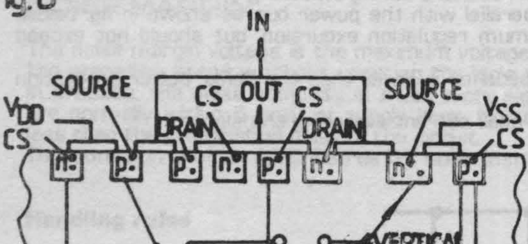
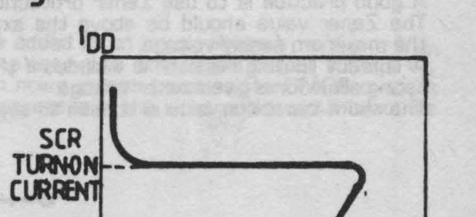
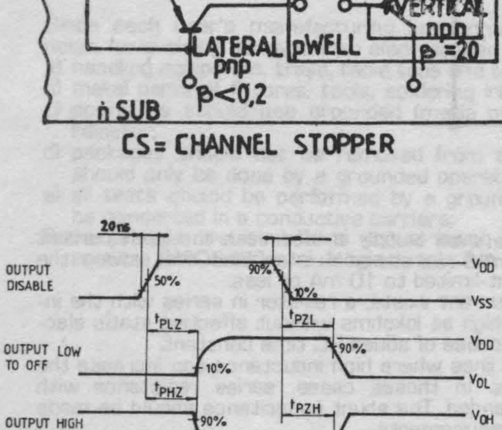
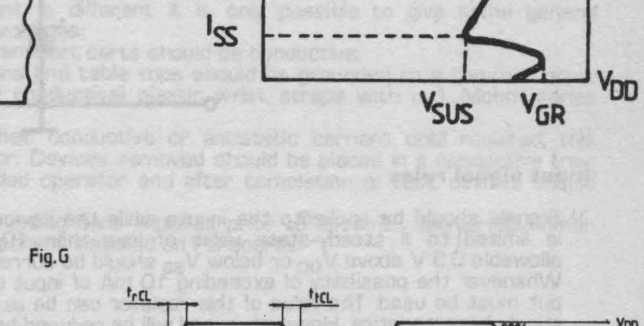


Fig.E





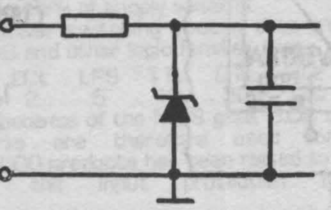


GENERAL OPERATING AND HANDLING INSTRUCTIONS

Power source rules

1) Refering to standard input network protection of fig., when separate power supplyies are used for V_{DD} and for the device inputs the V_{DD} supply should always be turned on before the input signal source and the input signal should be turned off before the V_{DD} supply is turned off.
This rule will prevent the D1 input protection diode from overdissi sipation and possible damage when the device power supply is grounded.
When the device power supply is an oppen circuit, violation of this rule can result in undesiredcircuit operation although device damage may not result; AC inputs can be rectified by D1 input diode to act as a power supply.
2) The steady power-supply operating voltage should be kept within the recommended operating conditions and always below the maximum ratings.
3) The power-supply polarity for CMOS circuits should not be reserved. The positive (V_{DD}) terminal should never be more than 0,5 V negative with respect to the negative (V_{SS}) terminal ($V_{DD} - V_{SS} > -0.5$ V)
Reversal of polaritie will forward-bias and short the structural and protection diode between V_{DD} and V_{SS}.
4) Power source current capability should be limited to the minimum value which will assure good logic oper ation.
5) Large value of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

A good practice is to use Zener protection diode in parallel with the power bus as shown in fig. below.
The Zener value should be above the expectec maximum regulation excursion, but should not exceed the maximum supply voltage.
A current limiting resistor is included if the supply impedance is lower than the Zener power dissipation rating allow for a given zener voltage.
The shunt capacitor value is chosen to supply required peak current switching transients.



Input signal rules

1) Signals should be appliedtp the inputs while the device power supply is off unless the input current is limited to a steady-state value of less than 10 mA. Input-signal interfaces that swing the allowable 0.5 V above V_{DD} or below V_{SS} should be current-limited to 10 mA or less.
Whenever the possibility of exceeding 10 mA of input current exists, a resistor in series with the input must be used. The value of this resistor can be as high as lokohms without affecting static electrical characteristics. However, speed will be reduced because of added RC time constant.
Particular attention should be giben to long input-signal lines where high inductance can increase the likelihood of large-signal pickup in noisy environments. In theses cases, series resistance with shunt capacitance at the IC input terminals is recommended. The shunt capacitance should be made as large as possible consistent with the system speed rewuirements.
2) All CMOS inputs should be terminated. When SMOS inputs are wired to adge card connectors with CMOS drive coming from another PC board, a shunt resistor should be connected to V_{DD}.
3) When CMOS circuits are driven by TTL logic a pull-up resistor should be connected from the CMOS input to 5 V.
4) Input signals should be maintained within the recommended input signal Swing range.
5) Input rise and fall times for clocked devices must not exceed 15 μs in order to avoid high consumption, false triggering, etc. With slower inputs a Schmitt trigger must be employed.

Output rules

1) The power dissipation in a CMOS package should not exceed the rated valuefor the ambient temperature specified. The actual dissipation should be calculated when (a) shorting outputs directly to V_{DD} or V_{SS}, (b) driving low-impedance loads, (c) directly driving the base of PNP or NPN bipolar transistor.

2) Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs on power supplies greater then 5 V can damage CMOS devices.
3) CMOS, like active pull-up TTL, cannot be connected in the „wire-or" configuration because an "on" PMOS and an "on" NMOS transistor could be directly shorted across the power-supply rails. For applications with wire OR cofigurations it is necessary to use devices with tri-state logic outputs.
4) Paralleling gates is recommended only when the gates are within the same IC package.
5) Outputs loads should return to a voltage within the supply-voltage range (V_{DD} to V_{SS}).
6) Large capacitive loads (greater than 5000 pF) on CMOS BUFFERS or high-current drivers act like short circuits and may over-dissipate output transistors.
7) Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.
8) Shorting of output to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 500 mW.
This is possible with supply voltage higher than 5 V.
For cases in which a short circuited load is driven directly (base of PNP or NPN bipolar transistor) the requirements for gate operation must be terminated by consulting the published data. Note that a individual output transistor dissipation must be limited to 100 mW.

Noise immunity and noise margin

DC NOISE IMMUNITY

The V_{IL} and V_{IH} characteristics define the maximum tolerable noise voltages at an input terminal when input signals are within 50 mV of supply lines

NOISE MARGIN

The noise margin voltage is the maximum voltage that can be added at an input voltage $V_I = V_{OL}$ or V_{OH} the preceding stage whithout upseting the logic or causing the output to exceed the output voltage V_O.
In practice, the noise immunity is much more significant than noise margin because the CMOS outputs are normally within 5 omV of supply lines. Noise immunity increases if the input pulse width becomes less than the propagation delay of the circuit.
This condition is often described as AC noise immunity.

Handling rules

Since each user's manufacturing environment is different it is only possible to give some general notes for avoiding damage from electrostatic voltages:
a) handling equipment, trays, table tops and transport carts should be conductive;
b) metal parts of fixtures, tools, soldering irons and table tops should be grounded to a common point;
c) operators should use grounded (metla or conductive) plastic wrist straps with a 1 Mohm series resistor;
d) packages should not be removed from their conductive or antistatic carriers until required; this should only be done by a grounded operator. Devices removed should be placed in a conductive tray;
e) all tests should be performed by a grounded operator and after completion of test, devices should be reinserted in a conductive carriers;
f) the printed circuits boards should have shorting bars installed prior to assembly (soldering). When possible CMOS IC's should be the last component installed on PC boards.

ORDERING NUMBERS CMOS 4000 SERIES

MMC 4XXX E — for dual in-line plastic package, intermediate temperature range
MMC 4XXX F — for dual in-line ceramic package, frit seal, intermediate temperature range
MMC 4XXX G — for dual in-line ceramic package, extended temperature range
MMC 4XXX H — for dual in-line ceramic package, frit seal, extended temperature range

NOR GATES: 4000 DUAL 3 INPUT PLUS INVERTER 4001 QUAD 2 INPUT 4002 DUAL 4 INPUT 4025 TRIPLE 3 INPUT

GENERAL DESCRIPTION

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.
The MMC 4000, MMC 4001, MMC 4002 and MMC 4025E/F/G/H
NOR gates provide the system designer with direct implementation of the NOR function.
The MMC 4000, MMC 4001, MMC 4002 and MMC 4025E/F/G/H types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages

FEATURES

- Propagation delay time = 60 ns (typ) at C_L = 50 pF V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current
- 5 V, 10 V and 15 V parametric ratings
- High noise immunity: 0.45 V_{DD} (typical)

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

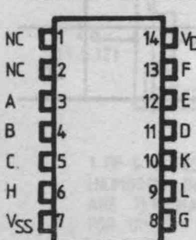
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

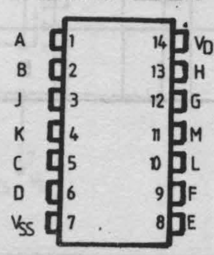
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

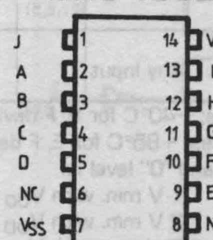
MMC 4000



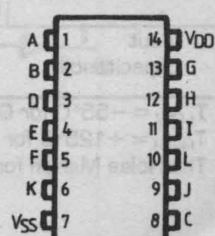
MMC 4001



MMC 4002



MMC 4025



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

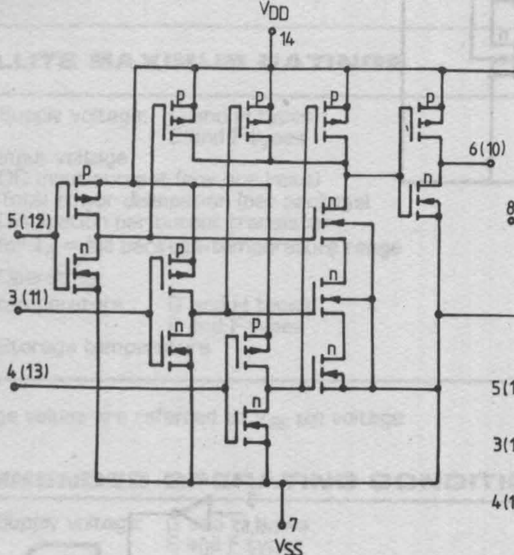
DYNAMIC ELECTRICAL CHARACTERISTICS

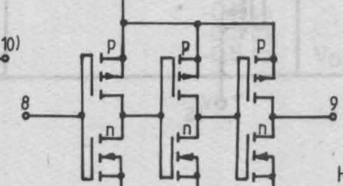
(T_A = 25°C, C_L = 50 pF, R_L = 200k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min	typ	max	
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		125 60 45	250 120 90	ns
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns

SCHEMATIC AND LOGIC DIAGRAMS

MMC 4000

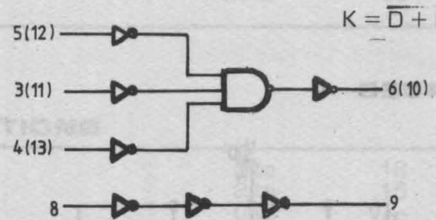




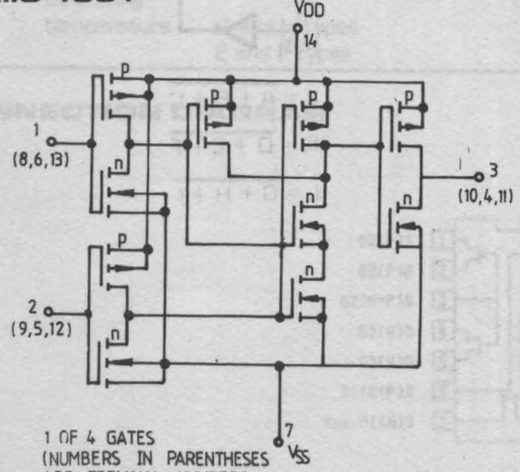
$H = \overline{A+B+C}$

$L = \overline{G}$

$K = \overline{D+E+F}$



MMC 4001



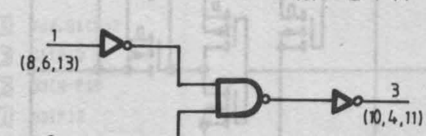
1 OF 4 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

$J = \overline{A+B}$

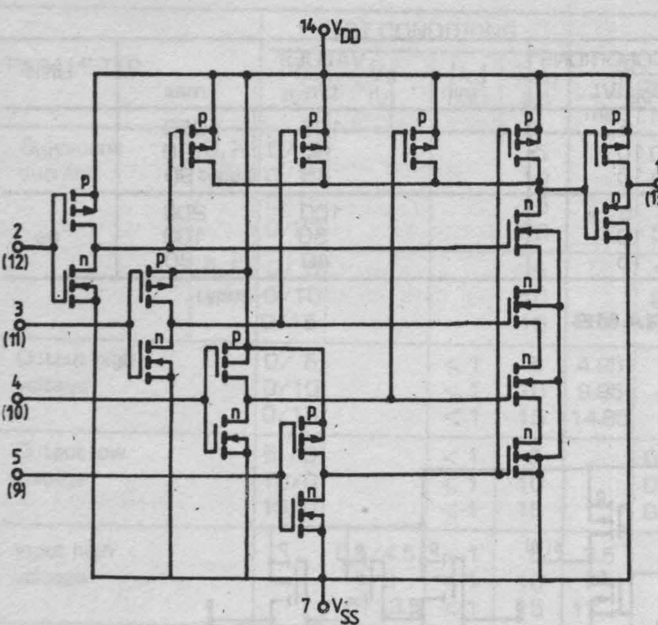
$K = \overline{C+D}$

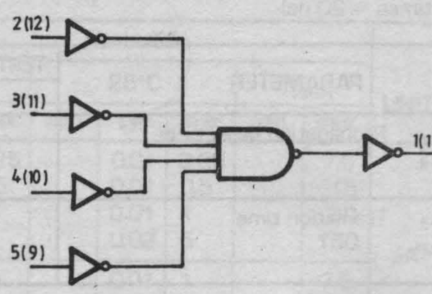
$L = \overline{E+F}$

$M = \overline{G+H}$



MMC 4002

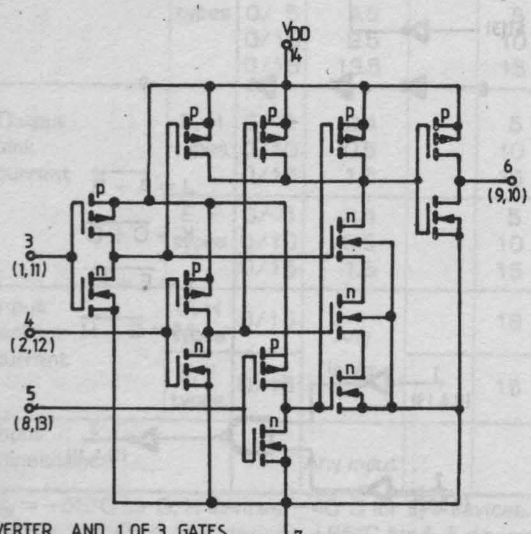




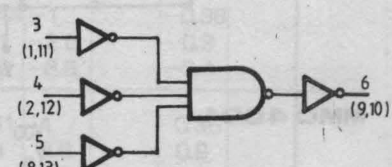
$J = \overline{A + B + c + D}$

$K = \overline{E + F + G + H}$

MMC 4025



INVERTER AND 1 OF 3 GATES
(NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR SECOND GATE)



$J = \overline{A + B + C}$

$K = \overline{D + E + F}$

$L = \overline{G + H + I}$

DUAL COMPLEMENTARY PAIR PLUS INVERTER

GENERAL DESCRIPTION

The MMC 4007 (G and H types) and MMC 4007 (E and F types) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package. The MMC 4007 types are comprised of three n-channel and three p-channel enchancement-type MOS transistors. The transistor elements are accessible through the package terminale to provide a convenient means for constructing the various typical circuits as shown in typical applications.
More complex functions are possible using multiple packages. Numbers shown in parantheses indicate terminals that are connected together to form the various configuration listed.

FEATURES

- Standardized symmetrical output characteristics
- Medium speed operation t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- Quiescent current specified to 20 V for G and H types
- Input current of 100 nA at 18 V and 25° C for G and H types
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

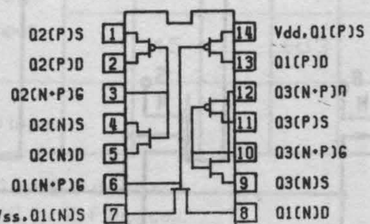
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

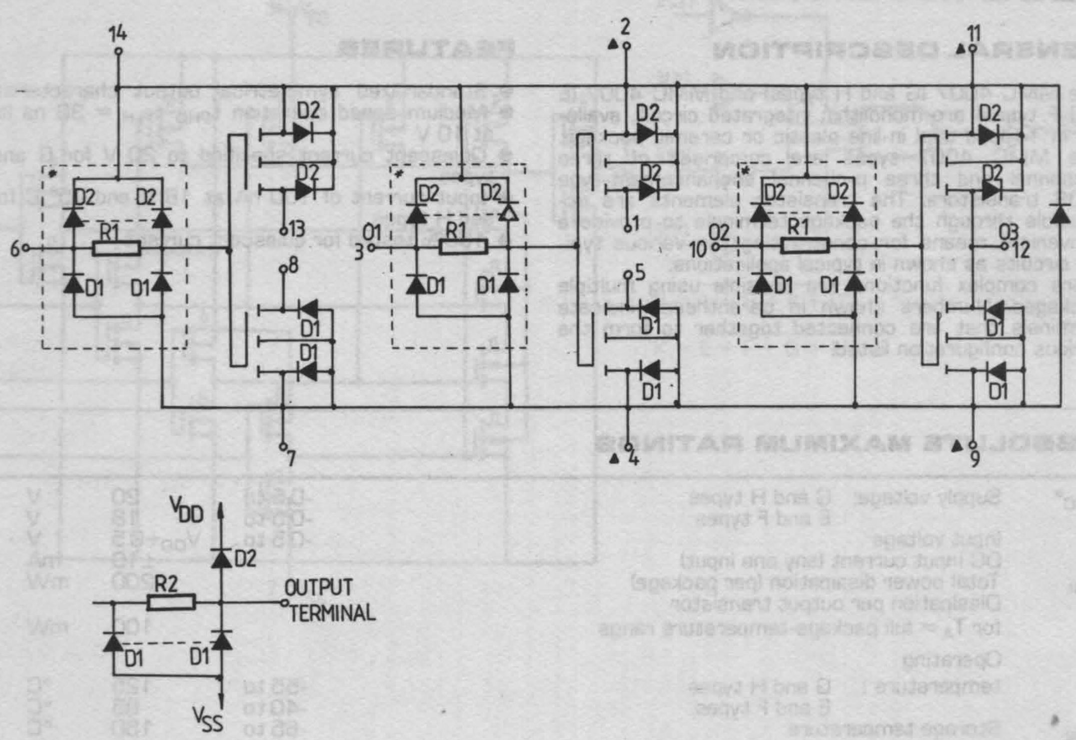
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

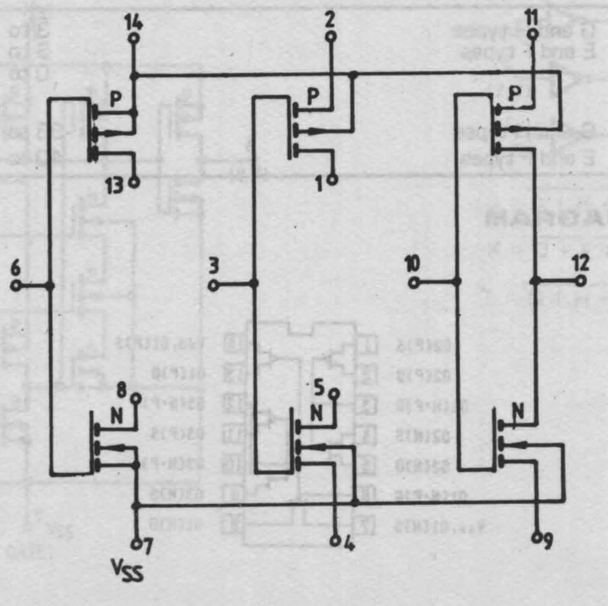
CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



FUNCTIONAL DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	—Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				1.5/13.5	< 1	15	12		12			12		
V_{IL}	—Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13.5/1.5	< 1	15		2.5			2.5		2.5	
I_{OH}	—Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

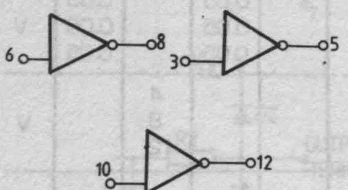
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_A = 25° C, C_L = 50 pF, R_L = 200 k, typical temperature coefficient for all V_{DD} values is 0.3/°C, all input rise and fall times = 20 ns)

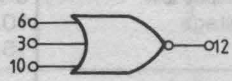
PARAMETER		TEST CONDITIONS		VALUES		Unit
			V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time		5		55	110	ns
			10		30	60	
			15		25	50	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	

TYPICAL APPLICATIONS (sample CMOS logic circuit arrangements using type 4007)

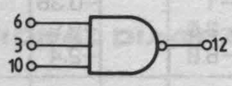
Triple inverters. (14,2,11); (8,13);



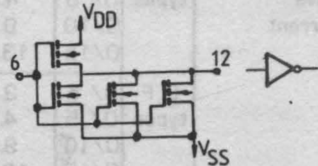
3—input NOR gate (13,2); (1,11); (12,5,8); (7,4,9);



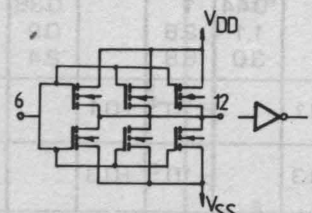
3—input NAND gate (1,12,13); (2,14,11), (4,8); (5,9);



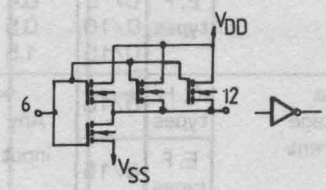
High sink-current driver. (6,3,10); (8,5,12); (11,14); (7,4,9);



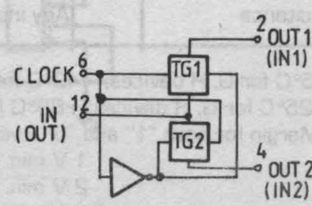
High sink-and source-curent driver. (6,3,10); (14,2,11); (7,4,9); (13,8,1,5,12)



High source-curent driver. (6,3,10); (13,1,12); (14,2,11); (7,9);



Dual bi-directional transmission gating. (1,5,12); (2,9); (11,4); (8,13,10); (6,3)



NAND GATES: 4011 QUAD 2 INPUT 4012 DUAL 4 INPUT 4023 TRIPLE 3 INPUT

GENERAL DESCRIPTION

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No. DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

The MMC 4011, MMC 4012 and MMC 4023E/F/G/H NAND gates provide the system designer with direct implementation of the NAND function. All inputs and outputs are buffered.

The MMC 4011, MMC 4012 and MMC 4023E/F/G/H types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages.

FEATURES

- Propagation delay time = 60 ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Buffered inputs and outputs
- 5 V, 10 V and 15 V parametric ratings
- 100% tested quiescent current
- High noise immunity 0.45 V_{DD} (typical)

APPLICATIONS

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltages are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

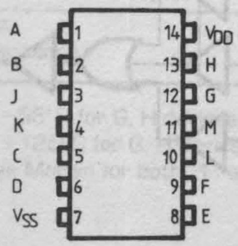
MMC 4011

$J = \overline{A \cdot B}$

$K = \overline{C \cdot D}$

$L = \overline{E \cdot F}$

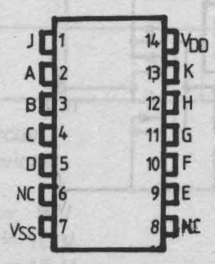
$M = \overline{G \cdot H}$



MMC 4012

$J = \overline{A \cdot B \cdot C \cdot D}$

$K = \overline{E \cdot F \cdot G \cdot H}$

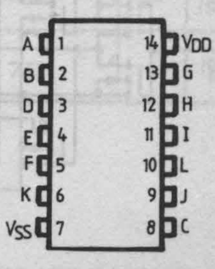


MMC 4023

$J = \overline{A \cdot B \cdot C}$

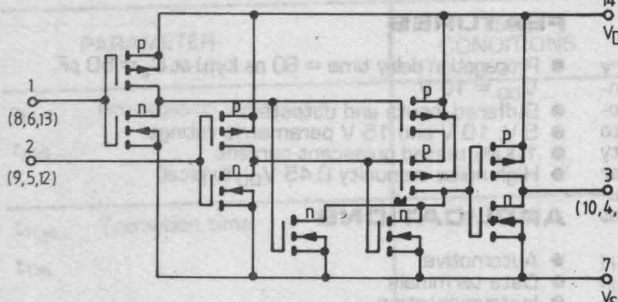
$K = \overline{D \cdot E \cdot F}$

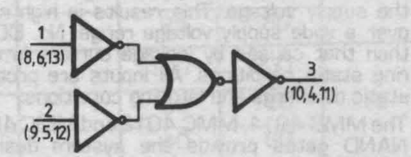
$L = \overline{G \cdot H \cdot I}$



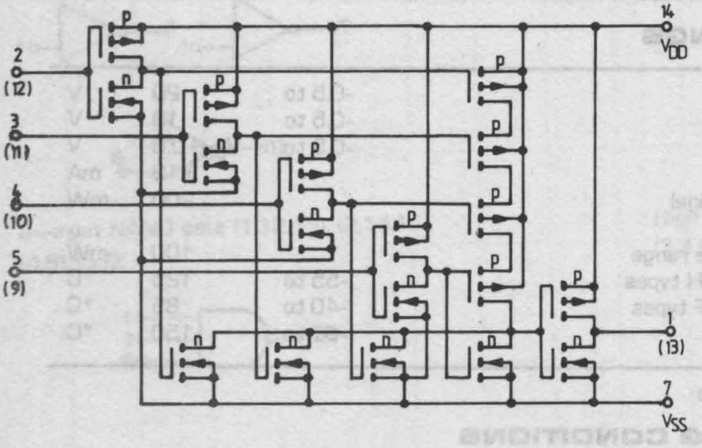
SCHEMATIC AND LOGIC DIAGRAMS

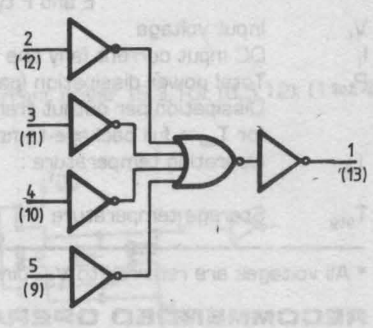
MMC 4011



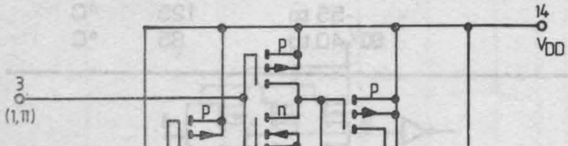


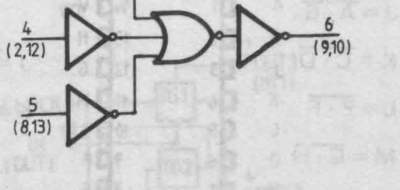
MMC 4012





MMC 4023





STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min	VALUES typ	VALUES max	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	5		125	250	ns
		10		60	120	
		15		45	90	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

DUAL "D" - TYPE FLIP-FLOP

GENERAL DESCRIPTION

The MMC 4013 is a monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.

The MMP 4013 consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

FEATURES

- set-reset capability
- static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- medium-speed operation — 16 MHz (typ.) clock toggle rate at 10 V
- quiescent current specified to 20 V
- maximum input leakage of 1 μA at 18 V (full package temperature range)
- standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

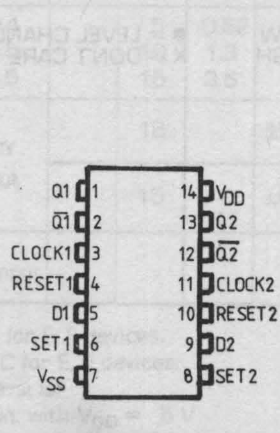
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

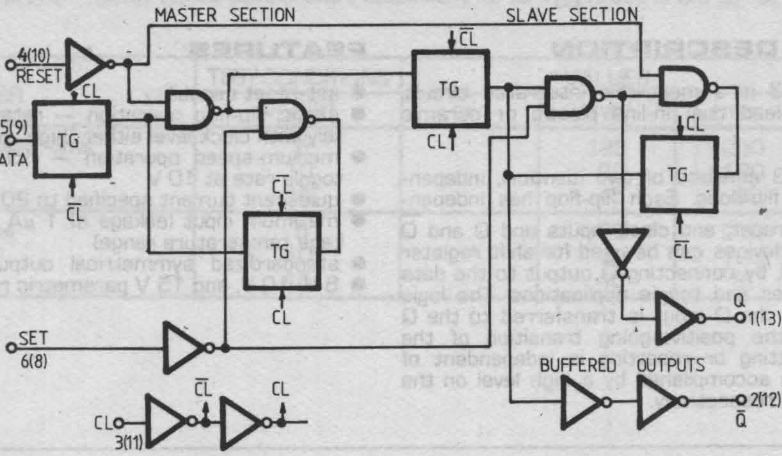
V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Imput voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM

(one of two identical flip-flops)



N(N) = FF1/FF2 TERMINAL ASSIGNEMENT

TRUTH TABLE

CL●	D	R	S	Q	$\overline{Q}$	
↑	0	0	0	0	1	
↑	1	0	0	1	0	
↓	X	0	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

LOGIC 0 = LOW
LOGIC 1 = HIGH

● = LEVEL CHANGE
X = DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T_{LOW}^* min.	T_{LOW}^* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}^* min.	T_{HIGH}^* max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q or $\bar{Q}$ outputs)	5 10 15		150 65 45	300 130 90	ns
t_{PLH},	Propagation delay time (Set to Q or Reset to $\bar{Q}$)	5 10 15		150 65 45	300 130 90	ns
t_{PHL},	Propagation delay time (Set to $\bar{Q}$ or Reset to Q)	5 10 15		200 85 60	400 170 120	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{CL}●	Maximum clock frequency	5 10 15	3.5 8 12	7 16 24		MHz
t_W	Clock pulse width	5 10 15	140 60 40	70 30 20		ns
t_r, t_f●●	Clock input rise or fall time	5 10 15			15 4 1	µs
t_W	Set or reset pulse width	5 10 15	180 80 50	90 40 25		ns
t_{setup}	Data setup time	5 10 15	40 20 15	20 10 7		ns

● Input t_r, t_f = 5 ns

●● If more than one unit is cascaded in a parallel clocked operation, tr should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

8-STAGE STATIC SHIFT REGISTERS: SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT: MMC 4014 ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT: MMC 4021

GENERAL DESCRIPTION

The MMC 4014, MMC 4021 series types are 8-stage parallel-or serial-input/serial-output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D type, master-slave flip-flop; in addition to an output from stage 8, "Q" outputs are also available from stage 6 and 7..

Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the MMC 4014. In the MMC 4021 serial entry is synchronous with the clock but parallel entry is asynchronous.

In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input.

When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line.

When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line.

In the MMC 4021, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made.

Register expansion using multiple package is permitted.

The MMC 4014, MMC 4021 series types are supplied in 16-lead dual-in-line plastic or ceramic package.

FEATURES

- Medium speed operation-12 MHz (typ.) clock rate at $V_{DD}—V_{SS} = 10$ V
- Fully static operation
- 8 Master-Slave flip-flops plus output buffering and control gating

ABSOLUTE MAXIMUM RATINGS

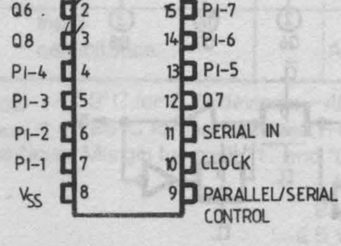
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



TRUTH TABLE

For 4014

CL	Serial input	Parallel/serial control	P I-1	P I-n	Q_1 (internal)	Q_n	
↑	X	1	0	0	0	0	
↑	X	1	1	0	1	0	
↑	X	1	0	1	0	1	
↑	X	1	1	1	1	1	
↑	0	0	X	X	0	Q_n-1	
↑	1	0	X	X	1	Q_n-1	
↓	X	X	X	X	Q_1	Q_n	NC

X = Don't care case NC = No change

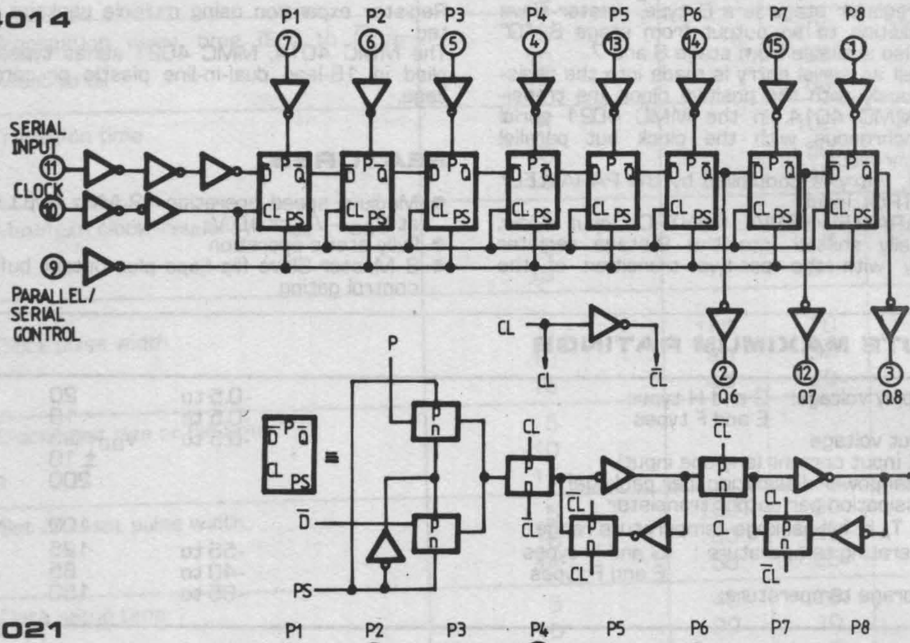
LOGIC DIAGRAMS AND TRUTH TABLE

For MMC 4021

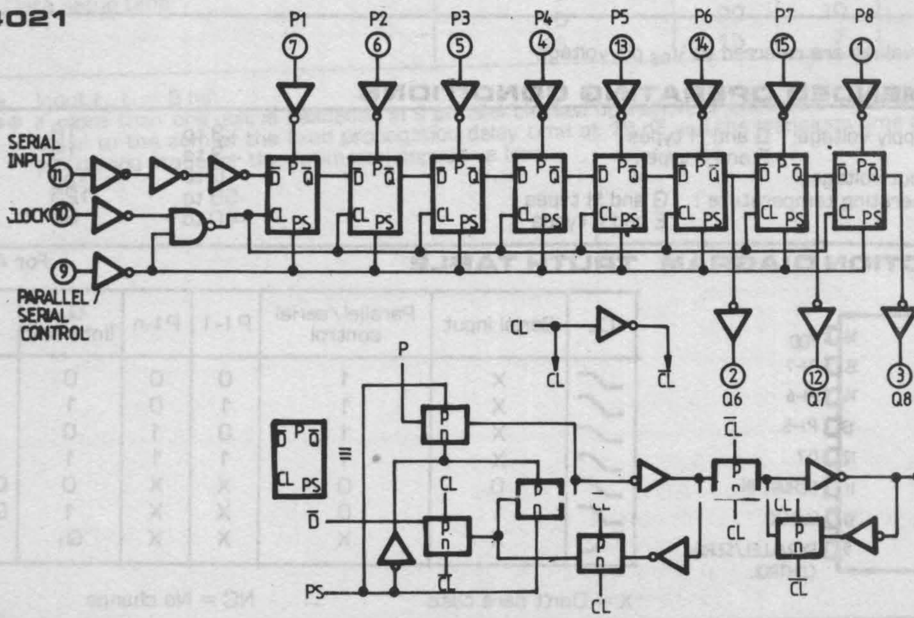
CL	Serial input	Parallel / serial control	P I-1	P I-n	Q_1 (internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
	0	0	X	X	0	Q_n-1	
	1	0	X	X	1	Q_n-1	
	X	0	X	X	Q_1	Q_n	NC

X = Don't care case NC = No change

MMC 4014



MMC 4021



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance		Any input							5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall times= 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		160 80 60	320 160 120	ns
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{CL}*	Maximum clock input frequency	5 10 15	3 6 8.5	6 12 17		MHz
t_W	Clock pulse width	5 10 15	180 80 50	90 40 25		ns
t_r, t_f	Clock input rise or fall time	5 10 15			15 15 15	μs
t_{setup}	Setup time, serial input (ref. to CL)	5 10 15	120 80 60	60 40 30		ns
t_{setup}	Setup time, paralel inputs (4014) (ref. to CL)	5 10 15	80 50 40	40 25 20		ns
t_{setup}	Setup time, parallel inputs (4021)	5 10 15	50 30 20	25 15 10		ns
t_{setup}	Setup time, parallel/serial control (4014) (ref. to CL)	5 10 15	180 80 60	90 40 30		ns
t_{hold}	Hold time, serial in, parallel in, parallel/serial control	5 10 15	0 0 0			ns
t_{WH}	P/S Pulse width (4021)	5 10 15	160 80 50	80 40 25		ns
t_{rem}	P/S Removal, time (4021) (ref. to CL)	5 10 15	280 140 100	140 70 50		ns

* If more then one unit is cascated t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT

GENERAL DESCRIPTION

The MMC 4015 (G and H types) and MMC 4015 (E and F types) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4015 consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA inputs is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one MMC 4015 package, or to more than 8 stages using additional MMC 4015's is possible.

FEATURES

- Medium speed operation: 12 MHz (typ.) clock rate at $V_{DD}-V_{SS} = 10$ V.
- Fully static operation.
- 8 master-slave flip-flops plus input and output buffering
- High noise immunity

ABSOLUTE MAXIMUM RATINGS

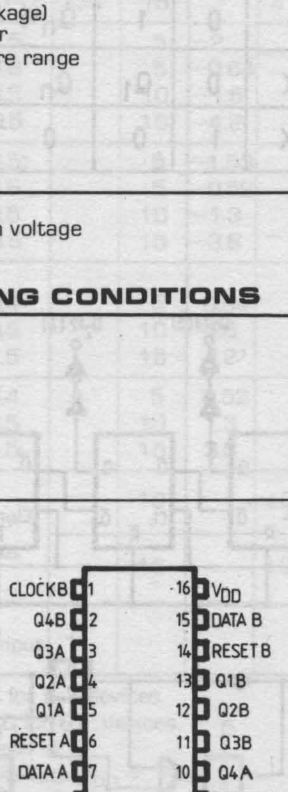
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

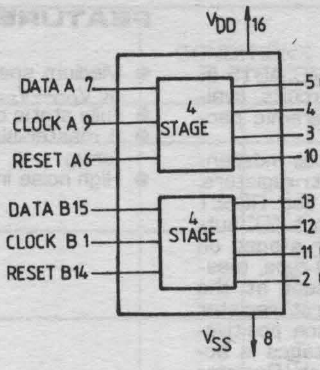
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



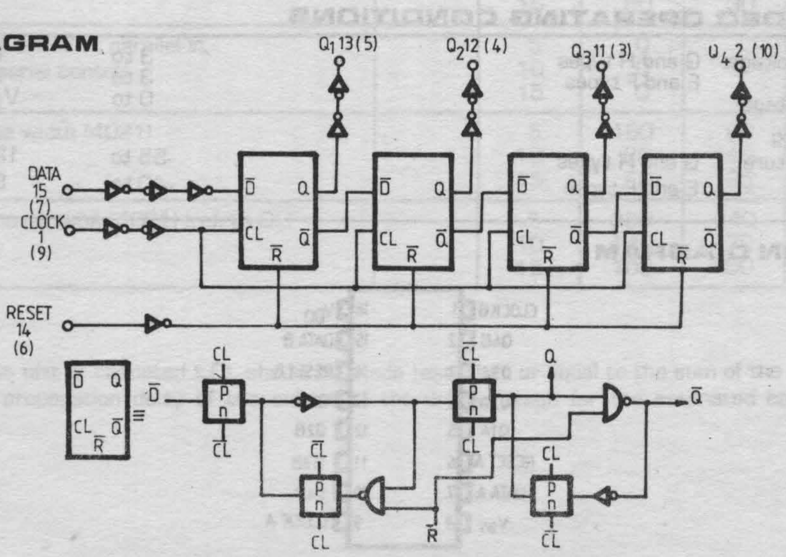
FUNCTIONAL DIAGRAM



TRUTH TABLE

CL	D	R	Q_1	Q_n	
	0	0	0	Q_n-1	
	1	0	1	Q_n-1	
	X	0	Q_1	Q_n	No change
X	X	1	0	0	

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times= 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decoded out Lines)	5 10 15		160 80 60	320 160 120	ns
t_{THL}, t_{TLH}	Transition time (Carry Out or Decoded Out Lines)	5 10 15		100 50 40	200 100 80	ns
f_{CL}	Maximum clock input frequency	5 10 15	3 6 8.5	6 12 17		MHz
t_W	Clock pulse width	5 10 15	180 80 50	90 40 25		ns
t_r, t_f*	Clock input rise or fall time	5 10 15			15 15 15	µs
t_{setup}	Data setup time	5 10 15	70 40 30	35 20 15		ns
Reset operation						
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		200 100 80	400 200 160	ns
t_W	Reset pulse width	5 10 15	200 80 60	100 40 30		ns

* If more than one unit is cascaded t_r CL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

QUAD BILATERAL SWITCH

GENERAL DESCRIPTION

The MMC 4016 (intermediate or extended temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.

The MMC 4016 types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

FEATURES

- 20 V digital or ± 10 V peak-to-peak switching
- 280 ohm typical ON resistance for 15 V operation
- Switch on resistance matched to within 10 ohm typ. over 15 V signal input range
- Extremely high control input impedance (control circuit isolated from signal circuit 10^{12} ohm typ.)
- Extremely low off switch leakage resulting in very low offset current and high effective off resistance: 110 pA typ. V_{DD}-V_{SS} = 18 V, T_A = 25°C
- Matched control-input to signal-output capacitance: reduces output signal transients.
- Frequency response switch on = 40 MHz (typ.).

ABSOLUTE MAXIMUM RATINGS

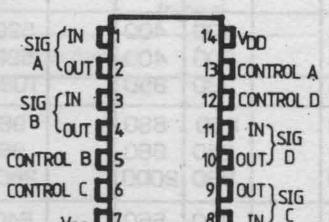
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

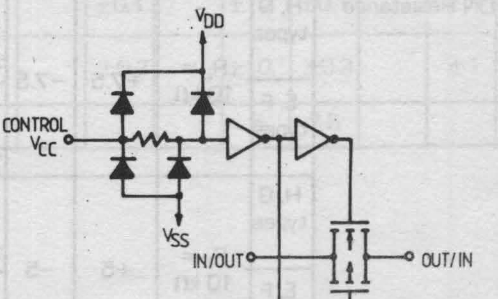
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



TYPICAL „ON“ RESISTANCE CHARACTERISTICS,

$T_A = 25°C$.

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			$R_L = 1\ k\Omega$		$R_L = 10\ k\Omega$		$R_L = 100\ k\Omega$	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)
R_{ON}	+15	0	200 200	+15 0	200 200	+15 0	180 200	+15 0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290 290	+10 0	250 250	+10 0	240 300	+10 0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860 600	+5 0	470 580	+5 0	450 800	+5 0
R_{ON} (max.)	+5	0	1.7 k	+4.2	7k	+2.9	33 k	+2.7
R_{ON}	+2.5	−2.5	590 720	+2.5 −2.5	450 520	+2.5 −2.5	490 520	+2.5 −2.5
R_{ON} (max.)	+2.5	−2.5	232 k	± 0.25	300 k	± 0.25	870 k	± 0.25

* Variation from a perfect switch, $R_{ON} = 0\ \Omega$

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES						UNIT
				$V_C = V_{DD}$	V_{SS} (V)	V_{DD} (V)	T_{LOW}		25°C			T_{HIGH}	
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent device current (all switches ON or all switches OFF)	G, H types				5 10 15 20		0.25 0.5 1 5		0.01 0.01 0.01 0.02	0.25 0.5 1 5		7.5 15 30 150	μA
		E, F types				5 10 15		1 2 4		0.01 0.01 0.01	1 2 4		7.5 15 30	

Switch

PARAMETER			$V_C = V_{DD}$	V_{SS} (V)	V_{IS}	T_{LOW} min.	T_{LOW} max.	25°C min.	25°C typ	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
R_{ON} ON Resistance	H, G types	$R_L = 10\ k\Omega$	+7.5	−7.5	+7.5 −7.5 ±0.25		360 360 775		200 200 280	400 400 850		600 600 1230	Ω
	E, F types				+7.5 −7.5 +0.25		370 370 790		200 200 280	400 400 850		520 520 1080	
	H, G types	$R_L = 10\ k\Omega$	+5	−5	+5 −5 ±0.25		600 600 1870		250 250 580	660 660 2000		960 960 2600	Ω
	E, F types				+5 −5 ±0.25		610 610 1900		250 250 580	660 660 2000		840 840 2380	

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS	$V_C = V_{DD}$	V_{SS} (V)	V_{DD} (V)	T_{LOW} min.	T_{LOW} max.	25°C min.	25°C typ	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
	G, H types	$R_L =$ 10 kΩ•	+15	0	+15		360		200	400		600	Ω
					+0.25		360		200	400		600	
					+9.3		775		300	850		1230	
	E, F types		+15	0	+15		370		200	400		520	
					+0.25		370		200	400		520	
					+9.3		790		300	800		1080	
	G, H types	$R_L =$ 10 kΩ•	+10	0	+10		600		250	660		960	Ω
					+0.25		600		250	660		960	
					+5.6		1870		560	2000		2600	
	E, F types		+10	0	+10		610		250	660		840	
					+0.25		610		250	660		840	
					+5.6		1900		560	2000		2380	
ΔR_{ON} Resistance (between any 2 of 4 switches)		$R_L =$ 10 kΩ•	+7.5	−7.5	±7.5				10				Ω
			+5	−5	±5				15				
Input or output leakage current switch OFF (effective OFF resistance)	G, H types		V_{DD} +18	$V_C = V_{SS}$ 0			±0.1		10^{-5}	±0.1		1	μA
	E, F types		V_{DD} +15	$V_C = V_{SS}$ 0			±0.3		10^{-5}	±0.3		1	
C_I Input capacitance		$V_{CC} = V_{SS} = -5$			+5				4				pF
C_O Output capacitance									4				
C_{IO} Feedthrough									0.2				
Control (V_C)													
V_{TH} Switch threshold voltage		$I_{IS} = 10\ \mu A$			5	1		1	2.25		1		V
					10	2		2	4.5		2		
					15	2		2	6.75		2		
I_I Input current	G, H types	$V_{IS} \leq V_{DD}$			18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
	E, F types				15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I Input capacitance									5	7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF all input square wave rise and fall time = 20 ns).

PARAMETER	V_C (V)	TEST CONDITIONS					VALUES			UNIT
		R_L (kΩ)	f_i (KHz.)	V_I (V)	V_{SS} (V)	V_{DD} (V)		typ.	max.	
Switch										
t_{pd} Propagation delay time (Signal input to output)	$= V_{DD}$	10		10 sq. Wave	GND	5 10 15		40 20 15	100 50 40	ns
Crosstalk between any 2 of 4 switches (f −50 dB) $20 \log \frac{V_O}{V_I} = -50$ dB	$V_{C(A)} = V_{DD} = +5$ $V_{C(B)} = V_{SS} = -5$	1		$V_{I(A)}$ (▲) =5pp				0.9		MHz
Frequency response switch "ON" (Sine wave input) at $20 \log \frac{V_O}{V_I} = -3$ dB	$= V_{DD}$ $= +5$	1		5p–p	−5			40		MHz
Feedthrough (Switch) OFF) at $20 \log \frac{V_O}{V_I} = -50$ dB	$= V_{SS}$ $= -5$	1		−5p-p		5		1.25		MHz
Sine wave distortion	$= V_{DD}$ $= 5$	10	1	5p–p	−5			0.4		%
Control (V_C)										
Propagation delay: (Turn ON control to output)	$V_{DD} - V_{SS}$ (Sq. wave)	1		V_{DD} or V_{SS}		5 10 15	$V_{DD} - V_{SS}$ = 10 V	35 20 15	70 40 30	ns
Max. allowable control input repetion rate	10 (Sq. wave)	1		V_{DD}	GND	10		10		MHz
Crosstalk (Control input to signal output)	10 (Sq. wave)	10			GND	10		50		mV

(▲) Symetrical about OV
(●) Fir all test conditions.

COUNTER/DIVIDERS: 4017` DECADE COUNTER WITH 10 DECODED OUTPUTS 4022 OCTAL COUNTER WITH 8 DECODED OUTPUTS

GENERAL DESCRIPTION

The MMC 4017 and MMC 4022 are 5-stage and 4 stage Johnson counters having 10 and 8 decoded outputs respectively.
The MMC 4017 and MMC 4022 are monolithic integrated circuits, fabricated in standard Al-gate CMOS technology. Are available in 16-lead dual in-line- plastic package.
Inputs include a CLOCK, a RESET and a CLOCK inhibit signal. Schmitt trigger in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high-speed operation. 2-input decimal-decode gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded Output remains high for one full clok cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the MMC 4017 or every 8 clock input cycles in the MMC 4022 and is used to ripple-clock the succeding device in a multi-device counting chain.

FEATURES

- Fully static operation
- Medium speed operation −12 MHz (typ) at V_{DD} = 10 V

APPLICATIONS

- Decade counter/decimal decode display
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide — by — N counting.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

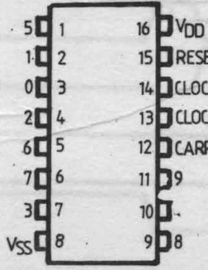
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

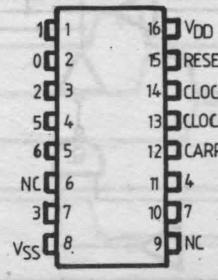
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

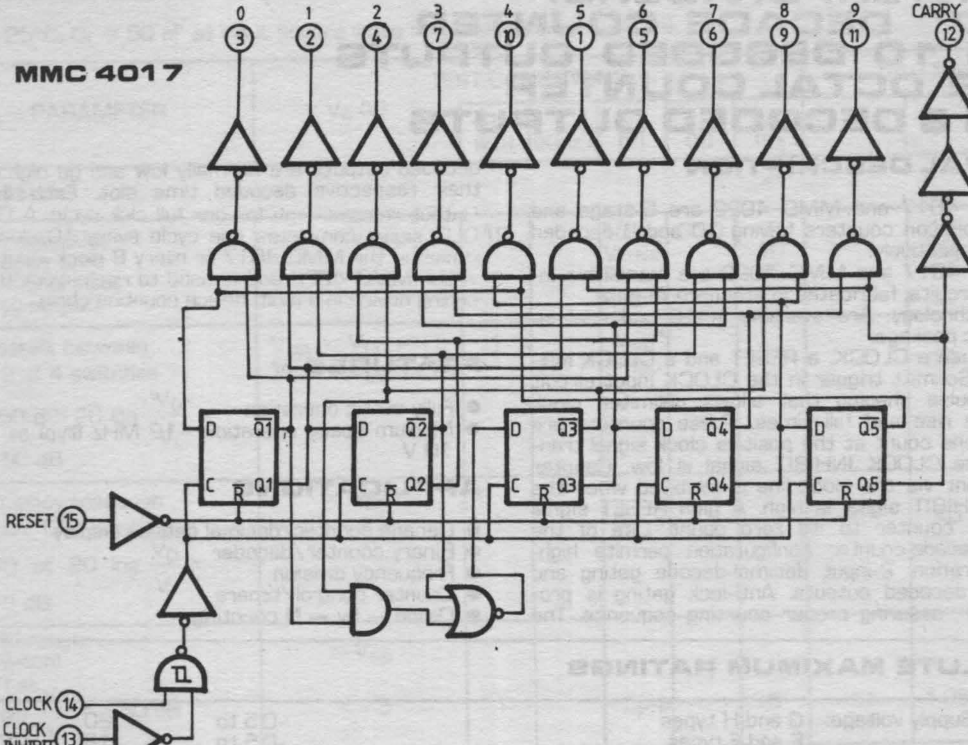
MMC 4017

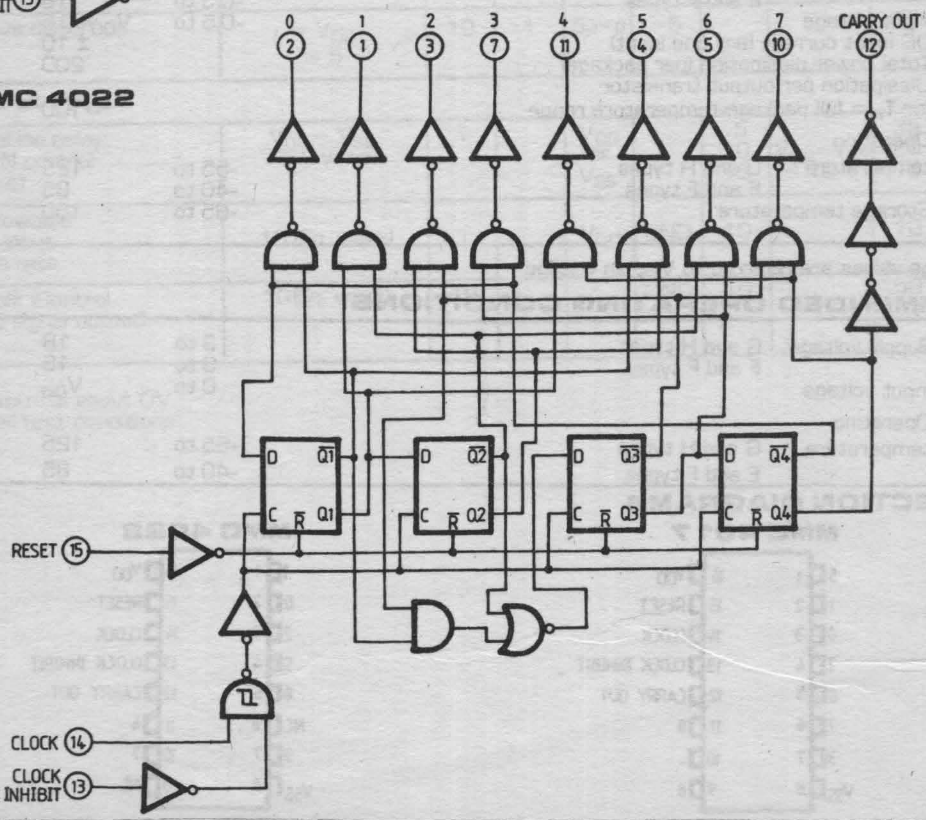


MMC 4022



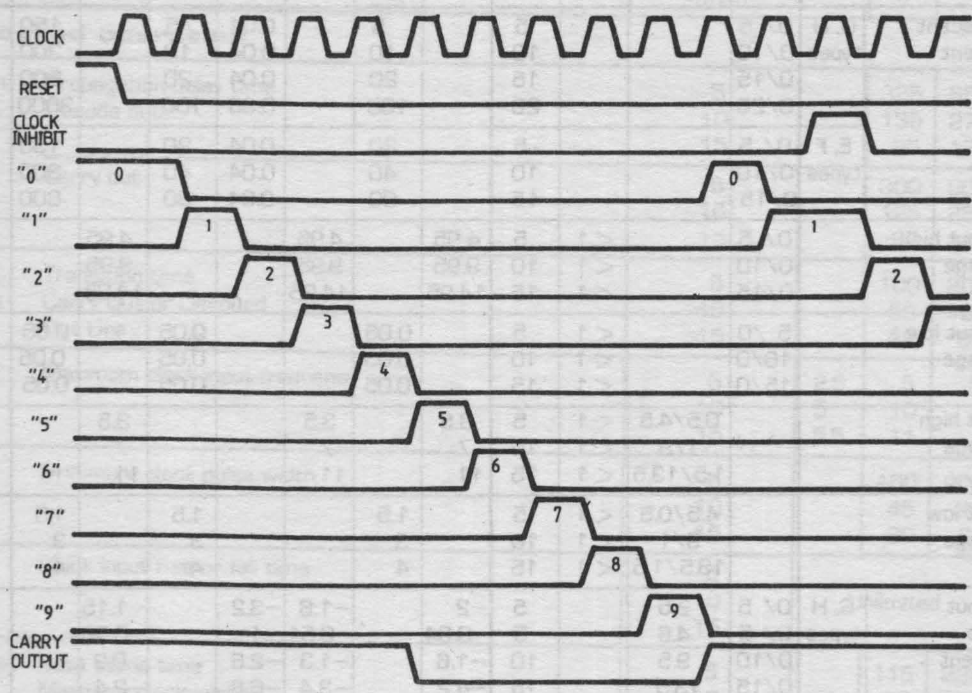
LOGIC DIAGRAM



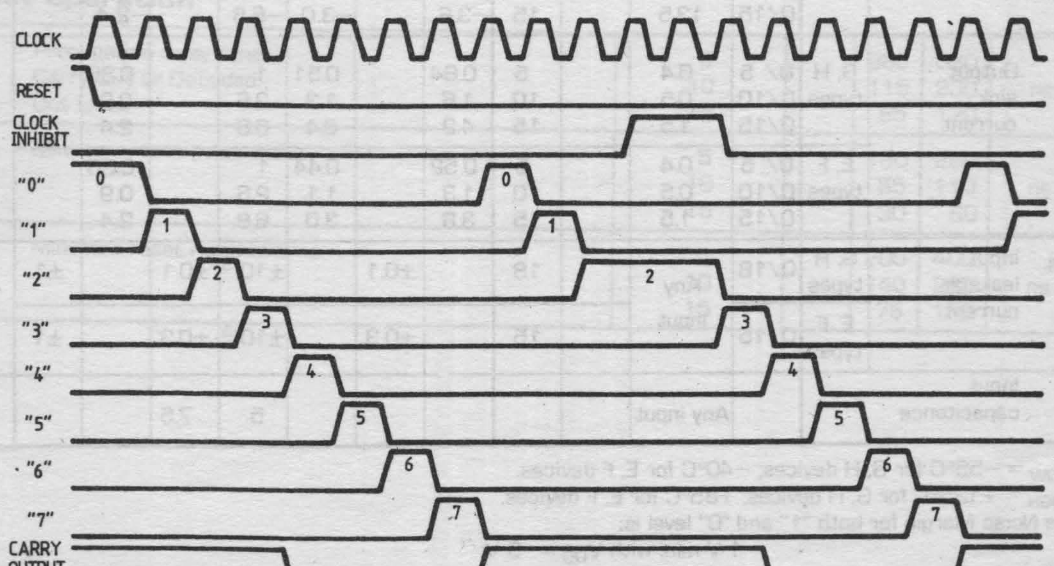


TIMING DIAGRAM

MMC 4017



MMC 4022



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T_{LOW}^*		25°C			T_{HIGH}^*		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		8.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

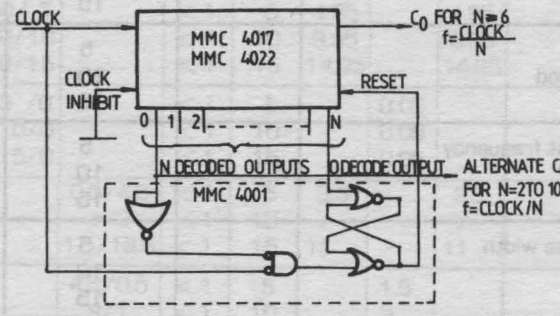
(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time Decode out	5		325	650	ns
		10		135	270	
		15		85	170	
	Carry out	5		300	600	ns
		10		125	250	
		15		80	160	
t_{THL}, t_{TLH}	Transition time Carry Out or Decoded Out Line	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	2.5	5	5	MHz
		10	5	10		
		15	5.5	11		
t_w	Minimum clock pulse width	5		100	200	ns
		10		45	90	
		15		30	60	
t_r t_f	Clock input rise or fall time	5				µs
		10		Unlimited		
		15				
t_{setup}	Data setup time Minimum clock inhibit	5		115	230	ns
		10		50	100	
		15		35	75	
Reset operation						
t_{PLH}, t_{PHL}	Propagation delay time Carry Out or Decoded Out Lines	5		265	530	ns
		10		115	230	
		15		85	170	
t_W	Minimum reset pulse width	5		130	260	ns
		10		55	110	
		15		30	60	
t_{rem}	Minimum reset removal time	5		200	400	ns
		10		140	280	
		15		75	150	

TYPICAL APPLICATIONS

Divide by N counter ($N \leqslant 10$) with N decoded outputs

When the N[th] decoded output is reached (N[th] clock pulse) the R—S flip-flop (constructed from two NOR gates of MMC 4001) generates a reset pulse which clears the MMC 4017 to its zero count. At this time, if the N[th] decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next MMC 4017 counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output high resets the R—S flip-flop to enable the MMC 4017. If the N[th] decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.



PRESSETTABLE DIVIDE-BY-N COUNTER

GENERAL DESCRIPTION

The MMC 4018 (G and H types) and MMC 4018 (E and F types) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage.

The MMC 4018 types consists of 5 Johnson-Counter stages, buffered $\bar{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q5}$, $\overline{Q4}$, $\overline{Q3}$, $\overline{Q2}$, $\overline{Q1}$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a MMC 4011 gate package to properly gate the feedback connection to the DATA input. Divide-by-functions greater than 10 can be achieved by use of multiple MMC 4018 units. The counter is advanced one count at the positive clock-signal transition. Schmitt-Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

FEATURES

- Medium speed operation 10 MHz (typ.) at $V_{DD}-V_{SS} = 10$ V.
- Fully static operation.

ABSOLUTE MAXIMUM RATINGS

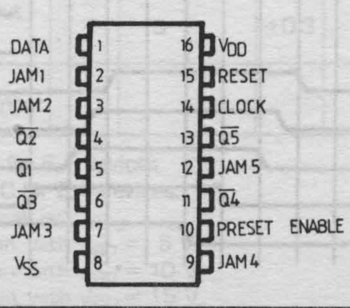
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

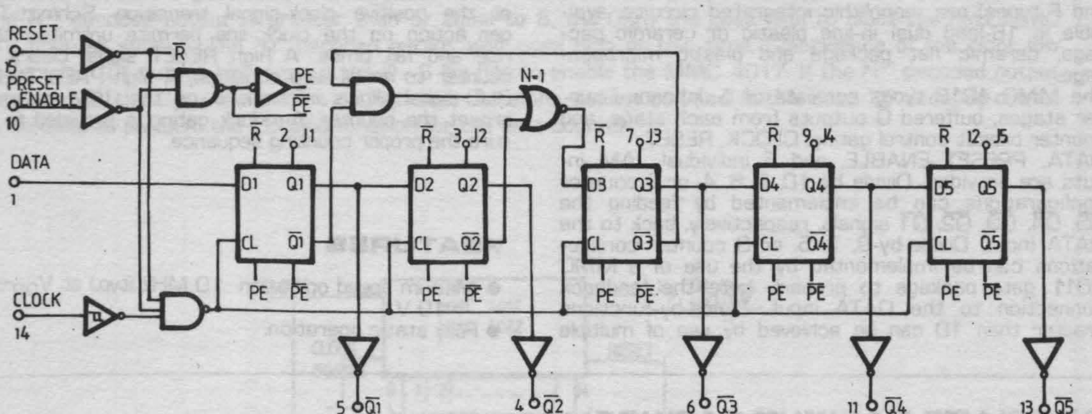
RECOMMENDED OPERATING CONDITIONS

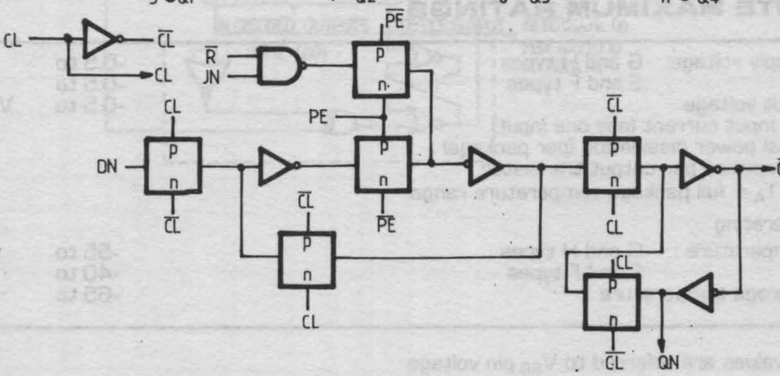
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	In put voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM

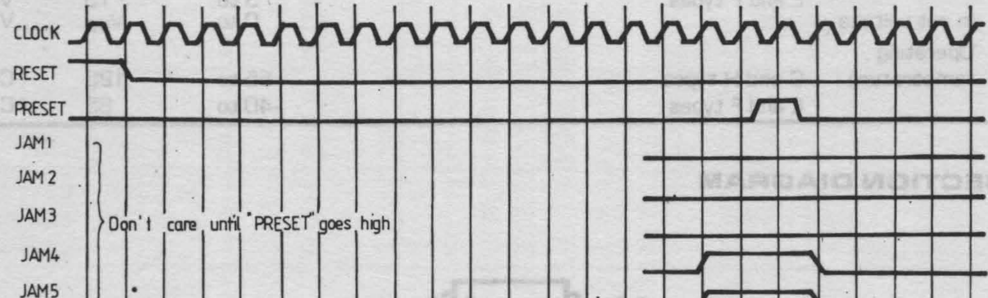




Detail for flip-flop

TIMING DIAGRAM

(Data input tied to $\overline{Q5}$ for decade counter configuration)



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage			0/ 5	<1	5	4.95		4.95			4.95		V
				0/10	<1	10	9.95		9.95			9.95		
				0/15	<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage			5 /0	<1	5		0.05			0.05		0.05	V
				10/0	<1	10		0.05			0.05		0.05	
				15/0	<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times= 20 ns).

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	5		200	400	ns
		10		90	180	
		15		65	130	
t_{THL}, t_{TLH}	Transition time	5		100	200	
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	3	6		MHz
		10	7	14		
		15	8.5	17		
t_W,	Clock pulse width	5	160	80		ns
		10	70	35		
		15	50	25		
t_r, t_f	Clock input rise or fall time	5	Unlimited			µs
		10				
		15				
t_{setup}	Data input Set-Up time	5	40	20		ns
		10	12	6		
		15	6	3		
t_H	Data input Hold-time	5	140	70		ns
		10	80	40		
		15	60	30		
Preset✲ or reset operation						
t_{PLH}, t_{PHL}	Propagation delay time (Preset or Reset to $\overline{Q}$)	5		275	550	ns
		10		125	250	
		15		90	180	
t_w	Preset or reset pulse width	5	160	80		ns
		10	70	35		
		15	50	25		
t_{rem}	Preset or reset removal time	5	80	40		ns
		10	30	15		
		15	20	10		

✲ At PRESET ENABLE OR JAM inputs.

QUAD AND/OR SELECT GATE

GENERAL DESCRIPTION

The MMC 4019 consists of four AND/OR select gate configurations, each consisting of two input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.
The MMC 4019 E/F/G/H types are supplied in 16-lead hermetic dual-in-line ceramic or plastic package.

FEATURES

- Medium-speed operation $t_{PHL} = t_{PLH} = 60$ ns (TYP.) at $V_{DD} = 10$ V, $C_L = 50$ pF
- 100% tested for quiescent current

APPLICATIONS

- AND-OR select gating
- Shift-right/shift/left registers
- True/complement selection
- And-OR/exclusive-OR selector

ABSOLUTE MAXIMUM RATINGS

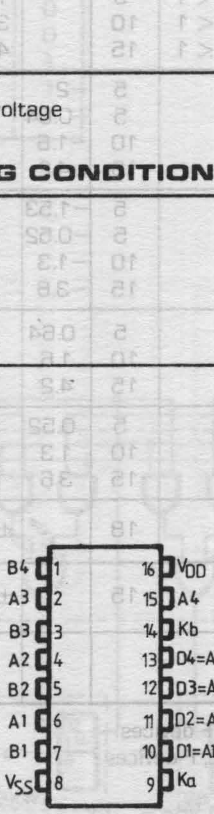
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	m
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	In put voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	.5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

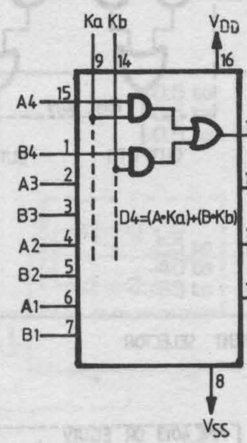
PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD}(V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		150 60 50	300 120 100	ns
t_{TLH}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns

TRUTH TABLE

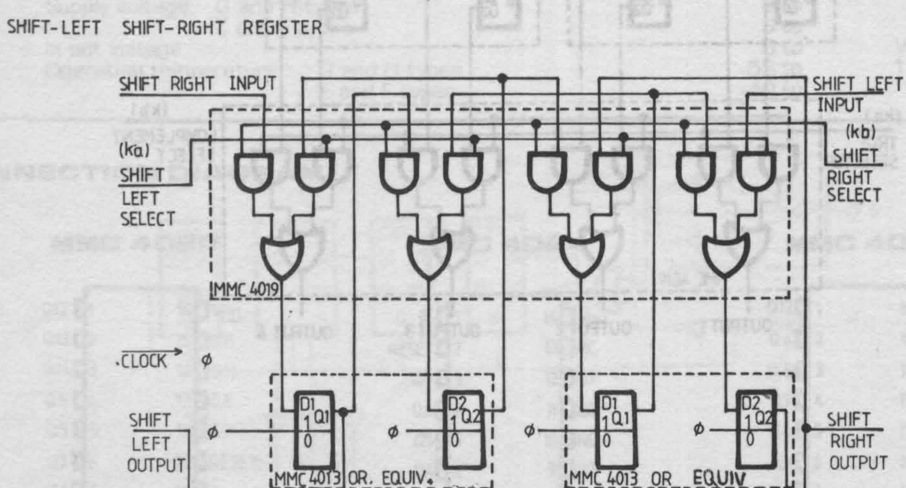
K_a	K_b	A_n	B_n	DN
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care

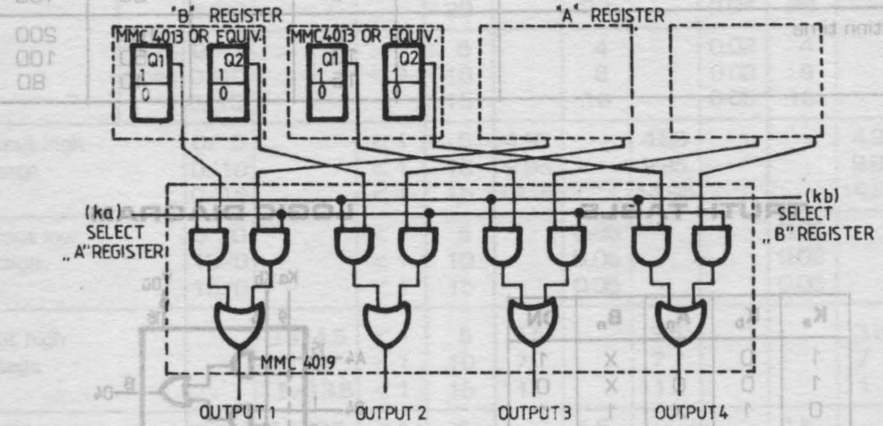
LOGIC DIAGRAM



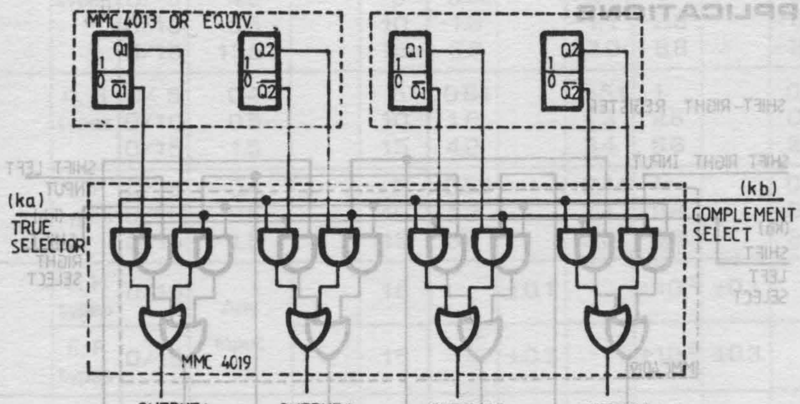
TYPICAL APPLICATIONS



AND-OR SELECTED GATING



TRUE COMPLEMENT SELECTOR



RIPPLE-CARRY BINARY COUNTER/DIVIDERS:

4020 - 14 STAGE
4024 - 7 STAGE
4040 - 12 STAGE

GENERAL DESCRIPTION

These devices are monolithic I.C's fabricated with standard AL-gate CMOS technology. All counter stages are master-slave flip-flops.

The state of a counter advances one count on the negative transition of each input pulse. A high level on the RESET line resets the counter to its all zeros stage. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered. MMC 4020, MMC 4040 are available in 16-lead dual-in-line ceramic or plastic package and MMC 4024 is available in 14-lead dual-in-line plastic or ceramic package.

FEATURES

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- Common RESET
- Quiescent current specified to 20 V
- Standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

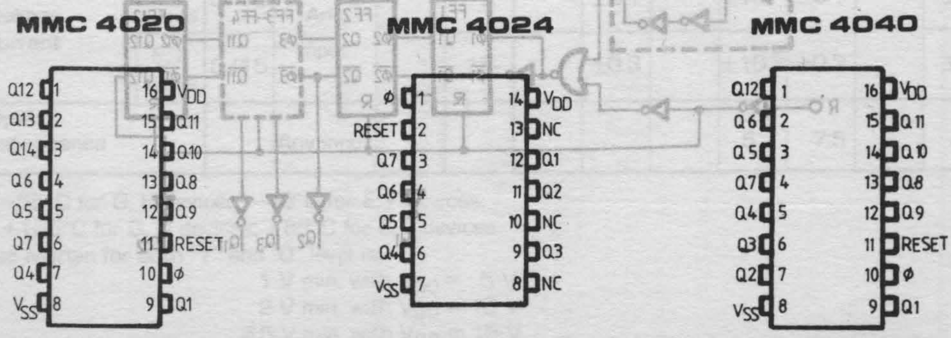
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

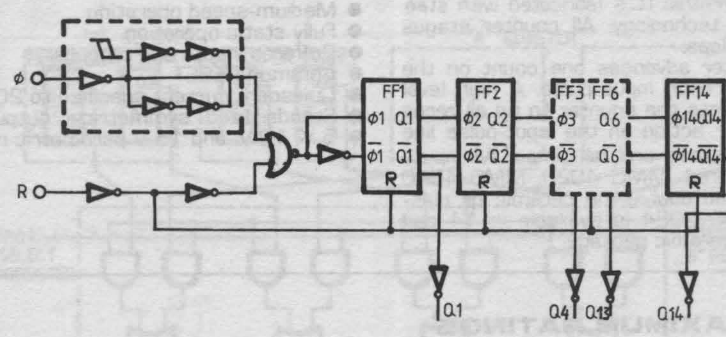
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	In put voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

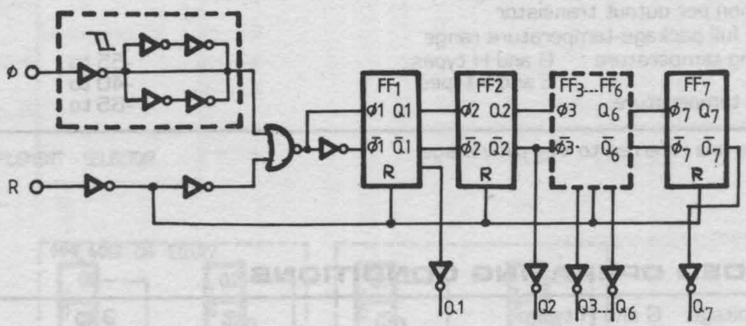


LOGIC DIAGRAM

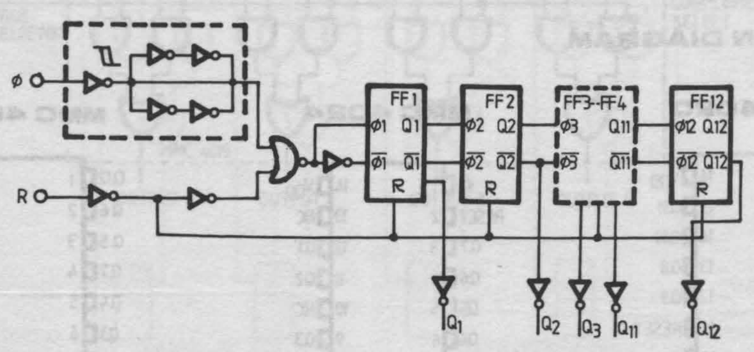
MMC 4020



MMC 4024



MMC 4040



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

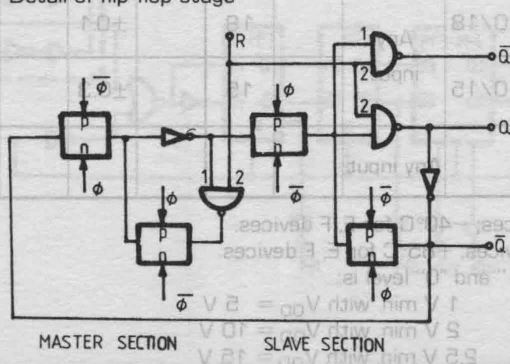
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Input pulse operation						
t_{PLH}, t_{PHL}	Propagation delay time (Φ to Q1 Out)	5 10 15		180 80 65	360 160 130	ns
t_{PLH}, t_{PHL}	Propagation delay time Qn to Qn+1	5 10 15		100 40 30	200 80 60	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
t_W	Minimum input pulse width	5 10 15		70 30 20	140 60 40	ns
t_r, t_f	Input rise and fall time	5 10 15		Unlimited		μs
f_{max}	Maximum input clock frequency	5 10 15	3.5 8 12	7 16 24		MHz
Reset operation						
t_{PHL}	Propagation delay time	5 10 15		140 60 50	280 120 100	ns
t_W	Minimum reset pulse width	5 10 15		100 40 30	200 80 60	ns
t_{rem}	Reset removal time	5 10 15		175 75 50	350 150 100	ns

Detail of flip-flop stage



DUAL J-K MASTER SLAVE FLIP-FLOP

GENERAL DESCRIPTION

The MMC 4027 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.

The MMC 4027 is a single monolithic chip integrated circuit containing two identical complementary-simmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset and Clock input signals. Buffered Q and Q signals are provided as outputs. This input-output arrangement provides for compatible operation with the MMC 4013 dual D-type flip-flop.
The MMC 4027 is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

FEATURES

- Set-Reset capability
- Static flip-flop operation-retains state indefinitely with clock level either „high" or „low"
- Medium speed operation-16 MHz (typ.) clock toggle rate at 10 V
- 100% tested for quiescent current

APPLICATIONS

- Registers, counters, control circuits

ABSOLUTE MAXIMUM RATINGS

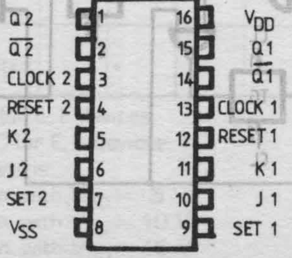
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

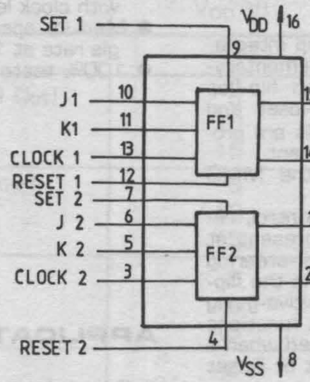
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

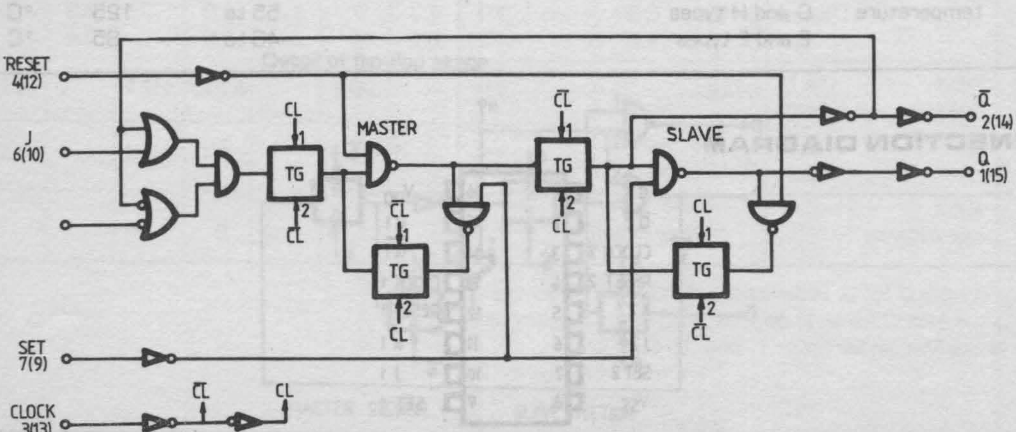


TRUTH TABLE

PRESENT STATE					CL ●	NEXT STATE OUTPUTS	
INPUTS				OUTPUT			
J	K	S	R	Q		Q	$\overline{Q}$
1	X	0	0	0		1	0
X	0	0	0	1		1	0
0	X	0	0	0		0	1
X	1	0	0	1		0	1
X	X	0	0	X		—NO CHANGE	
X	X	1	0	X	X	1	0
X	X	0	1	X	X	0	1
X	X	1	1	X	X	1	1

● Level change
x Don't care

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.

* $T_{HIGH} = +125$°C for G, H devices; $+85$°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	Clock to Q or $\overline{Q}$ outputs	5 10 15		150 65 45	300 130 190	ns
t_{PLH},	Propagation delay time	Set to Q or Reset to $\overline{Q}$	5 10 15		150 65 45	300 130 90	
t_{PHL}	Propagation delay time	Set to $\overline{Q}$ or Reset to Q	5 10 15		200 85 60	400 170 120	ns
t_{THL}, t_{TLH}	Transition time		5 10 15		100 50 40	200 100 80	ns
t_W	Pulse width	Clock	5 10 15	140 60 40	70 30 20		
t_W	Pulse width	Set or Reset	5 10 15	180 80 50	90 40 25		ns
t_r, t_f	Clock input rise or fall time		5 10 15			15 4 1	ns
t_{setup}	Setup time	Data	5 10 15	200 75 50	100 35 25		ns
f_{max}	Maximum clock input frequency*	Toggle mode	5 10 15	3.5 8 12	7 16 24		MHz

* Input t_r, t_f = 5 ns.

BCD-TO-DECIMAL DECODER

GENERAL DESCRIPTION

The MMC 4028 is a BCD-to-decimal or binary-to-octal decoder. This device is a monolithic IC fabricated in standard Al-gate CMOS technology. MMC 4028 is available in 16-lead dual in line ceramic and plastic package. The MMC 4028 consists of buffering on all four inputs decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of ten decimal decoded outputs. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

FEATURES

- High decoded output drive capability
- Medium speed operation
- „Positive logic" inputs and outputs (decoded outputs go high on selection)

ABSOLUTE MAXIMUM RATINGS

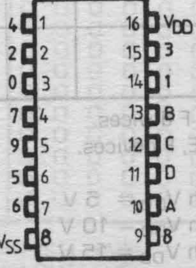
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

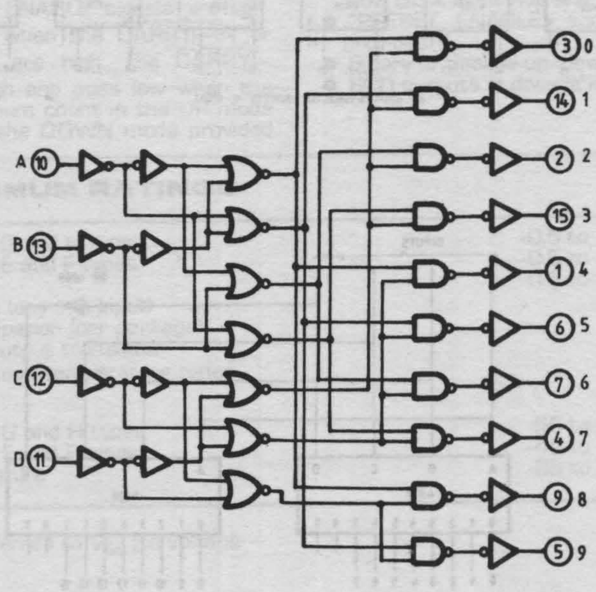
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 K, typical temperature coefficient for all V_{DD} values is 0.3 %/°C all input rise and fall times= 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			UM
			min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time (clock to out)	5		175	350	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

LOGIC DIAGRAM



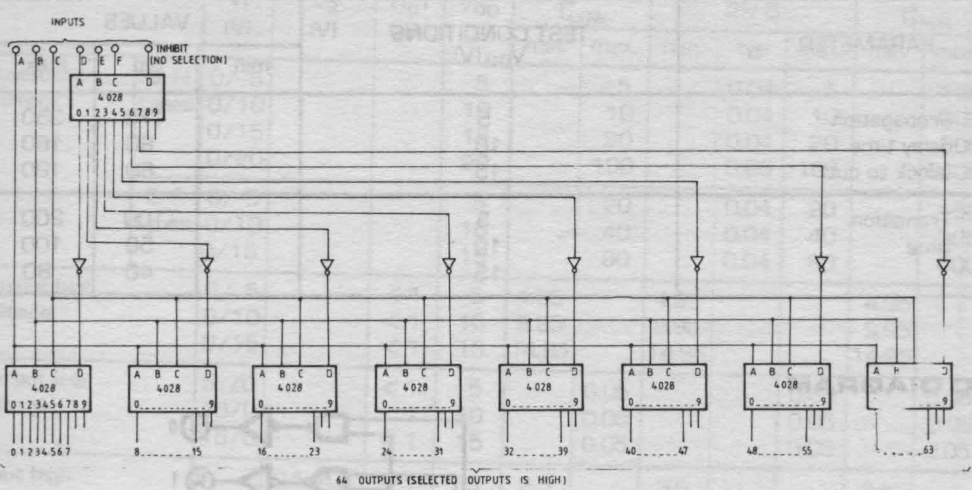
TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

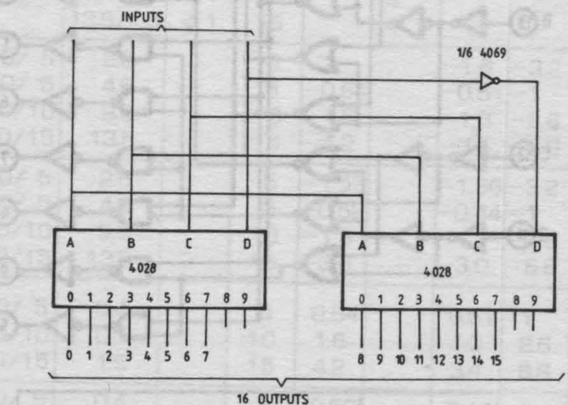
WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

TYPICAL APPLICATIONS

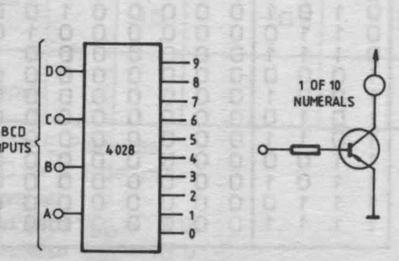
6 — bit binary to 1 of 64 address decoder



Code conversion circuit



Neon readout (Nixie Tube) display application



PRESETTABLE UP/DOWN COUNTER
BINARY OR BCD-DECADE

GENERAL DESCRIPTION

The MMC 4029 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4029 consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY—IN (CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET—ENABLE signal is high, resets the counter to it's zero count. The counter is advanced one count at the positive transition of the clock when the CARRY—IN or PRESET ENABLE signals are high. Advancement is inhibited when the CARRY—IN or PRESET ENABLE signals are high. The CARRY—OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY—IN signal is low. The CARRY—IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY—IN terminal must be conected to V_{SS} when not in use. Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low.
Multiple packages can be conected in either a parallel-clocking or a ripple-clocking arrangement as shown in cascading counter packages. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

FEATURES

- Medium speed operation—8 MHz (typ.) at C_L = 50 pF and V_{DD}—V_{SS} = 10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "PRESET ENABLE" and individual "JAM" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode

ABSOLUTE MAXIMUM RATINGS

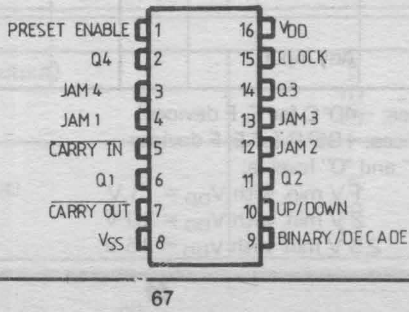
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.
* $T_{HIGH} = +125$°C for G, H devices; $+85$°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time (Q outputs)	5		250	500	ns
		10		120	240	
		15		90	180	
t_{PLH}, t_{PHL}	Propagation delay time (Carry Output)	5		280	560	ns
		10		130	260	
		15		95	190	
t_{TLH}, t_{THL}	Transition time (Q outputs, carry output)	5		100	200	ns
		10		50	100	
		15		40	80	
t_W,	Minimum clock pulse width	5		90	180	ns
		10		45	90	
		15		30	60	
t_r, t_f*	Clock rise and fall time	5			15	µs
		10			15	
		15			15	
t_{setup}**	Minimum setup time (Carry input)	5		30	60	ns
		10		10	20	
		15		6	12	
t_{setup}	Minimum setup time (B/D or U/D)	5		170	340	ns
		10		70	140	
		15		50	100	
f_{max}	Maximum clock input frequency	5	2	4		MHz
		10	4	8		
		15	5.5	11		
Preset enable						
t_{THL}, t_{TLH}	Propagation delay time (Q outputs)	5		235	470	ns
		10		100	200	
		15		80	160	
t_{PHL}, t_{PLH}	Propagation delay time (Carry Output)	5		320	640	ns
		10		145	290	
		15		105	210	
t_W,	Minimum Preset enable pulse width)	5		65	130	ns
		10		35	70	
		15		25	50	
t_{rem}**	Minimum preset enable (removal time)	5		100	200	ns
		10		55	110	
		15		40	80	
Carry input						
t_{PHL}, t_{PLH}	Propagation delay time (Carry output)	5		170	340	ns
		10		70	140	
		15		50	100	
t_{setup}***	Minimum setup time (Carry input)	5		25	50	ns
		10		15	30	
		15		12	25	

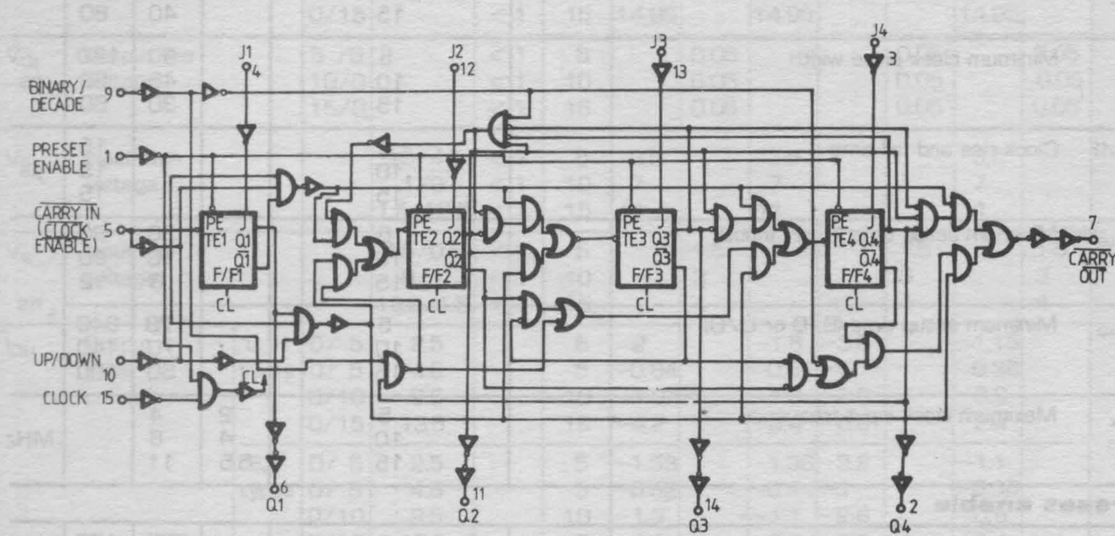
PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			UNIT
		min.	typ.	max.	
t_{hold}*** Minimum hold time (Carry input)	5 10 15		100 35 30	200 70 60	ns

* If more than one unit is cascaded in the parallel clocked application, t_r should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

** From Up/Down, Binary/Decade, Carry In preset Enable Control Inputs to Clock Edge.

*** From Carry In to Clock Edge.

LOGIC DIAGRAM



TRUTH TABLES

CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	0	0	0	1
⌐_ (negative edge)	0	1	X	$\overline{Q}$	Q
X	X	0	1	1	0
⌐_ (negative edge)	1	1	X	Q	$\overline{Q}$ NC
_⌐ (positive edge)	X	1	X	Q	$\overline{Q}$ NC

X = don't care

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
$\overline{\text{CARRY IN}}$ ($\overline{\text{CI}}$) (CLOCK ENABLE)	1 0	NO COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION

QUAD EXCLUSIVE-OR GATE

GENERAL DESCRIPTION

The MMC 4030 is a monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.
The MMC 4030 consists of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. All inputs and outputs are protected against electrostatic effects.

FEATURES

- MEDIUM-SPEED OPERATION-$t_{PHL} = t_{PLH} = 65$ ns (TYP.) AT $C_L = 50$ pF and $V_{DD}-V_{SS} = 10$ V
- LOW OUTPUT IMPEDANCE: 500 Ω (TYP.) AT $V_{DD}-V_{SS} = 10$ V

APPLICATIONS

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/substractors
- General logic functions

ABSOLUTE MAXIMUM RATINGS

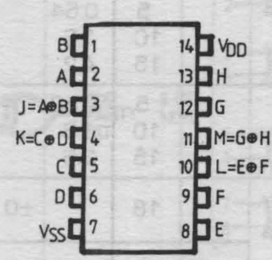
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

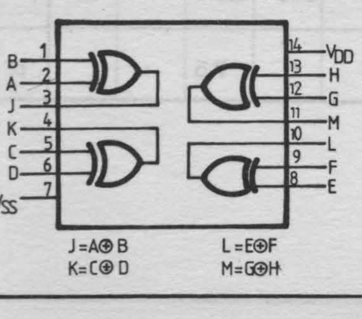
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



TRUTH TABLE

One of four identical gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where „1" = High level
„0" = Low level

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

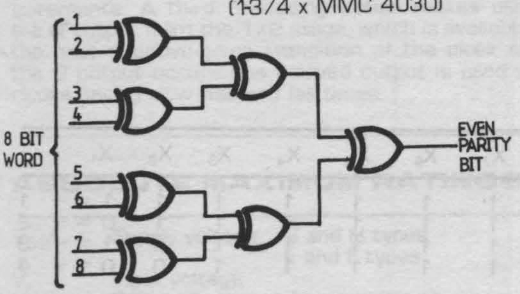
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall time = 20 ns).

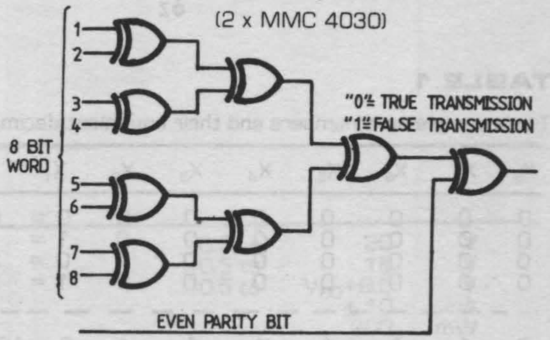
	PARAMETER	TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min	typ	max	
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		140 65 50	280 130 100	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns

TYPICAL APPLICATIONS

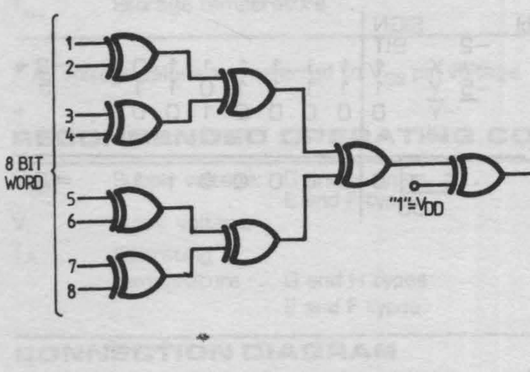
Even-parity-bit generator
(1-3/4 x MMC 4030)



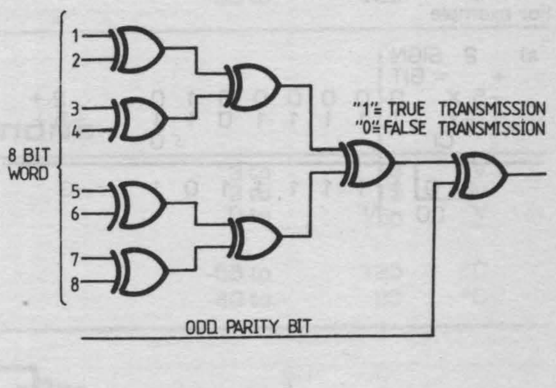
Even-parity checker
(2 x MMC 4030)



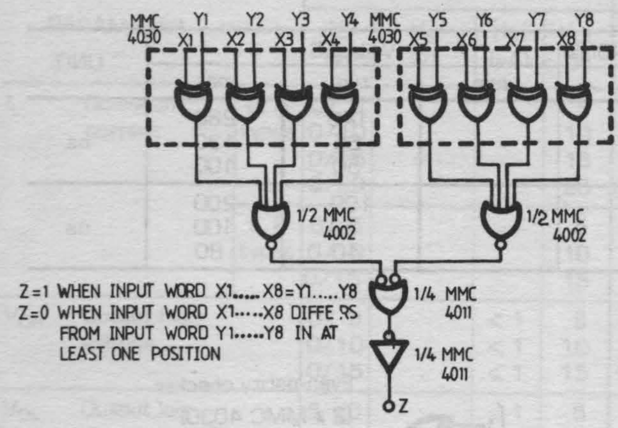
Odd-parity-bit generator
(2 x MMC 4030)



Odd-parity checker
(2 x MMC 4030)



8-bit comparator



8-bit two's complement adder-substractor

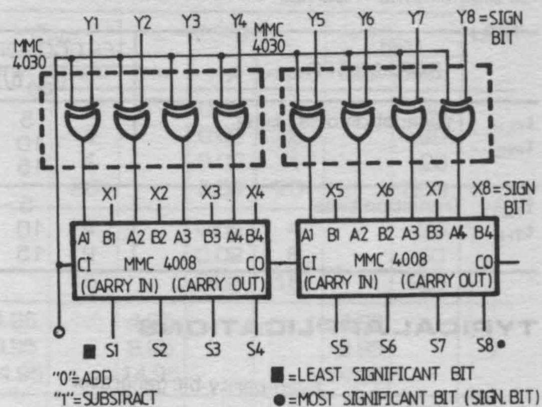


TABLE 1

Two's complement numbers and their equivalent decimal values

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1		X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	
0	0	0	0	0	0	0	0	= 0	1	1	1	1	1	1	1	1	= − 1
0	0	0	0	0	0	0	1	= 1	1	1	1	1	1	1	1	0	= − 2
0	0	0	0	0	0	1	0	= 2	1	1	1	1	1	1	0	1	= − 3
0	0	0	0	0	0	1	1	= 3	1	1	1	1	1	1	0	0	= − 4
0	1	1	1	1	1	1	0	= 126	1	0	0	0	0	0	0	1	= −127
0	1	1	1	1	1	1	1	= 127	1	0	0	0	0	0	0	0	= −128

The two's complement adder-substractor can add or substract any two of the numbers in TABLE 1.

For example

a)

```
      2  SIGN
 +       = BIT
 -5  X      0 0 0 0 0 0 1 0       2 +
    -Y      1 1 1 1 1 0 1 1      -5 +
    CI                    0
 -----------------------------------
  S  0 |  1 1 1 1 1 1 0 1   = -3
  CO
```

b)

```
            SIGN
 -2         BIT
 - =  X      1 1 1 1 1 1 1 0       -2 +
 -5   Y      1 1 1 1 1 0 1 1       -5
      Y̅      0 0 0 0 0 1 0 0        +
      CI                   1
 -----------------------------------
  S  1 |  0 0 0 0 0 0 1 1      = 3
  CO
```

64-STAGE STATIC SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 4031 is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop.
The MMC 4031 is a monolithic integrated circuit, fabricated in standard Al-gate CMOS technology. It is available in 16-lead dual in-line plastic and ceramic package.
The logic level present at the DATA input of MMC 4031 is transferred into the first stage and shifted one stage at each positive-going clock transition. The MMC 4031 has a MODE CONTROL input that when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. A delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output is used with clocks having slow rise and fall times.

FEATURES

- Fully static operation: dc to 16 MHz, $V_{DD} - V_{SS} = 15$ V
- Standard TTL drive capability on Q output
- Three cascading modes:
  - -- direct clocking for high-speed operation
  - -- delayed clocking for reduced clock drive requirements
  - -- additional 1/2 stage for slow clocks
- Recirculation capability

ABSOLUTE MAXIMUM RATINGS

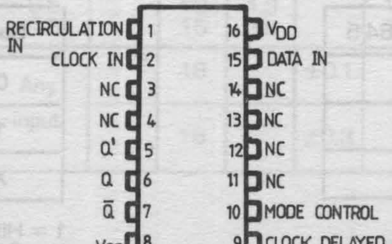
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

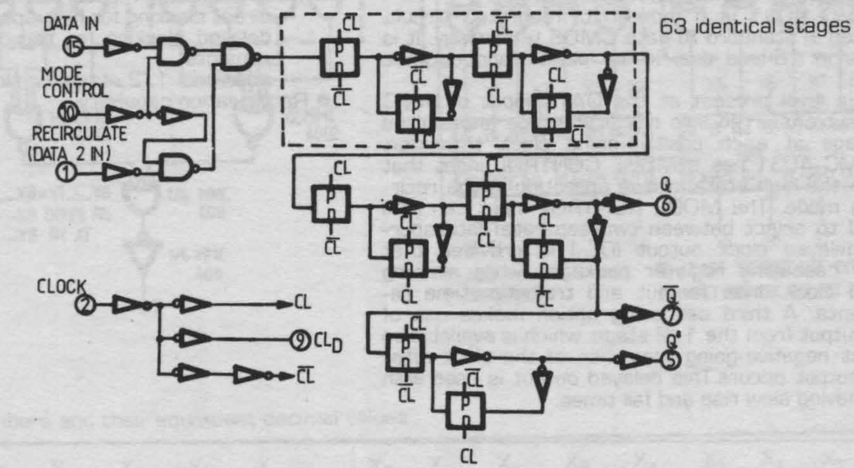
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLES



INPUT CONTROL CIRCUIT

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE

OUTPUT FROM Q' (PIN 5)

Data + 64	CL	Data + 64.5
0	⌐_	0
1	⌐_	1
X	_/‾	NC

1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE, NC = NO CHANGE

TYPICAL STAGE

Data	CL	Data + 1
0	_/‾	0
1	_/‾	1
X	‾_	NC

1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE, NC = NO CHANGE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output source current (source) Q, $\overline{Q}$, Q CL_D	G, H types	0/5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current Q	G, H types	0/5	0.4		5	2.56		2.04	4		1.44		mA
			0/10	0.5		10	6.4		5.2	10.4		3.6		
			0/15	1.5		15	16.8		13.6	27.2		9.6		
		E, F types	0/5	0.4		5	2.08		1.74	4		1.43		
			0/10	0.5		10	5.01		4.42	10.4		3.74		
			0/15	1.5		15	13.6		11.56	27.2		9.52		
I_{OL}	Output sink current $\overline{Q}$, Q' CL_D	G, H types	0/5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
C_I	Input capacitance	Any input							5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times= 20 ns)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PHL}, t_{PLH} t_{PLH}	Propagation delay time: Clock to $\overline{Q}$, Clock to Q	5 10 15		250 110 90	500 220 180	ns
t_{PHL}, t_{PLH} t_{PHL}	Propagation delay time: Clock to Q' Clock to Q	5 10 15		190 80 65	380 160 130	ns
	Clock to CL_D	5 10 15		100 50 40	200 100 80	ns
t_{THL}, t_{TLH}	Transition time (any output, except Q t_{THL})	5 10 15		100 50 40	200 100 80	ns
t_{THL}	Q	5 10 15		50 25 20	100 50 40	ns
t_{setup}	Data setup time	5 10 15		30 15 10	60 30 20	ns
t_{hold},	Data hold time	5 10 15		30 15 10	60 30 20	ns
t_W,	Clock pulse width	5 10 15		120 50 40	240 100 80	ns
t_{max}	Maximum clock input frequency**	5 10 15	2 5 6	4 10 12		MHz
t_r, t_f*	Clock input rise or fall time	5 10 15			1000 1000 200	μs

* If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

** Maximum clock frequency for cascaded units;

a) Using delayed clock feature in recirculation mode:

$$f_{max} = \frac{1}{(n-1)\ CL_D\text{prop. delay} + Q\text{ prop. delay} + \text{set-up time}}$$

where n=number of packages.

b) Not using delayed clock:

$$f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 4035 (G and H types) and MMC 4035 (E and F types) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package The. MMC 4035 integrated circuit is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transfered on positive clock transition. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particulary in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

FEATURES

- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous TRUE/COMPLEMENT control an all outputs
- Static flip-flop operation; master-slave configuration
- Buffered inputs and outputs
- High speed 12 MHz (typ.) at V_{DD} = 10 V.

ABSOLUTE MAXIMUM RATINGS

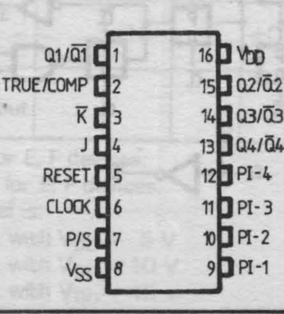
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

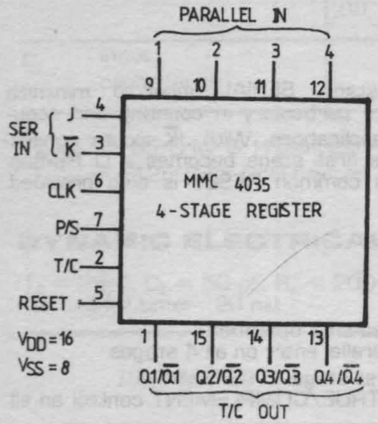
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

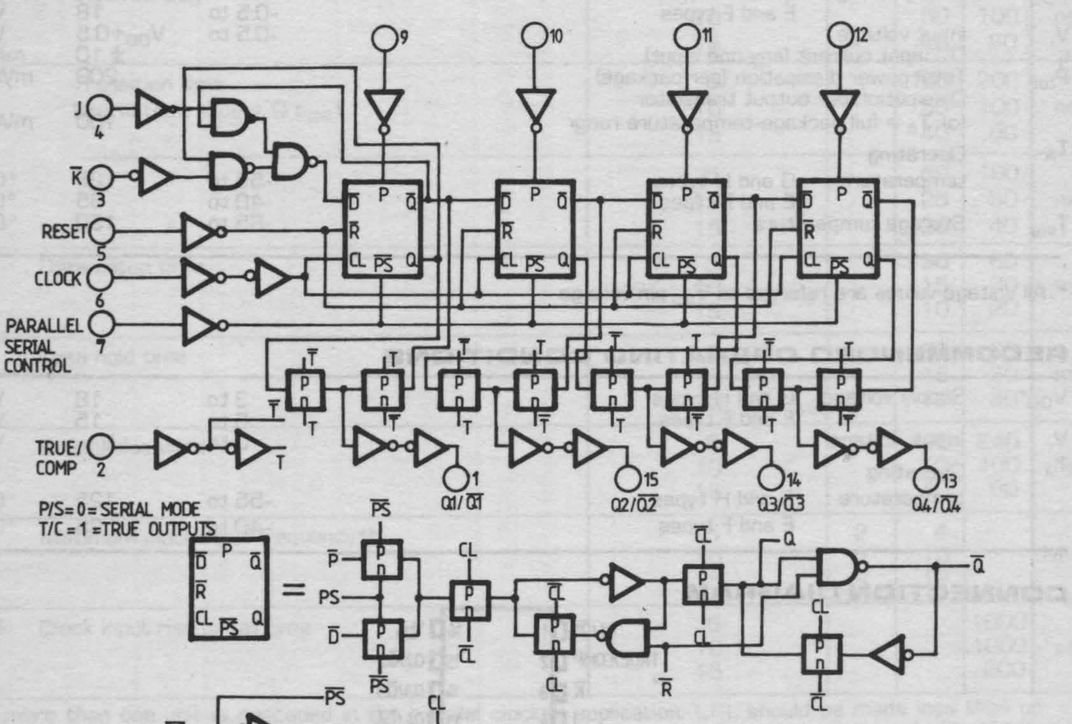


TRUTH TABLE

FIRST STAGE

CLOCK ($\mathscr{C}$)	t_{n-1} (INPUTS) J	K	R	Q_{n-1}	t_n(OUTPUTS) Q_n
_/‾	0	X	0	0	0
_/‾	1	X	0	0	1
_/‾	X	0	0	1	0
_/‾	1	0	0	Q_{n-1}	$\overline{Q}_{n-1}$ TOGGLE MODE
_/‾	X	1	0	1	1
‾_	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	3.6		3.0	6.8		2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.
* $T_{HIGH} = +125$°C for G, H devices; $+85$°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

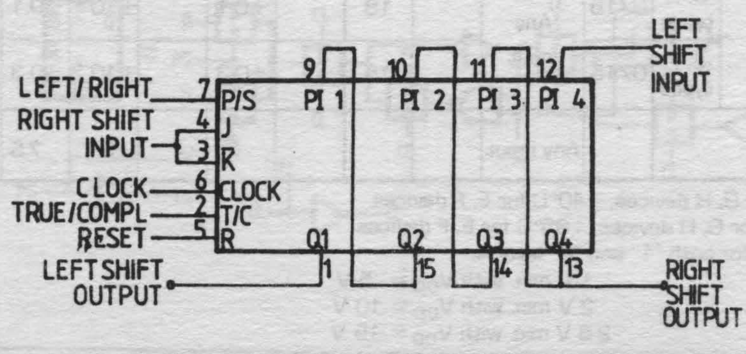
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise rise and fall time = 20 ns)

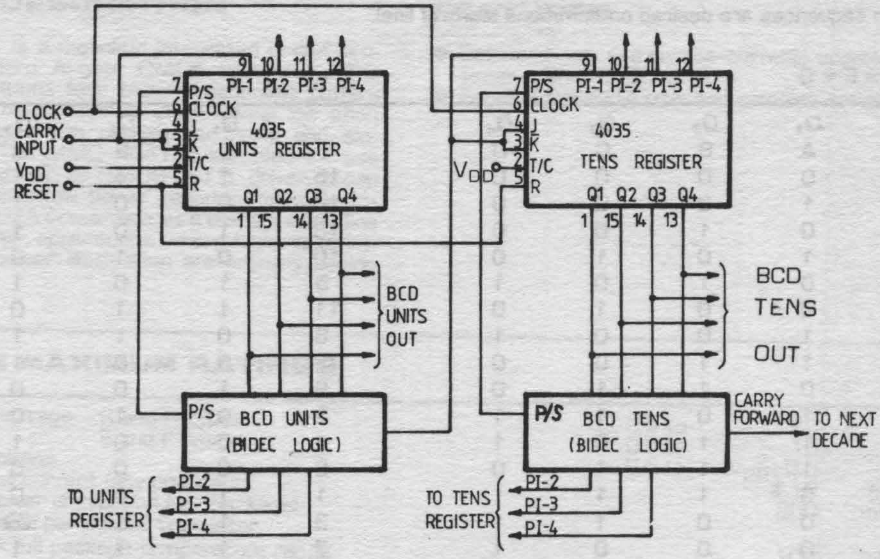
	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	Unit
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time	5		250	500	ns
		10		100	200	
		15		75	150	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	2	4		MHz
		10	6	12		
		15	8	16		
t_W	Clock pulse width	5		100	200	ns
		10		45	90	
		15		30	60	
t_r, t_f	Clock input rise or fall time	5		15		µs
		10		15		
		15		15		
t_{setup}	Data setup time J/$\overline{K}$ lines	5		110	220	ns
		10		40	80	
		15		30	60	
t_{setup}	Data setup time Parallel-In-Lines	5		70	140	ns
		10		25	50	
		15		20	40	
Reset operation						
t_{PLH}, t_{PHL}	Propagation delay time	5		230	460	ns
		10		100	200	
		15		80	160	
t_W	Reset pulse width	5		125	250	ns
		10		55	110	
		15		40	40	

TYPICAL APPLICATIONS

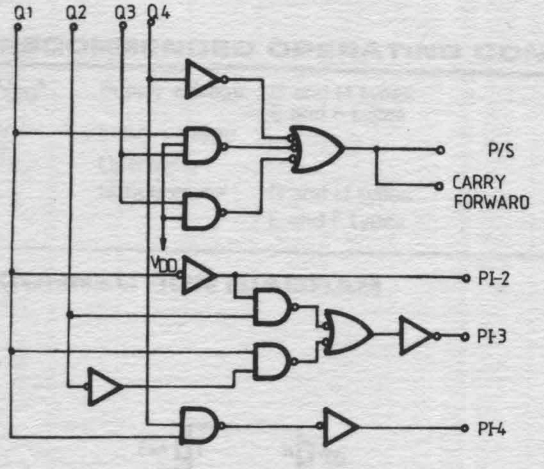
Shift left/shift right register



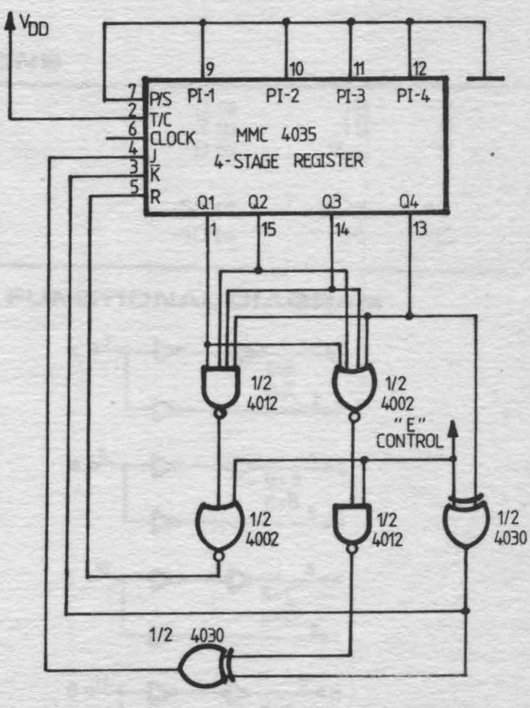
Binary — to — BCD converter



BIDEC logic



Double sequence generator



State sequences

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line).

Control = E = 0

	Q_1 A	Q_2 B	Q_3 C	Q_4 D		Q_1 A	Q_2 B	Q_3 C	Q_4 D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	0	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	09	0
8	0	0	0	1	7	1	1	1	0

QUAD TRUE/COMPLEMENT BUFFER

GENERAL DESCRIPTION

The MMC 4041 is a monolitic integrated circuit processed in standard Al-gate CMOS technology. The MMC 4041 contains four true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The MMC 4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

FEATURES

- Balanced sink and source current; approximately 4 times standard „B" drive
- Equalized delay to true and complement outputs

ABSOLUTE MAXIMUM RATINGS

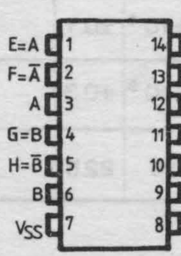
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

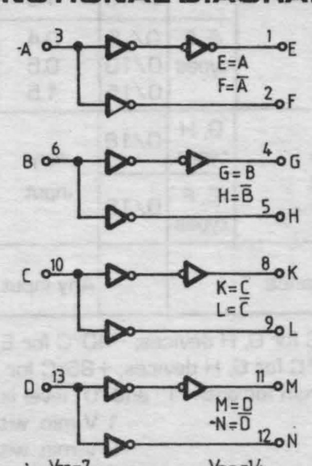
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	—Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				1.5/13.5	< 1	15	12		12			12		
V_{IL}	—Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13.5/1.5	< 1	15		2.5			2.5		2.5	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	-8.4		-6.4	-12.8		-4.6		mA
			0/ 5	4.6		5	-2.1		-1.6	-3.2		-1.2		
			0/10	9.5		10	-6.25		-5	-10		-3.5		
			0/15	13.5		15	-24		-19	-38		-13		
		E, F types	0/ 5	2.5		5	-6.8		-5.44	-12.8		-4.08		
			0/ 5	4.6		5	-1.7		-1.36	-3.2		-1.02		
			0/10	9.5		10	-5.31		-4.25	-10		-3.18		
			0/15	13.5		15	-20.18		-16.15	-38		-12.1		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	2.1		1.6	3.2		1.2		mA
			0/10	0.5		10	6.25		5	10		3.5		
			0/15	1.5		15	24		19	38		13		
		E, F types	0/ 5	0.4		5	1.7		1.36	3.2		1.02		
			0/10	0.5		10	5.31		4.25	10		3.18		
			0/15	1.5		15	20.18		16.15	38		12.11		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						15	22.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} =$ 5 V

2 V min. with $V_{DD} =$ 10 V

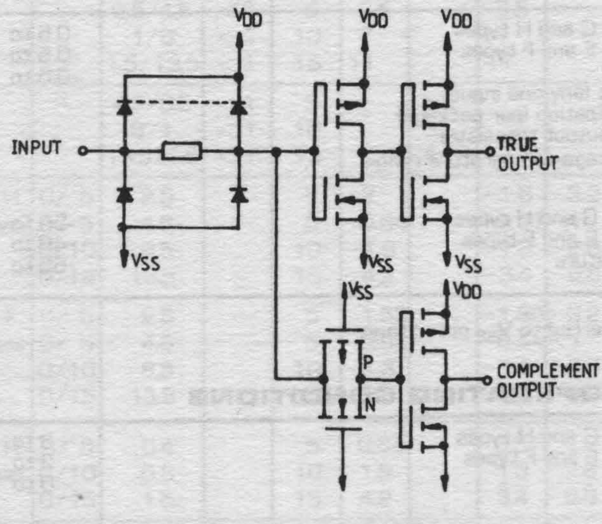
2.5 V min. with $V_{DD} =$ 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		VDD(V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		60	120	ns
		10		35	70	
		15		25	50	
t_{THL}, t_{THL}	Transition time	5		40	80	ns
		10		20	40	
		15		15	30	

SCHEMATIC DIAGRAM



QUAD CLOCKED „D" LATCH

GENERAL DESCRIPTION

The MMC 4042 is a monolithic integrated circuit, available in 16-lead dual in-line plastic package. The MMC 4042 contains four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit.
Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the I CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

FEATURES

- Medium-speed operation
- Fully static operation
- Low power TTL compatible
- Common CLOCK
- Buffered inputs and outputs

ABSOLUTE MAXIMUM RATINGS

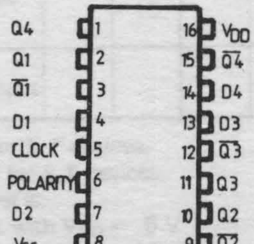
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS
(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

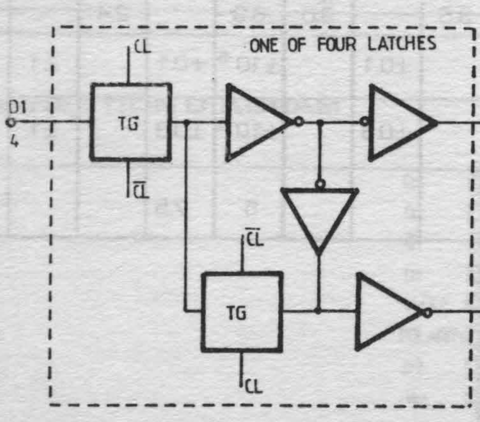
* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, typical temperature coeficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

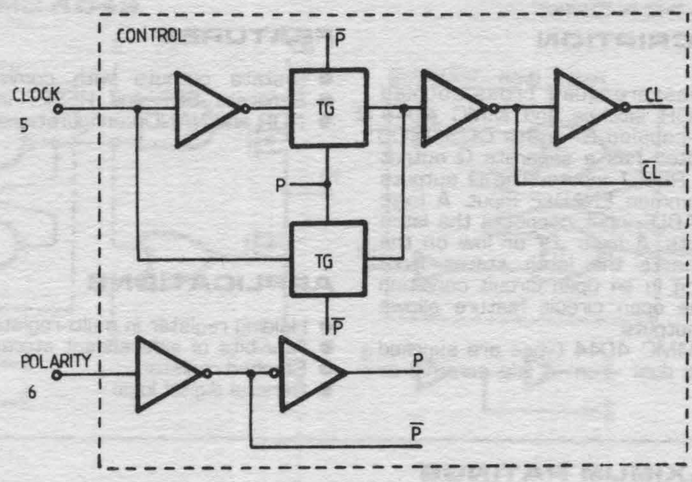
PARAMETER			TEST CONDITIONS V_{DD}(V)	VALUES Min.	VALUES Typ.	VALUES Max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	Data In to Q	5 10 15		110 55 40	220 110 80	ns
		Data In to $\overline{Q}$	5 10 15		150 75 50	300 150 100	ns
		Clock to Q	5 10 15		225 100 80	450 200 160	ns
		Clock to $\overline{Q}$	5 10 15		250 115 90	500 230 180	ns
t_{THL}, t_{TLH}	Transition time		5 10 15		100 50 40	200 100 80	ns
t_W,	Clock pulse width		5 10 15	200 100 60	100 50 30		ns
t_{setup},	Setup time		5 10 15	50 30 25	0 0 0		ns
t_{hold},	Hold time		5 10 15	120 60 50	60 30 25		ns
t_r, t_f,	Clock input rise and fall time		5 10 15	Not rise or fall time sensitive			ns

LOGIC DIAGRAM



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	D
	0	LATCH
1	1	D
	1	LATCH


CONTROL
CLOCK
5
P̄
TG
P
TG
P̄
CL
C̄L̄
POLARITY
6
P
P̄

QUAD 3-STATE R/S LATCHES:
QUAD NOR R/S LATCH-MMC 4043
QUAD NAND R/S LATCH-MMC 4044

GENERAL DESCRIPTION

The MMC 4043 types are quad cross-coupled 3-state COS/MOS NOR latches and MMC 4044 types are quad cross-coupled 3—state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic „1" or high on the ENABLE input connects the latch states to the Q outputs. A logic „0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.
The MMC 4043 and MMC 4044 types are supplied in 16 — lead hermetic dual — in — line ceramic or plastic packages.

FEATURES

- 3-state outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations

APPLICATIONS

- Holding register in multi-register system
- Four-bits of independent storage with output enable
- Strobed register
- General digital logic

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

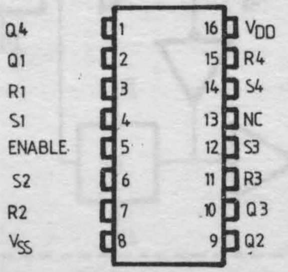
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

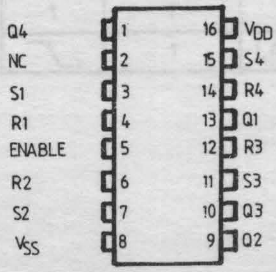
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

MMC 4043

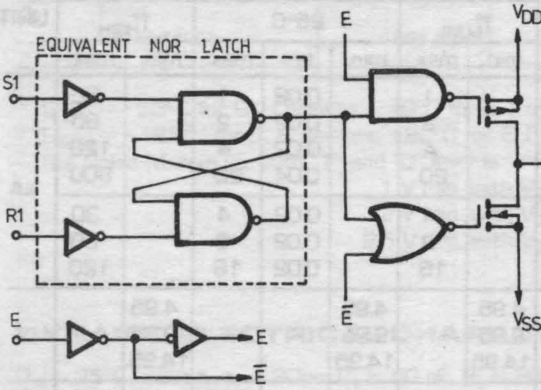


MMC 4044

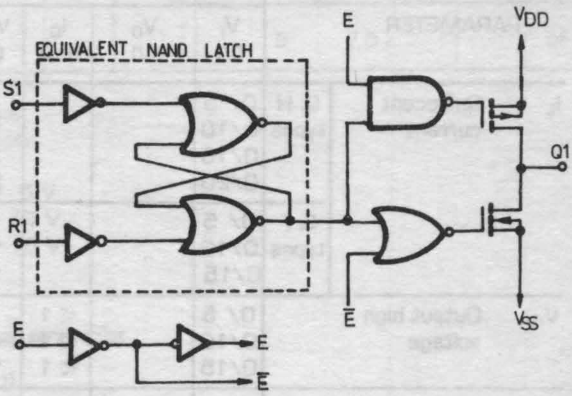


LOGIC DIAGRAMS

MMC 4043

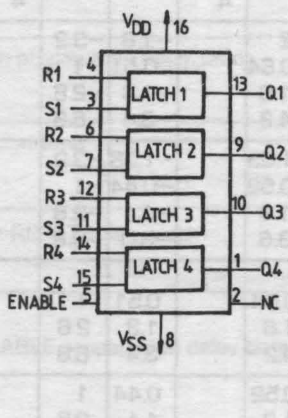


MMC 4044

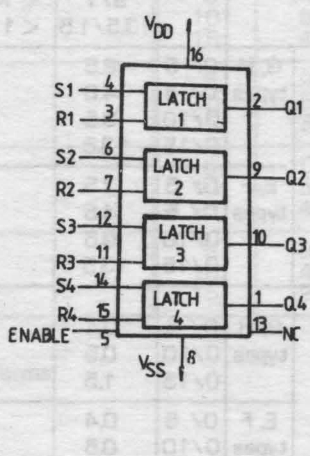


FUNCTIONAL DIAGRAMS

For 4043



For 4044



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm10^{-4}$	±1.0		±7.5	

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
C_I	Input capacitance		Any input						5	7.5			pF

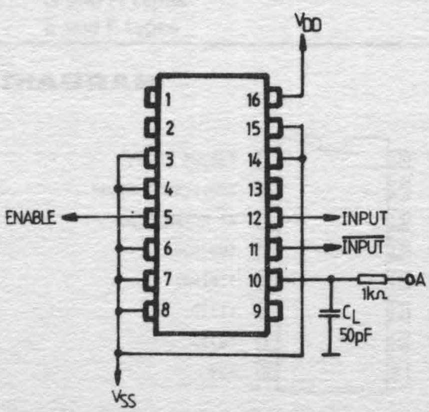
* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, input t_r, $t_f = 20$ns, $C_L = 50$ pF, $R_L = 200$ kΩ)

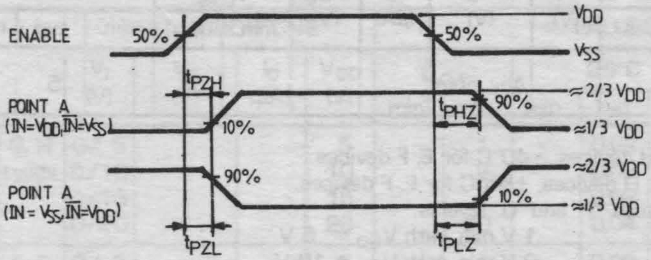
PARAMETER		V_{DD} (V)	VALUES		UNITS
			typ.	max.	
t_{PLH} t_{PHL}	Propagation delay time (SET or RESET to Q)	5 10 15	150 70 50	300 140 100	ns
t_{PHZ} t_{PZH}	3-state propagation delay time (ENABLE to Q)	5 10 15	115 55 40	230 110 80	ns
t_{PLZ} t_{PZL}	3-state propagation delay time	5 10 15	90 50 35	180 100 70	ns
t_{THL} t_{TLH}	Transition time	5 10 15	100 50 40	200 100 80	ns
t_w	SET or RESET pulse width	5 10 15	80 40 20	160 80 40	ns

TEST CIRCUITS ENABLE propagation delay time and waveforms



TEST	IN	$\overline{IN}$	A
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}	V_{SS}
t_{PZL}	V_{SS}	V_{DD}	V_{DD}

Z = HIGH IMPEDANCE


ENABLE
50%
50%
V_{DD}
V_{SS}
t_{PZH}
POINT A
($IN=V_{DD}, \overline{IN}=V_{SS}$)
10%
$\approx 2/3\ V_{DD}$
t_{PHZ}
90%
$\approx 1/3\ V_{DD}$
90%
POINT A
($IN=V_{SS}, \overline{IN}=V_{DD}$)
$\approx 2/3\ V_{DD}$
10%
$\approx 1/3\ V_{DD}$
t_{PZL}
t_{PLZ}

MICROPOWER PHASE -LOCKED LOOP

GENERAL DESCRIPTION

The MMC 4046 micropower phase-locked loop (PLL) consists of a low powere, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two stage comparators. The two phase comporators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

FEATURES

- Wide supply voltage range −3V to 18V
- Low dynamic power consumption −70 μW (typ) at f_0=10 kHz, V_{DD}=5V
- VCO frequency −1.3 MHz (typ) at V_{DD}=10V
- Low frequency drift with temperature −0.6%/C at V_{DD}=10V
- High VCO linearity −1% (typ)

APPLICATIONS

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- Motor speed control

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

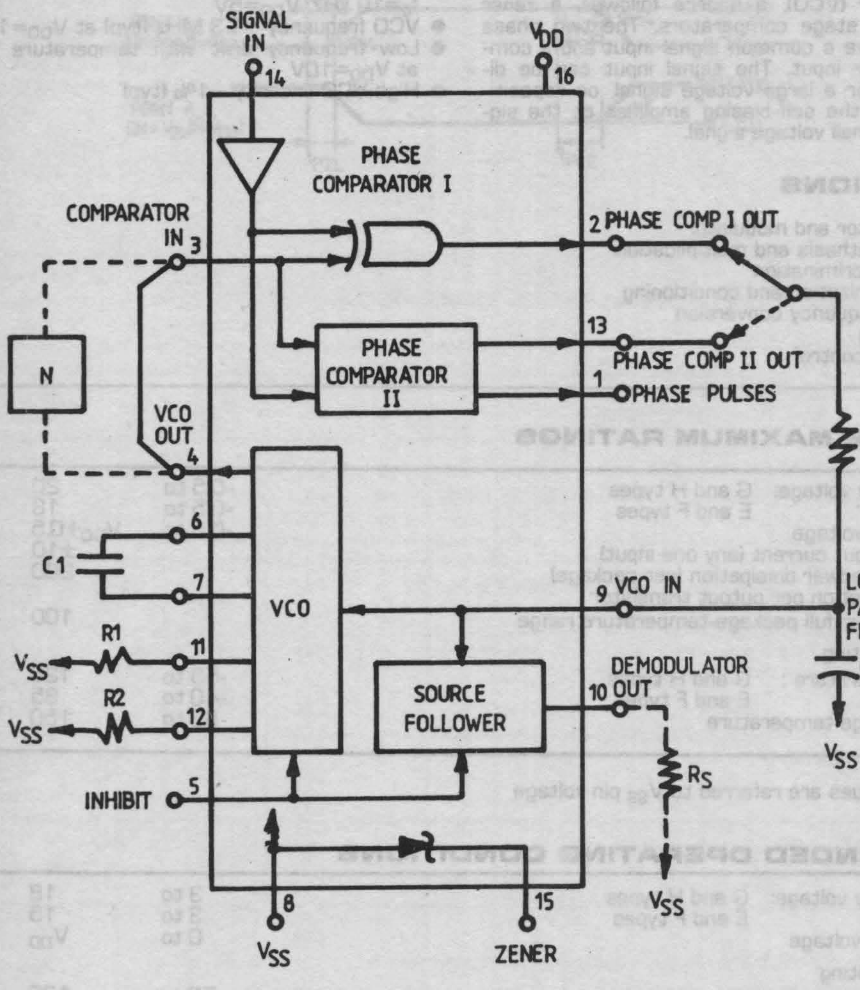
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

PHASE PULSES	1	16	Vdd
PHASE COMP.I.OUT	2	15	ZENER
COMPARATOR IN	3	14	SIGNAL IN
VCO OUT	4	13	PHASE COMP.II.OUT
INHIBIT	5	12	R2
C1(1)	6	11	R1
C1(2)	7	10	DEMODULATED OUT
Vss	8	9	VCO IN

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

VCO SECTION

The VCO requires one external capacitor C1 and one or two external resistors (R_1 or R_1 and R_2). Resistor R_1 and capacitor C_1 determine the frequency range of the VCO and resistor R_2 enables the VCO to have a frequency offset if required. The high input impedance (10^{12} Ω) of the VCO simplifiers the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios in order not to load the low pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10K or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the MMC 4024, MMC 4018, MMC 4020, MMC 4022, MMC4029, MMC4059. One or more MMC 4018 (Presettable Divide-by-N-Counter) or MMC 4029 (presettable Up/Down Counter), together with the MMC 4046, (phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input „enables" the VCO and the source follower, while a logic 1 „turns off" both to minimize standby power consumption.

PHASE COMPARATORS

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels /logic "0" < 30% (V_{DD}—V_{SS}), logic "1" > 70% (V_{DD}—V_{SS})/. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; ot operates analogously to an over-driver balanced mixer.. To maximize the lock range, the signal-and comparator -input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is <the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock into input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. (a) shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition f_0 is shown in Fig. (b).

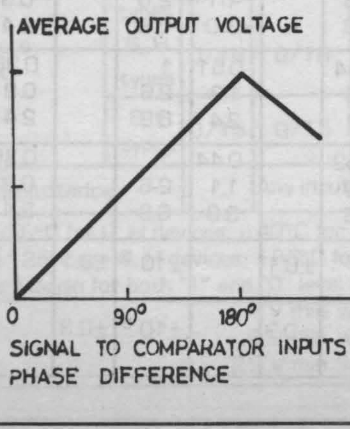
Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output comprising p-and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained On most of the time, and both n-and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is mainteined ON most of the time, and both the n-and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected th this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p-and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. More-over, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p-and n-type output drivers are OFF for most of the signal input cycle.

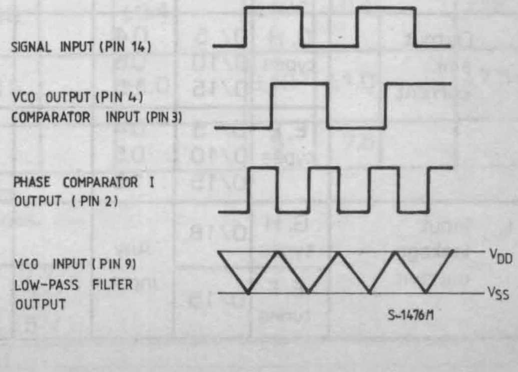
It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. (c) shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

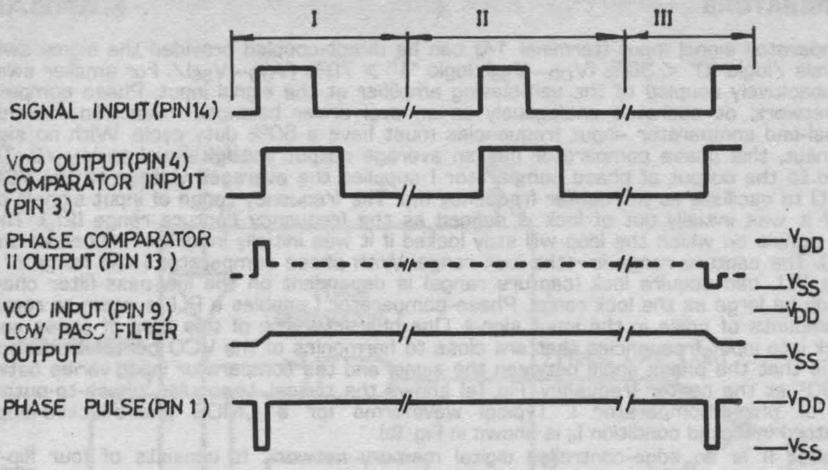
Fig. (a) — Phase comparator I characteristics low-pass filter output

Fig. (b) — Typical waveforms for CMOS Phase Locked-Loop empleying phose comparator I in locked condition of fo.

Fig. (c) — Typical waveforms for CMOS Phase-Locked-Loop employing phase comparator II in locked condition.







NOTE: DASHED LINE IS AN OPEN-CIRCUIT CONDITION

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
VCO SECTION														
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		V
			0/15		<1	15	14.95		14.95			14.95		V
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	V
			15/0		<1	15		0.05			0.05		0.05	V
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		mA
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		mA
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		mA
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		mA
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		mA
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		mA
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		mA
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		mA
			0/15	1.5		15	4.2		3.4	6.8		2.4		mA
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		mA
			0/10	0.5		10	1.3		1.1	2.6		0.9		mA
			0/15	1.5		15	3.6		3.0	6.8		2.4		mA
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	μA

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	UNIT
PHASE COMPARATOR SECTION													
I_{DD} Total device current		0/ 5			5		0.1		0.05	0.1		0.1	
Pin 14=open		0/10			10		0.5		0.25	0.5		0.5	mA
Pin 5=V_{DD}		0/15			15		1.5		0.75	1.5		1.5	
		0/20			20		4		2	4		4	
Pin 14=V_{SS} or V_{DD}	G, H types	0/ 5			5		5		0.04	5		150	
Pin 5=V_{DD}		0/10			10		10		0.04	10		300	
		0/15			15		15		0.04	20		600	
		0/20			20		100		0.08	100		3000	μA
	E, F types	0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V_{IH} —Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		
			1/9	< 1	10	7		7			7		V
			1.5/13.5	< 1	15	11		11			11		
V_{IL} —Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	
			9/1	< 1	10		3			3		3	V
			13.5/1.5	< 1	15		4			4		4	
I_{OH} —Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		
		0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
		0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
		0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		mA
	E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
		0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
		0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
		0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL} —Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		mA
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL} —Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
	E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH} 3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
	E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	
C_I —Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A=25°C; C_L=50pF; R_L=200K; typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns).

	PARAMETER	TEST CONDITIONS		V_{DD} (V)	Min.	Typ.	Max.	UNIT
VCO SECTION								
P_D	Operating power dissipation	f_0=10kHz $R_2=\infty$	R_1=1MΩ V_{COIN}=VDD/2	5 10 15		70 800 3000	140 1600 6000	μW
f_{max}	Maximum frequency	R_1=10K $R_2=\infty$	C_1=50pF	5 10	0.3 0.6	0.6 1.2		MHz
		V_{COIN}=VDD		15	0.8	1.6		
		R_1=5K $R_2=\infty$ V_{COIN}=VDD	C_1=50pF	5 10 15	0.5 1 1.4	0.8 1.4 2.4		
	Center frequency (fo) and frequency range $f_{max}-f_{min}$	Programmable with external components R_1, R_2 and C_1						
	Linearity	V_{COIN}=2.5V±0.3	R_1=10K	5		1.7		%
		V_{COIN}=5V±1	R_1=100K	10		0.5		
		V_{COIN}=5V±2.5	R_1=400K	10		4		
		V_{COIN}=7.5V±1.5	R_1=100K	15		0.5		
		V_{COIN}=7.5V±5	R_1=1M	15		7		
	Temperature frequency stability (no frequency offset) f_{min} = 0			5 10 15		±0.12 ±0.04 ±0.015		%/°C
	Frequency offset $f_{min}\neq0$			5 10 15		±0.09 ±0.07 ±0.03		
V_{CO}	Output duty cycle			5,10,15		50		%
t_{THL}, t_{TLH}	VCO output transition time			5 10 15		100 50 40	200 100 80	ns
	Source follower output (demodulated output): offset voltage $V_{COIN}-V_{DEM}$	RS>10k		5,10,15		1.8	2.5	V
	Source follower output (demodulated output): Linearity	V_{COIN}=2.5V±0.3	R_S=100K	5		0.3		%
		V_{COIN}=5V±2.5	R_S=300K	10		0.7		
		V_{COIN}=7.5V±5	R_S=500K	15		0.9		
V_Z	Zener diode voltage	I_Z=50μA			4.45	5.5	6.15	V
R_Z	Zener dynamic resistance	I_Z=1mA				40		Ω

PHASE COMPARATOR SECTION

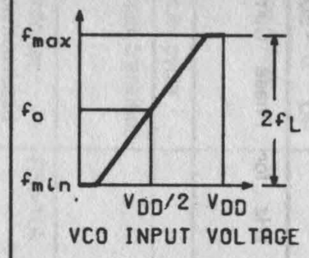
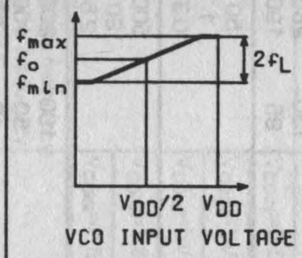
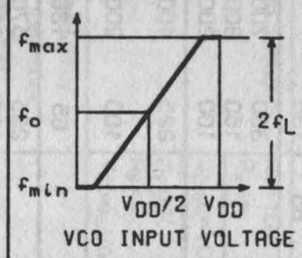
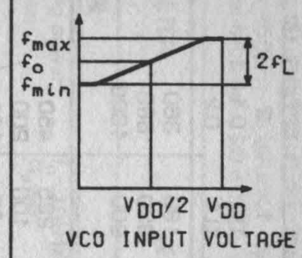
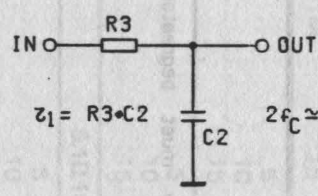
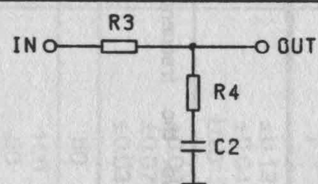
R14 Pin 14 (signal in) input rezistance		5 10 15	1 0.2 0.1	2 0.4 0.2		MΩ
A.C. coupled signal input voltage sensitivity✲ (peak-to-peak)	f_{IN}=100KHz sine wave	5 10 15	180 330 900	360 660 1800		mV
t_{PHL}, Propagation delay time High to low level Pins 14 to 13		5 10 15	225 100 65	450 200 130		ns
t_{PLH}, Propagation delay time Low to high, level		5 10 15		350 150 100	700 300 200	ns
t_{PHZ}, Propagation delay time 3-state High level to High impedance Pins 14 to 13		5 10 15		225 100 65	450 200 130	ns
t_{PLZ}, Low level to high impedance		5 10 15		285 130 95	570 260 190	ns
t_r, t_f, Input rise or fall time Comparator Pin 3		5 10 15			50 1 0.3	µs
Signal Pin 14		5 10 15			500 20 2.5	µs
t_{THL}, Transition time t_{TLH}		5 10 15		100 50 40	200 100 80	ns

✲ For sine wave the frequency must begreater than 10 kHz for Phase Comparator 11.

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the 4046 in a Phase -Locked-Loop system. The selected external components must be within the following ranges.

5 k <R_1, R_2, RS<1M C1>100pF at V_{DD}>5V C1>50pF at V_{DD}>10V

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL systems will adjust to centre frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	 $\tau_1 = R3 \bullet C2$ $2f_C \simeq \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau_1}}$		$f_C = f_L$	
Loop Filter Component Selection				
Phase Angle beetwen Signal and Comparator	90^o at centre frequency (f_o), approximating 0^o and 180^o at ends of look range ($2f_L$)		Always 0^o in lock	
Looks on Harmonics of Centre Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

LOW-POWER MONOSTABLE/ ASTABLE MULTIVIBRATOR

GENERAL DESCRIPTION

The MMC 4047 is a monolithic integrated circuit processed in standard Al-gate CMOS technology available in 14 lead dual in-line package. The MMC 4047 consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options. Inputs include +TRIGGER,-TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and EXTERNAL RESET. Buffered outputs are Q,$\overline{\text{Q}}$ and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and C-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

FEATURES

- Low-power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-runing) operation
- True and complemented buffered outputs
- Only one external R and C required
- Buffered inputs

ABSOLUTE MAXIMUM RATINGS

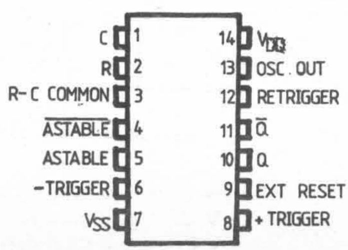
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

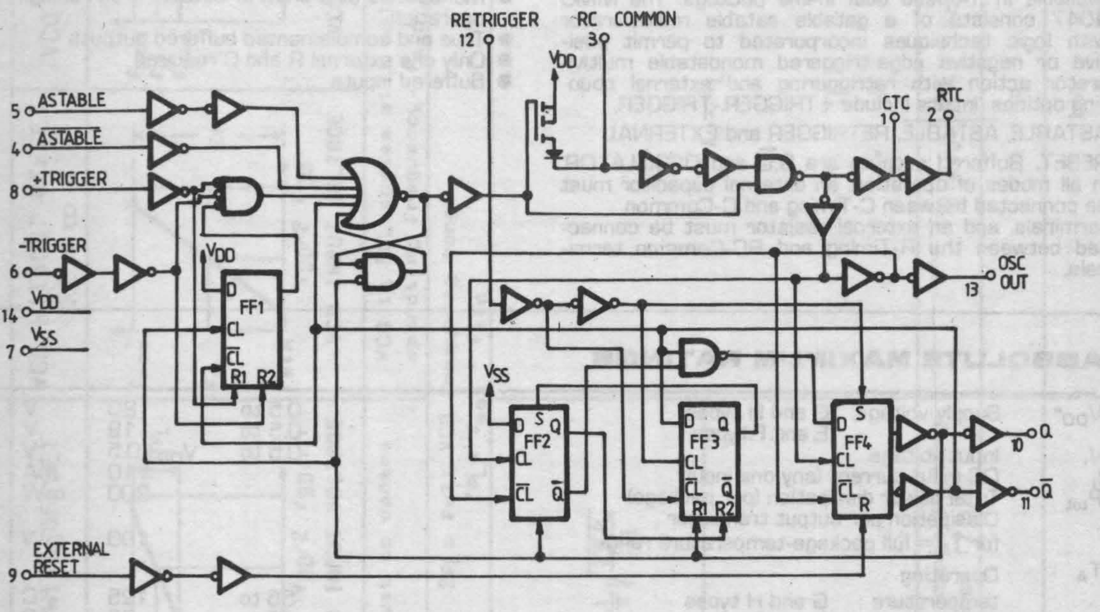
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM



FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION*	TERMINAL CONNECTIONS: TO V_{DD}	TO V_{SS}	INPUT PULSE TO	OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
Astable multivibrator:					
Free running	4, 5, 6, 14	7, 8, 9, 12	—	10,11, 13	t_A(10, 11)=4.40 RC
True gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A(13)=2.20 RC
Complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable multivibrator:					
Positive-edge trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-edge trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M(10, 11)=2.48 RC
External countdown**	14	5, 6, 7, 8, 9, 12	—	10, 11	

* In all cases external capacitor and resistor between pins 1, 2 and 3 (see logic diagrams)

** Input pulse to reset of external counting chip.
External counting chip output to pin 4

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 15 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	Astable, $\overline{\text{Astable}}$ to osc. out	5		200	400	ns
			10		100	200	
			15		80	160	
		Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	5		350	700	ns
			10		175	350	
			15		125	250	
		+ or − Trigger to Q, $\overline{Q}$	5		500	1000	ns
			10		225	450	
			15		150	300	
		Retrigger to Q, $\overline{Q}$	5		300	600	ns
			10		150	300	
			15		100	200	
		External Reset to Q, $\overline{Q}$	5		250	500	ns
			10		100	200	
			15		70	140	
t_{THL}, t_{TLH}	Transition time osc. out Q, $\overline{Q}$		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Input pulse width:	+Trigger, −Trigger	5		200	400	ns
			10		80	160	
			15		50	100	
		Reset	5		100	200	ns
			10		50	100	
			15		30	60	
		Retrigger	5		300	600	ns
			10		115	230	
			15		75	150	
t_r, t_f	Input rise and fall time All inputs		5		Unlimited		μs
			10				
			15				
	Q or $\overline{Q}$ deviation from 50% Duty factor		5		±0.5	±1	%
			10		±0.5	±1	
			15		±0.1	±0.5	

APPLICATION INFORMATION

1 - Circuit description

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. „True" input pulses on the ASTABLE input or „Complement" pulses on the $\overline{\text{ASTABLE}}$ input alow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output. In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGER input and a low level to the −TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the −TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse.

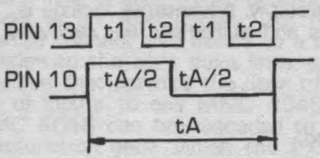
The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components. An external countdown option can be implemented by coupling „Q" to an external „N" counter and resetting the counter with the trigger pulse. The

counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A high level on the EXTERNAL RESET input assures no output pulse during an „ON" power condition. This input can also be activated to terminte the output pulse at any time. In the monostable mode, high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

2 - Astable Mode

The following anlysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33%—67% V_{DD}) for free-running (astable) operation.

Astable mode waveforms



$$t1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

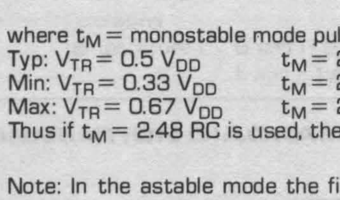
$$t_A = 2(t1 + t2) = -2RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} - V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62\ RC$
Max: $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62\ RC$
thus if $t_A = 4.40\ RC$ is used, the maximum variation will be (+5.0%, − 0.0%) In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature.

3 - Monostable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33%—67% V_{DD}) for one-shot (monostable) operation.

Monostable waveforms



$$t1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{DD}}$$

$$t2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$tM = (t1 + t2) = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = monostable mode pulse width. Values for t_M are as follows:
Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max: $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$
Thus if $t_M = 2.48\ RC$ is used, the maximum variation will be (+9.3% − 0.0%)

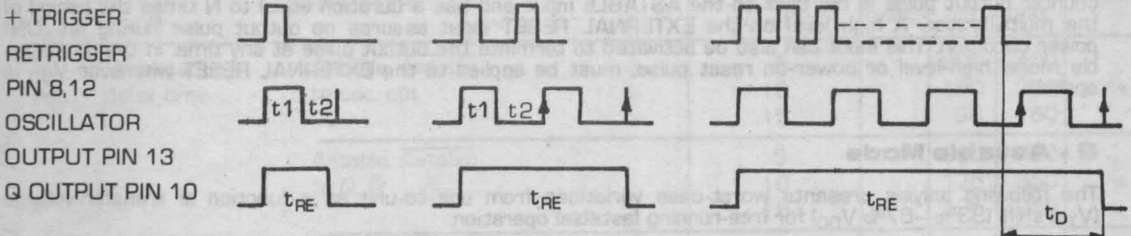
Note: In the astable mode the first positive half cycle has a duration of T_M; succeding durations are $t_A/2$. In addition to variations from unit-to-unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature.

4 - Retrigger mode

The MMC 4047 can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. A normal monostable action is obtained when one retrigger pulse is applied. For two input pulses, $t_{RE} = t_1 + t_1 + 2t_2$.

For more than two pulses, t_{RE}(Q OUTPUT) terminates at some variable time t_D after the termination of the last retrigger pulse. t_D is variable because t_{RE}(Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see logic diagram).

Fig. A` Retrigger-mode waveforms



5-External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration small timing capacitors for long time periods and extremely fast recovery time.
A typical implementation is shown in Fig. B. The pulse duration at the output is

$$t_{ext} = (N-1)t_A + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

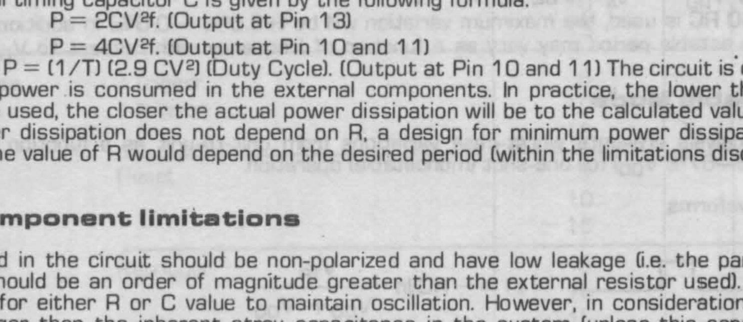
6-Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula:
Astable Mode: $P = 2CV^2f$. (Output at Pin 13)
$P = 4CV^2f$. (Output at Pin 10 and 11)
Monostable Mode: $P = (1/T)\ (2.9\ CV^2)$ (Duty Cycle). (Output at Pin 10 and 11) The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.
Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above).

7 - Timing-component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation. However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.
The reccomended values for these components to maintain agreement with previously calculated formulas without trimming should be:
$C \geq 100$ pF, up to any practical value, for astable modes;
$C \geq 1000$ pF, up to any practical value, for monostable modes. $10k \leq R \leq 1M$.

Fig. B` Implementation of external counter option



MULTIFUNCTION EXPANDABLE 8-INPUT GATE

GENERAL DESCRIPTION

The MMC 4048 (intermediate or extended temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package. The MMC 4018 is an 8-input gate having four control inputs. Three binary control inputs` Ka, Kb, and Kc` provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth control input` Kd` provides the user with a 3-state output. When control input Kd is high the output is either a logic 1 or logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one MMC 4048. For example, two MMC 4048 can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

FEATURES

- Three-state output
- Many logic functions available in one package.

ABSOLUTE MAXIMUM RATINGS

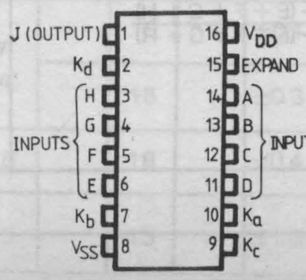
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

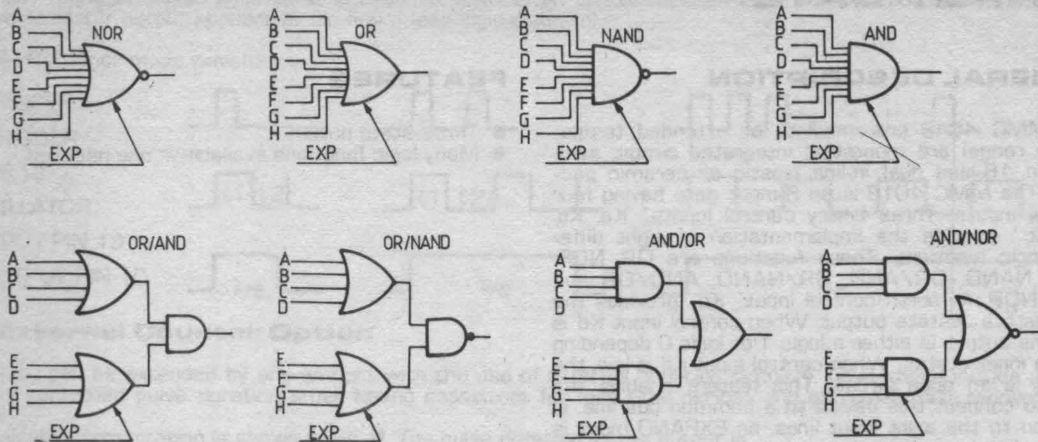
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

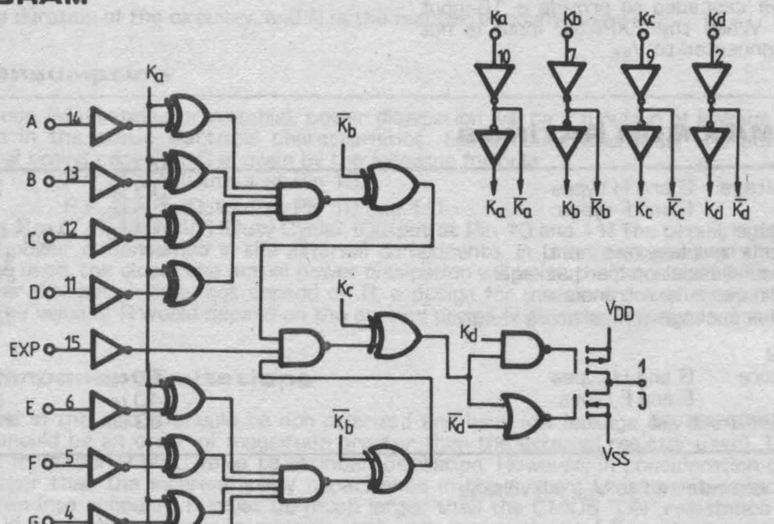
CONNECTION DIAGRAM



BASIC LOGIC CONFIGURATIONS



LOGIC DIAGRAM



FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESION	Ka	Kb	Kc	UNUSED INPUT
NOR	$J = \overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J = A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J = (A+B+C+D) \cdot (E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J = \overline{(A+B+C+D) \cdot (E+F+G+H)}$	0	1	1	V_{SS}
AND	$J = ABCDEFGH$	1	0	0	V_{DD}
NAND	$J = \overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J = \overline{ABCD + EFGH}$	1	1	0	V_{DD}
AND/OR	$J = ABCD + EFGH$	1	1	1	V_{DD}

Kd = 1 Normal Inverter Action
Kd = 0 High Impedance Output

EXPAND Input = o

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

PARAMETER	TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
C_I —Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS	V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time Inputs to output and Ka to Output		5		300	600	ns
			10		150	300	
			15		120	240	
	Kb to Output		5		225	450	ns
			10		85	170	
			15		55	110	
	Kc to Output		5		140	280	ns
			10		50	100	
			15		40	80	
	Expand Input to Output		5		190	380	ns
			10		90	180	
			15		65	130	
t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	3-state propagation delay time Kd to Output	$R_L = 1$ k	5		80	160	ns
			10		35	75	
			15		25	50	
t_{THL}, t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
3-state output capacitance					5	10	pF

HEX BUFFER/CONVERTERS: MMC 4049-INVERTING TYPE MMC 4050-NON-INVERTING TYPE

GENERAL DESCRIPTION

The MMC 4049 and the MMC 4050 are monolithic integrated circuits processed in standard Al-gate CMOS technology. The MMC 4049 and the MMC 4050 are inverting and non-inverting hex-buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{DD}). The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads ($V_{DD} = 5V$, $V_{OL} \leq 0.4V$, and $I_D \geq 3.2mA$).

FEATURES

- High sink current for driving 2TTL loads
- High-to-low level logic conversion
- High sink and source current capability

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

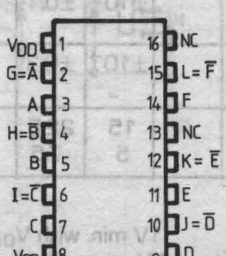
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

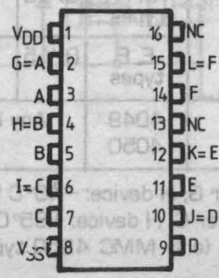
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_I	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

MMC 4049



MMC 4050



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

	PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5		5		1		0.02	1		30	µA
			0/10		10		2		0.02	2		60	
			0/15		15		4		0.02	4		120	
			0/20		20		20		0.04	20		600	
		E, F types	0/ 5		5		4		0.02	4		30	
			0/10		10		8		0.02	8		60	
			0/15		15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		5	4.95		4.95			4.95		V
			0/10		10	9.95		9.95			9.95		
			0/15		15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		5		0.05			0.05		0.05	V
			10/0		10		0.05			0.05		0.05	
			15/0		15		0.05			0.05		0.05	
V_{IH}	Input high voltage (4049)			0.5	5	4		4			4		V
				1	10	8		8			8		
				2	15	12		12			12		
V_{IH}	Input high voltage (4050)			4.5	5	3.5		3.5			3.5		V
				9	10	7		7			7		
				13.5	15	11		11			11		
V_{IL}	Input low voltage (4049)			4.5	5		1			1		1	V
				9	10		2			2		2	
				13	15		3			3		3	
V_{IL}	Input low voltage (4050)			0.5	5		1.5			1.5		1.5	V
				1	10		3			3		3	
				1.5	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5	5	1.6		-1.25	-6.4		-0.9		mA
			0/ 5	4.6	5	0.64		-0.51	-1.6		-0.36		
			0/10	9.5	10	1.6		-1.30	-3.6		-0.9		
			0/15	13.5	15	4.7		-3.75	-12		-2.6		
		E, F types	0/ 5	2.5	5	1.5		-1.25	-6.4		-1		
			0/ 5	4.6	5	0.61		-0.51	-1.6		-0.42		
			0/10	9.5	10	1.5		-1.25	-3.6		-1		
			0/15	13.5	15	4.5		-3.75	-12		-3		
I_{OL}	Output sink current	G, H types	0/ 5	0.4	5	3.75		3.2	6.4		2.2		
			0/10	0.5	10	10		8	16		5.6		
			0/15	1.5	15	30		24	48		17		
		E, F types	0/ 5	0.4	5	3.6		3.2	6.4		2.6		
			0/10	0.5	10	9.6		8	16		6.6		
			0/15	1.5	15	28		24	48		19		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18		18		±0.1		$\pm10^{-5}$	±0.1		±1	µA
		E, F types	0/15		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance	4049	Any input						15	22.5			pF
		4050							5	7.5			

* $T_{LOW} = -55°C$ for G, H device: $-40°C$ for E, F device

* $T_{HIGH} = +125°C$ for G, H device: $+85°C$ for E, F device

The noise margin (only MMC 4050 type) for both „1" and „0" level is:

1V min. with $V_{DD} = 5V$
2V min. with $V_{DD} = 10V$
2.5V min. with $V_{DD} = 15V$

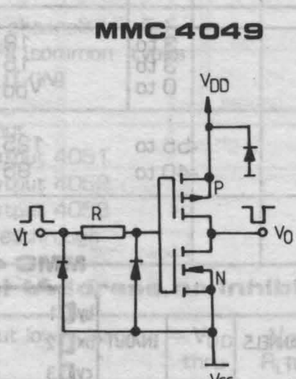
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns).

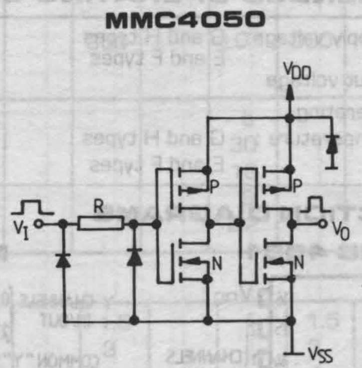
PARAMETER		TEST CONDITIONS V_I(V)	TEST CONDITIONS V_{DD}(V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}	Propagation delay time (4049)	5 10 10 15 15	5 10 5 15 5		60 32 45 25 45	120 65 90 50 90	ns
t_{PLH}	Propagation delay time (4050)	5 10 10 15 15	5 10 5 15 5		70 40 45 30 40	140 80 90 60 80	ns
t_{PHL}	Propagation delay time (4049)	5 10 10 15 15	5 10 5 15 5		32 20 15 15 10	65 40 30 30 20	ns
t_{PHL}	Propagation delay time (4050)	5 10 10 15 15	5 10 5 15 5		55 22 50 15 50	110 55 100 30 100	ns
t_{TLH}	Transition time	5 10 15	5 10 15		80 40 30	160 80 60	ns
$t_{THL'}$	Transition time	5 10 15	5 10 15		30 20 15	60 40 30	ns

SCHEMATIC DIAGRAMS

MMC 4049



MMC4050



ANALOG MULTIPLEXERS-DEMULTIPLEXERS:

4051 SINGLE 8-CHANNEL
4052 DIFFERENTIAL 4-CHANNEL
4053 TRIPLE 2-CHANNEL

GENERAL DESCRIPTION

The MMC 4051, MMC 4052 and MMC 4053 are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic package. MMC 4051, MMC 4052 and MMC 4053 analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}—V_{SS} and V_{DD}—V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a-logic „1" is present at the inhibit input terminal all channel are off. The MMC 4051 is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output. The MMC 4052 is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The MMC 4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a singlepole double-throw configuration.

FEATURES

- Low „ON" resistance: 125 ohm (typ.) over 15 Vp.p. signal-input range for V_{DD}—V_{EE} = 15 V
- High „OFF" resistance: channel leakage ± 100 pA (typ.) V_{DD}—V_{EE} = 18 V
- Binary address decoding on chip
- Very low quiescent power dissipation under all digital control input and supply conditions: 0.2/uW (typ.), V_{DD}—V_{SS} = V_{DD}—V_{EE} = 10 V
- Matched switch characteristics: R_{ON} = 5 ohm (typ.) for V_{DD}—V_{EE} = 15 V
- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 Vp.p.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

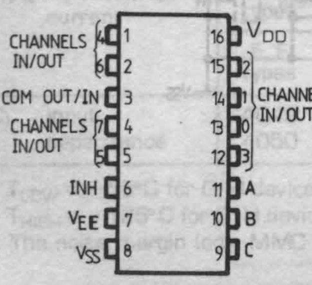
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

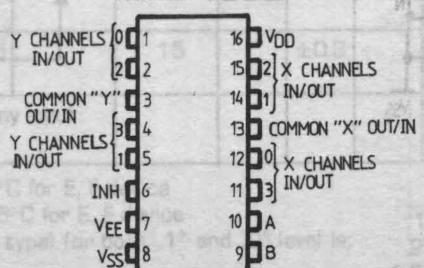
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

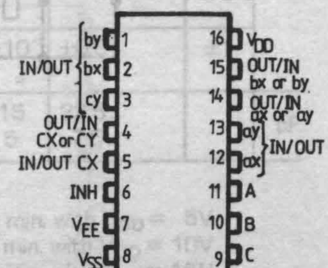
MMC 4051



MMC 4052



MMC 4053



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ.	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	quiescent device current	G, H types				5		5		0.04	5		150	µA
						10		10		0.04	10		300	
						15		20		0.04	20		600	
						20		100		0.08	100		3000	
		E, F types				5		20		0.04	20		150	
						10		40		0.04	40		300	
						15		80		0.04	80		600	
Switch														
ON-resistance		G, H types	$0 \leq V_I \leq V_{DD}$	0	0	5		880		470	1050		1200	Ω
						10		310		180	400		580	
						15		220		125	280		400	
		E, F types	$0 \leq V_I \leq V_{DD}$	0	0	5		880		470	1050		1200	
						10		330		180	400		520	
						15		230		125	280		360	
ΔON-resistance (between any 2 channels)				0	0	5				10				Ω
						10				10				
						15				5				
OFF (●) channel leakage current	Any channel OFF	G, H types		0	0	18		100		±0.1	100		1000	nA
	All channels OFF (common OUT/IN)	G, H types		0	0	18		100		±0.1	100		1000	nA
	Any channel OFF	E, F types		0	0	15		300		±0.1	300		1000	nA
	All channels OFF (common OUT/IN)	E, F types		0	0	15		300		±0.1	300		1000	nA
C-capacitance	Input			−5	−5	5				5				pF
	Output 4051									30				
	Output 4052									18				
	Output 4053									9				
	Feedthrough									0.2				
Control (Address or Inhibit)														
V_{IL}	Input low voltage		$= V_{DD}$ thru 1KΩ	$V_{EE} = V_{SS}$ $R_L = 1K\Omega$ to V_{SS}		5		1.5			1.5		1.5	V
						10		3			3		3	
						15		4			4		4	
V_{IH}	Input high voltage			$I_{IS} > 2\mu A$ (on all OFF channels)		5	3.5		3.5			3.5		V
						10	7		7			7		
						15	11		11			11		

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ.	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_{IH}, I_{IL} Input leakage current	G, H types	$V_I = 0/18$ V			18		±0.1		$±10^{-3}$	±0.1		±1	µA
	E, F types	$V_I = 0/15$ V			15		±0.3		$±10^{-3}$	±0.3		±1	µA
C_I Input capacitance		Any address or inhibit input							5	7.5			pF

(o) Determined by minimum feasible leakage measurement for automatic testing
(*) $T_{Low} = -55°C$ for G, H device; $-40°C$ for E, F device.
$T_{High} = +125°C$ for G, H device; $+85°C$ for E, F device.

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, all input square wave rise and fall time = 20 ns)

PARAMETER	TEST CONDITIONS V_{EE} (V)	R_L (KΩ)	f_i (KHz)	V_{IS} (V)	V_{SS} (V)	V_{DD} (V)			VALUES typ.	VALUES max.	UNIT
Switch											
t_{pd}-Propagation delay time (Signal Input to output)		200		10 V (pulse)		5			30	30	ns
						10			15	60	
						15			11	20	
Frequency response channel „ON" (Sine wave Input) at $20 \log \frac{V_0}{V_I} = -3$ dB	$=V_{SS}$	1		5(•)		10	VO at common OUT/IN	4053	30		MHz
								4052	25		
								4051	20		
							V_0 at any channel		60		MHz
Feedthrough (all channels OFF) at $20 \log \frac{V_0}{V_1} = -40$ dB	$=V_{SS}$	1		5(•)		10	V_0 at common OUT/IN	4053	8		MHZ
								4052	10		
								4051	12		
							V_0 at any channel		8		MHz
Frequency signal crosstalk at $20 \log \frac{V_0}{V_I} = -40$ dB	$=V_{SS}$	1		5(•)		10	Between any 2 channels		3		MHz
							Between sections 4052 only	Measured on common	6		
								Measured on any channel	10		
							Between any 2 sections 4053 only	In pin 2 out pin 14	2.5		
								In pin 15 out pin 14	6		
Sine wave distortion $f_{IS} = 1$ KHz sine wave	$=V_{SS}$	10	1	2(•)		5			0.3		%
		10	1	3(•)		10			0.2		
		10	1	5(•)		15			0.12		

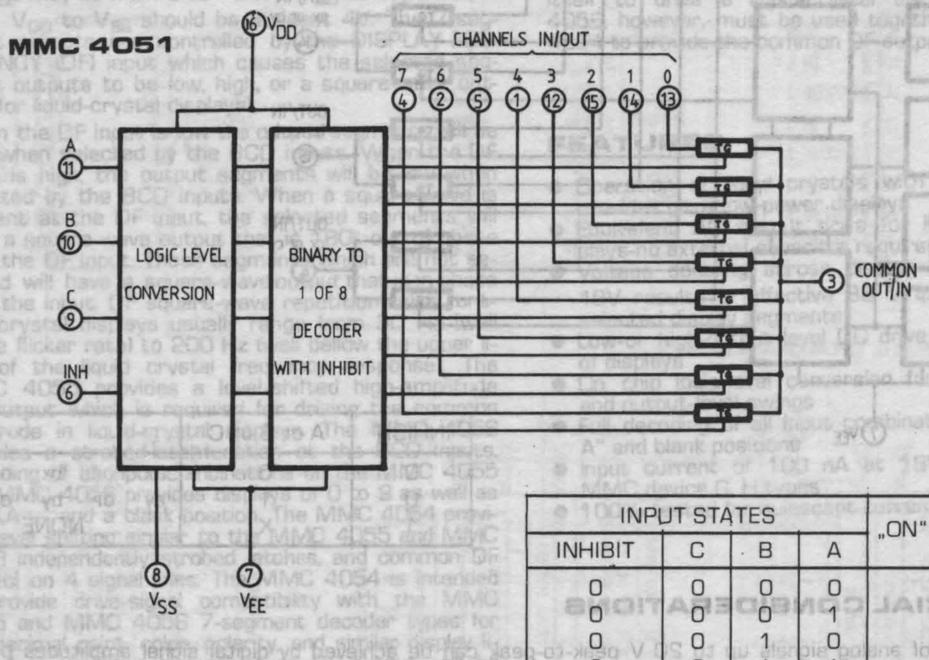
PARAMETER	TEST CONDITIONS V_{EE} (V)	R_L (K)	f_i (KHz)	V_{IS} (V)	V_{SS} (V)	V_{DD} (V)	VALUES typ.	max.	UNIT
Control (address or inhibit)									
Propagation delay time: Address-to signal OUT channels ON or OFF	0 0 0 − 5				0 0 0 0	5 10 15 5	360 160 120 225	720 320 240 450	ns
Propagation delay time: Inhibit to signal OUT (channel turning ON)	0 0 0 − 10	10			0 0 0 0	5 10 15 5	360 160 120 200	720 320 240 400	ns
Propagation delay time: Inhibit to signal OUT (channel turning OFF)	0 0 0 − 10	0.3				5 10 15 5	200 90 70 130	450 210 160 300	ns
Address or inhibit to signal crosstalk	0	10(✲)				10 $V_C = V_{DD} - V_{SS}$ (Square wave)	65		mV peak

(●) Peak to peak voltage symetrical about $\frac{V_{DD} - V_{EE}}{2}$

(✲) Both ends of channel.

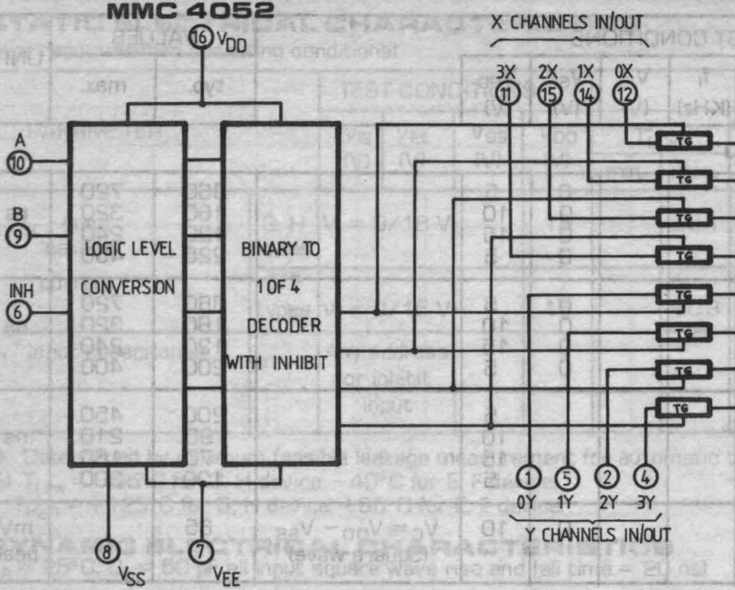
FUNCTIONAL DIAGRAMS AND TRUTH TABLES

MMC 4051



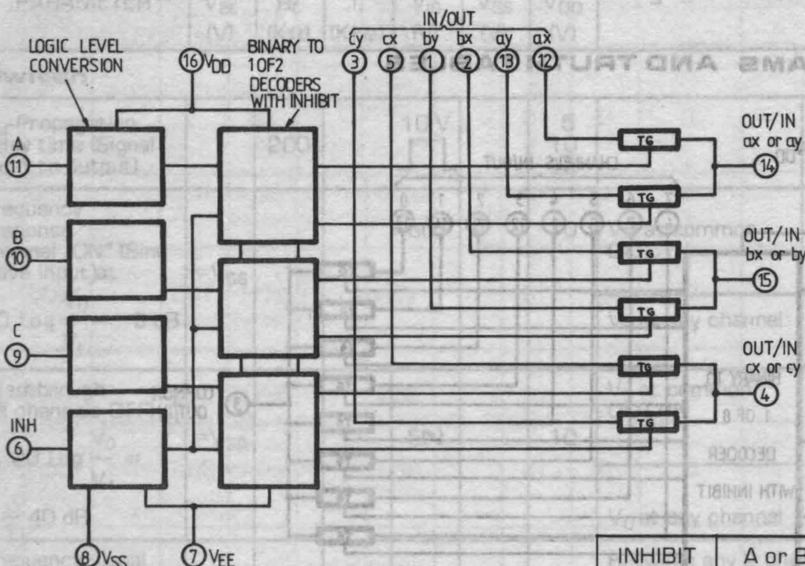
INPUT STATES INHIBIT	C	B	A	„ON" CHANNEL(S)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE

MMC 4052



INHIBIT	B	A	
0	0	0	0x, 0y
0	0	1	1x, 1y
0	1	0	2x, 2y
0	1	1	3x, 3y
1	X	X	NONE

MMC 4053



INHIBIT	A or B or C					
0	0	ax	or	bx	or	cx
0	1	ay	or	by	or	cy
1	X	NONE				

SPECIAL CONSIDERATIONS

Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if $V_{DD}-V_{SS} = 3$ V, a $V_{DD}-V_{EE}$ of up to 13 V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13 V, a $V_{DD}-V_{SS}$ of at least 4.5V is required). For example, if $V_{DD} = +5$V, $V_{SS} = 0$, and $V_{EE} = -13.5$V, analog signals from -13.5V to $+4.5$V can be controlled by digital inputs of 0 to 4.5V. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt. No V_{DD} current will flow through R_L if the switch current flows into lead 3 on the MMC 4051; leads 3 and 13 on the MMC 4052; leads 4, 14, 15 on the MMC 4053.

LIQUID-CRYSTAL DISPLAY DRIVERS

4054 - 4 SEGMENT DISPLAY DRIVER-STROBED LATCH FUNCTION
4055 - BCD TO 7-SEGMENT DECODER/ DRIVER, WITH „DISPLAY-FREQUENCY" OUTPUT
4056 - BCD TO 7-SEGMENT DECODER/ DRIVER WITH STROBED LATCH FUNCTION

GENERAL DESCRIPTION

The MMC 4054, MMC 4055, MMC 4056 (G, H types extended temperature range and the E, F types intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package. The MMC 4055 and MMC 4056 types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signals swings (V_{DD} to V_{SS}) may be as low as 0 to −3V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be from 0 to −5V. If V_{DD} to V_{EE} exceeds 15V, V_{DD} to V_{SS} should be at least 4V. The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays).

When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well bellow the upper limit of the liquid crystal frequency response). The MMC 4055 provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The MMC 4056 provides a strobed latchfunction at the BCD inputs. Decoding of all input combinations on the MMC 4055 and MMC 4056 provides displays of 0 to 9 as well as L,P,H,A — and a blank position. The MMC 4054 provides level shifting similar to the MMC 4055 and MMC 4056 independently strobed latches, and common DF control on 4 signal lines. The MMC 4054 is intended to provide drive-signal compatibility with the MMC 4055 and MMC 4056 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any MMC 4054 output line by connecting the corresponding input and strobe lines to a low and high level, respectively. The MMC 4054 may also be utilized for logic-level „up conversion" or „down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to −5V. The level shifted function on all three types permits the use of different input-and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus, the input and output swings can be selected independently of each other over a 3-to 18V range. V_{SS} may be connected to V_{EE} when no level-shift function is required. For the MMC 4054 and the MMC 4056, data are transfered from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low. Whenever the level-shifting function is required, the MMC 4055 can be used by itself to drive a liquid-crystal display. The MMC 4056, however, must be used together with a MMC 4054 to provide the common DF output.

FEATURES

- Operation of liquid crystals with CMOS circuits provides ultra low-power displays
- Equivalent AC output drive for liquid-cristal displays-no external capacitor required
- Voltage doubling across display (V_{DD} — V_{EE}) = 18V results in effective 36 V (pp) drive across selected display segments
- Low-or high-output level DC drive for other types of displays
- On chip logic-level conversion for different input and output-level swings
- Full decoding of all input combinations: "0-9,L,H,P, A" and blank positions
- Input current of 100 nA at 18V and 25°C for MMC device G, H types
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

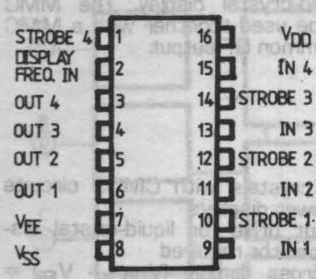
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

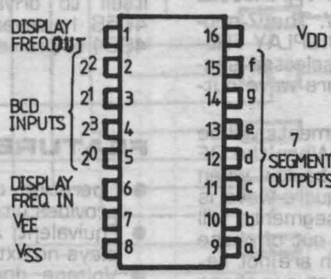
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

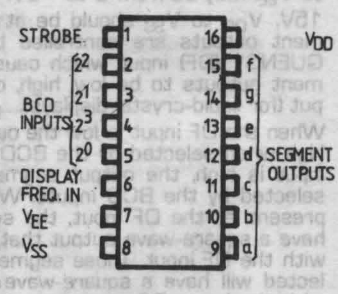
MMC 4054



MMC 4055

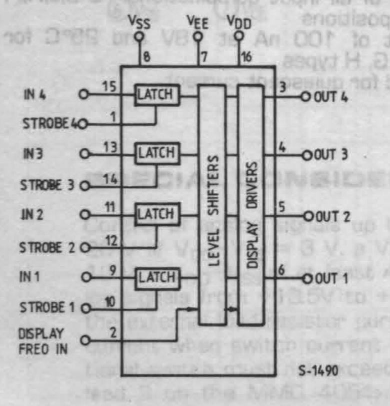


MMC 4056

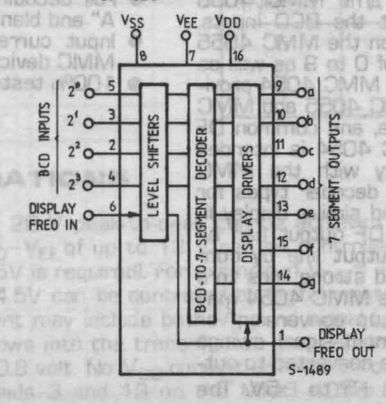


FUNCTIONAL DIAGRAMS

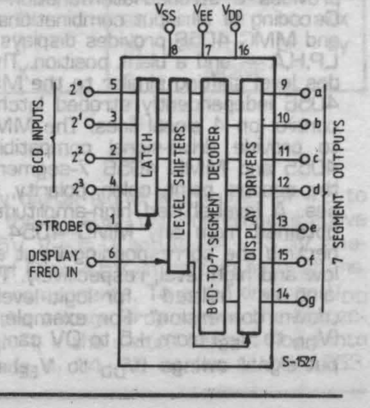
For 4054



For 4055



For 4056

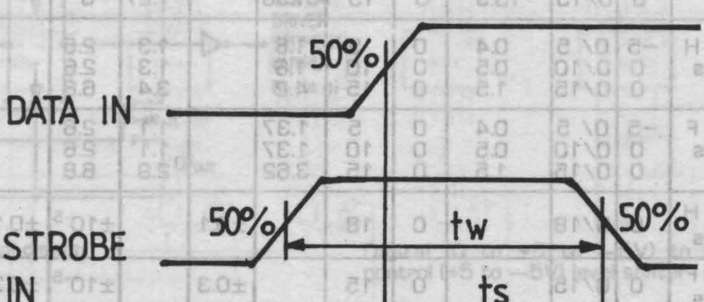


TRUTH TABLE

For 4055 and 4056

INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2^3	2^2	2^1	2^0	a	b	c*	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9
1	0	1	0	0	0	0	1	1	1	0	L
1	0	1	1	0	1	1	0	1	1	1	H
1	1	0	0	1	1	0	0	1	1	1	P
1	1	0	1	1	1	1	0	1	1	1	A
1	1	1	0	0	0	0	0	0	0	1	-
1	1	1	1	0	0	0	0	0	0	0	BLANK

Data setup time and strobe pulse duration



STATIC ELECTRICAL CHARACTERISTICS

(under recommended operating conditions)

PARAMETER		TEST CONDITIONS V_{EE} (V)	V_I (V)	V_O (V)	V_{SS} (V)	V_{DD} (V)	VALUES T^*_{LOW} Min.	T^*_{LOW} Max.	25°C Min.	25°C Typ.	25°C Max.	T^*_{HIGH} Min.	T^*_{HIGH} Max.	UNIT
I_L Quiescent supply curent	Gand H types	−5	0/ 5		0	5		5		0.04	5		150	µA
		0	0/10		0	10		10		0.04	10		300	
		0	0/15		0	15		20		0.04	20		600	
		0	0/20		0	20		100		0.08	100		3000	
	Eand F types	−5	0/ 5		0	5		20		0.04	20		150	
		0	0/10		0	10		40		0.04	40		300	
		0	0/15		0	15		80		0.04	80		600	
V_{OH} Output high voltage		0	0/ 5		0	5	4.95		4.95			4.95		V
		0	0/10		0	10	9.95		9.95			9.95		
		0	0/15		0	15	14.95		14.95			14.95		
V_{OL} Output low voltage		0	5 /0		0	5		0.05			0.05		0.05	V
		0	10/0		0	10		0.05			0.05		0.05	
		0	15/0		0	15		0.05			0.05		0.05	
V_{IH} Input high voltage		−5		0.5/4.5	0	5	3.5		3.5			3.5		V
		0		1/9	0	10	7		7			7		
		0		1.5/13.5	0	15	11		11			11		
V_{IL} Input low voltage		5		4.5/0.5	0	5		1.5			1.5		1.5	V
		0		9/1	0	10		3			3		3	
		0		13.5/1.5	0	15		4			4		4	
I_{OH} Output high current	Gaud H types	−5	0/ 5	4.5	0	5	−0.6		−0.45	−0.9		−0.3		mA
		0	0/10	9.5	0	5	−0.6		−0.45	−0.9		−0.3		
		0	0/15	13.5	0	15	−1.9		−1.5	−3		−1.1		
	Eaud F types	−5	0/ 5	4.5	0	5	−0.47		−0.38	−0.9		−0.28		
		0	0/10	9.5	0	10	−0.47		−0.38	−0.9		−0.28		
		0	0/15	13.5	0	15	−1.58		−1.27	−3		−0.95		
I_{OL} Output low current	Gand H types	−5	0/ 5	0.4	0	5	1.6		1.3	2.6		0.9		mA
		0	0/10	0.5	0	10	1.6		1.3	2.6		0.9		
		0	0/15	1.5	0	15	4.2		3.4	6.8		2.4		
	Eand F types	−5	0/ 5	0.4	0	5	1.37		1.1	2.6		0.82		mA
		0	0/10	0.5	0	10	1.37		1.1	2.6		0.9		
		0	0/15	1.5	0	15	3.62		2.9	6.8		2.17		
I_{IH}, I_{IL} **Input leakage current	Gaud H types	0	0/18		0	18		±0.1		$\pm10^{-5}$	±0.1		±1	µA
	Eaud F types	0	0/15		0	15		±0.3		$\pm10^{-5}$	±0.3		±1	µA
C_I** Input capacitance										5	7.5			pF

* T_{LOW} = −55°C for Gaud H devices; −40°C for Eaud F devices.
* T_{HIGH} = +125°C for Gaud H devices; +85°C for Eaud F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS

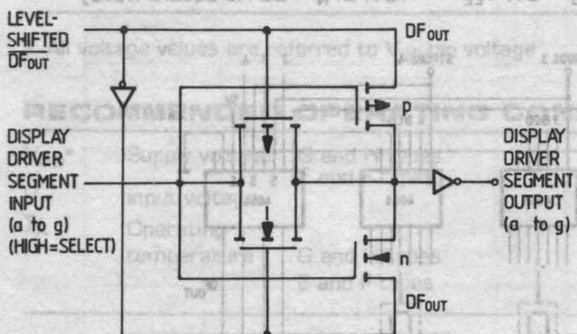
(T_{amb} = 25°C, C_L = 50 pF, R_L = 200 k typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	TYPES 4054 Min.	4054 Typ.	4054 Max.	4055 and 4056 Min.	4055 and 4056 Typ.	4055 and 4056 Max.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time (Any time to Any output)	−5	0	5		400	800		650	1300	ns
		0	0	10		340	680		575	1150	
		0	0	15		250	500		375	750	
t_{THL}, t_{TLH}	Transition time (Any output)	−5	0	5		100	200		100	200	ns
		0	0	10		100	200		100	200	
		0	0	15		75	150		75	150	
$t_{Set\ up}$*	Data setup time	−5	0	5	220	110		220	110		ns
		0	0	10	100	50		100	50		
		0	0	15	70	35		70	35		
t_W*	Strobe pulse width	−5	0	5	220	110		220	110		ns
		0	0	10	100	50		100	50		
		0	0	15	70	35		70	35		

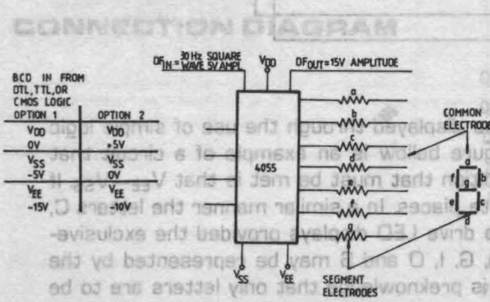
* MMC 4055 and 4056 only

TYPICAL APPLICATIONS

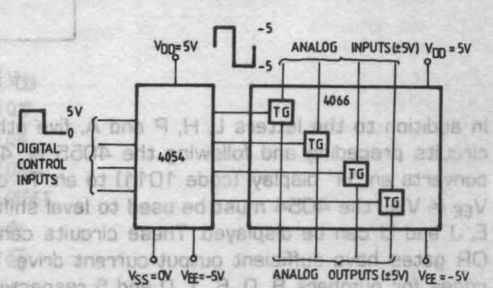
Display-driver circuit for one segment line



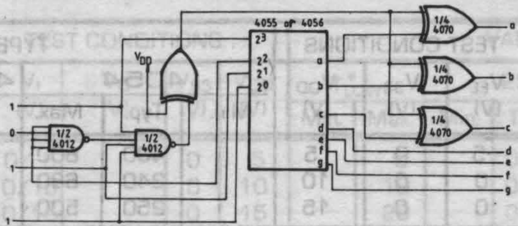
Single-digit liquid crystal display



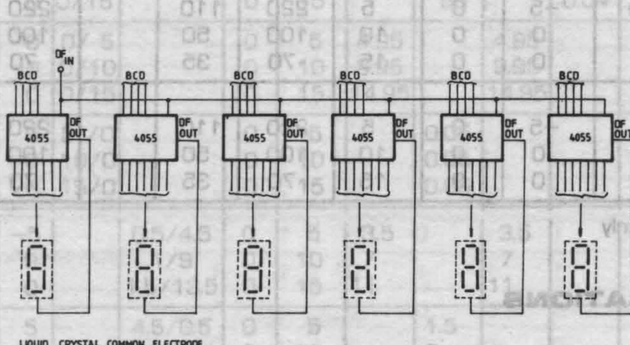
Digital (0 to +5 to −5V) to bidirectional analog control (+5 to −5V) level shifter



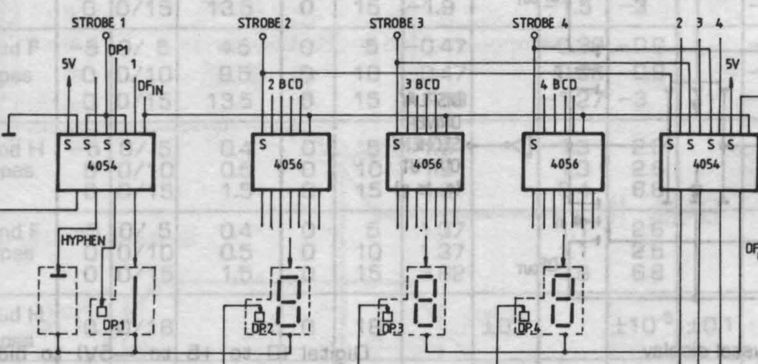
Conversion of "H" display to "F" display



Clock display



Typical 3 1/2-digit liquid crystal display: (V_{DD} = +5V, V_{SS} = 0V, V_{EE} = —10V, DF_N = 30 Hz square wave)



* In addition to the letters L, H, P and A, five other letters can be displayed through the use of simple logic circuits preceding and following the 4055 or 4056 devices. Figure bellow is an example of a circuit that converts an "H" display, (code 1011) to an "F" display.. One condition that must be met is that V_{EE}—V_{SS}. If $V_{EE} \neq V_{SS}$, the 4054 must be used to level shift in the appropiate places. In a similar manner the letters C, E, J and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive. The letters B, D, G, I, O and S may be represented by the codes for numbers 8, 0, 6, 1, 0 and 5 respectively, when there is preknowledge that only letters are to be displayed.

14-STAGE RIPPLE-CARRY BINARY COUNTER/ DIVIDER AND OSCILLATOR

GENERAL DESCRIPTION

The MMC 4060 is a monolithic i.c. processed in standard Al-gate CMOS technology. This device consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\emptyset_I$ (and Øo) A high level on the RESET line resets the counter to the all O's state and disables the oscillator. Schmitt trigger action on the clock line permits unlimited clock rise and fall times. All inputs and outputs are fully buffered.

FEATURES

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- Common reset

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.
* $T_{HIGH} = +125$°C for G, H devices; $+85$°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

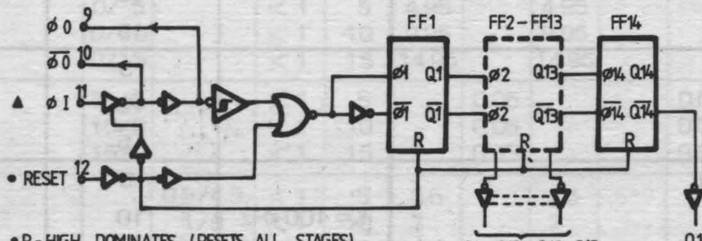
(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	Min.	Typ.	Max.	
Input-pulse operation							
t_{PLH}, t_{PHL}	Propagation delay time (Ø to Q4 Out)		5		370	740	ns
			10		150	300	
			15		100	200	
t_{PLH}, t_{PHL}	Propagation delay time (Q_n to Q_{n+1})		5		100	200	ns
			10		50	100	
			15		40	80	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Input pulse width	f = 100 kHz	5		50	100	ns
			10		20	40	
			15		15	30	
t_r, t_f	Input rise and fall time		5	Unlimited			μs
			10				
			15				
f_{max}	Maximum clock input frequency		5	3.5	7		MHz
			10	8	16		
			15	12	24		
Reset operation							
t_{PLH}	Propagation delay time		5		180	360	ns
			10		80	160	
			15		50	100	
t_W	Reset pulse width		5		60	120	ns
			10		30	60	
			15		20	40	
RC operation							
	Variation of frequency (Unit-to-Unit)	C_x = 200 pF	5	18	21.5	25	kHz
		R_S = 560 kΩ	10	20	23	26	
		R_x = 50 kΩ	15	21.1	24	27	
	Variation of frequency with voltage (Same Unit)	C_x = 200 pF	5V to 10 V	–	–	2	
		R_S = 560 kΩ					
		R_x = 50 kΩ	10 V to 15 V	–	–	1	
	R_x max	C_x = 10 μF	5	–	–	20	MΩ
		= 50 μF	10	–	–	20	
		= 10 μF	15	–	–	10	

PARAMETER	TEST CONDITIONS		VALUES			UNIT
		V_{DD}(V)	Min.	Typ.	Max.	
C_x max	$R_x = 500\ k\Omega$	5	–	–	1000	μF
	$= 300\ k\Omega$	10	–	–	50	
	$= 300\ k\Omega$	15	–	–	50	
Maximum Oscillator Frecquency*	$R_x = 5\ k\Omega$	10	530	650	810	kHz
	$C_x = 15\ pF$	15	690	800	940	

* RC oscillator applications are not recommended at supply voltages below 7 V for $R_x = 50\ k\Omega$

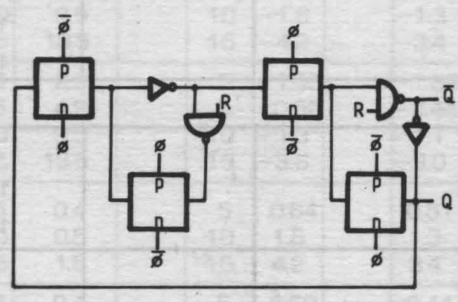
LOGIC DIAGRAM



• R = HIGH DOMINATES (RESETS ALL STAGES)

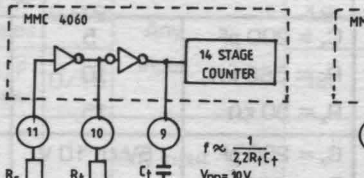
▲ COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE-GOING TRANSITION OF ø I (AND ø 0)

Detail of tipical flip-flop stage

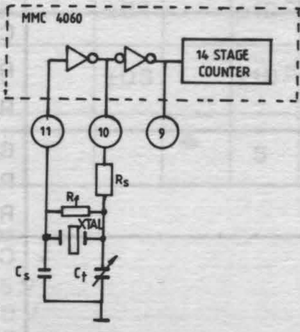


APPLICATIONS

Typical RC oscillator circuit



Typical crystal oscillator circuit



QUAD BILATERAL SWITCH FOR TRANSMISSION OR MULTIPLEXING OF ANALOG OR DIGITAL SIGNALS

GENERAL DESCRIPTION

The MMC 4066 (E, F — intermediate temperature range and G, H — extended temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.

The MMC 4066 is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with MMC 4016, but exhibits a much lower ON resistance. In addition, the ON resistance in relatively constant over the full input-signal range. The MMC 4066 consists of four independent bilateral switches. A single control signal is required per switch. Both the p and n device in a given switch are biased ON or OFF simultaneously by the control signal.

As shown in schematic diagram, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range. The advantages over single-channel switches include peak input signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range.

FEATURES

- 15 V digital or ±7.5 V peak-to-peak switching
- 80 Ω typical ON resistance for 15 V operation
- Switch ON resistance matched to within 5 Ω over 15 V signal-input range
- High on/off output-voltage ratio: 65 dB typ. at f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity: < 0.5% distortion typ. at f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD}—V_{SS} \geq$ 10 V, R_L = 10 kΩ
- Extremely low off switch leakage resulting in very low offset current and high effective OFF resistance; 10 pA typ. at $V_{DD}—V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: −50 dB typ. at f_{is} = 0.9 MHZ, R_L = 1 k
- Matched control-input to signal-output capacitance: reduces output signal transients

ABSOLUTE MAXIMUM RATINGS

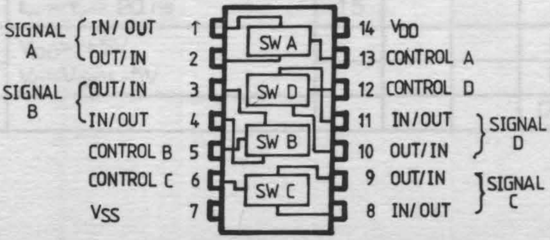
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

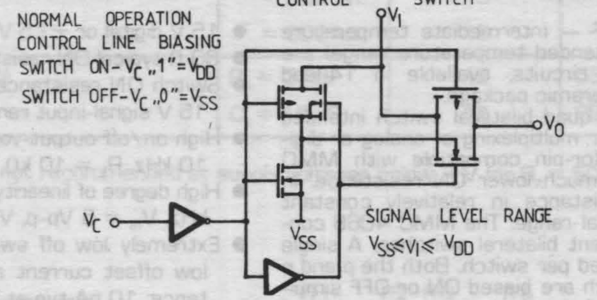
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

FUNCTIONAL DIAGRAM



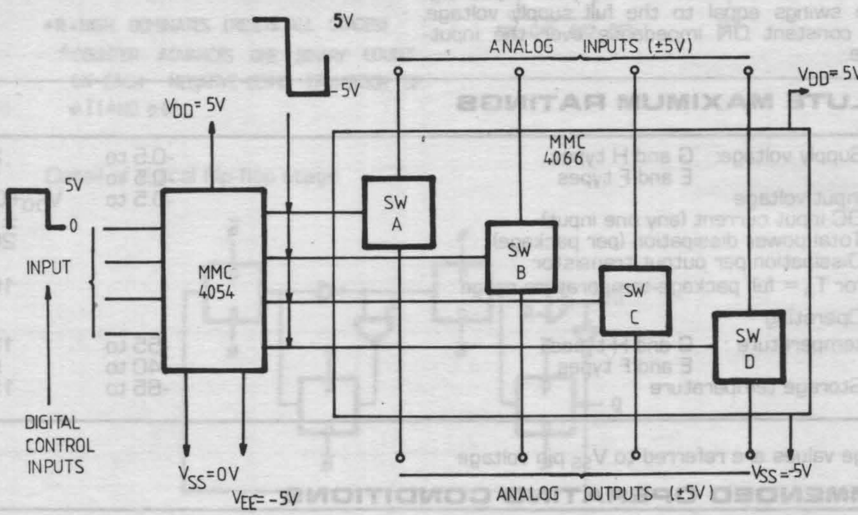
SCHEMATIC DIAGRAM

1 of 4 identical switches and its associated control circuitry



TYPICAL APPLICATIONS

Bidirectional signal transmission via digital control logic



ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, typical temperature coefficient for all V_{DD} values is 0,3% /°C)

PARAMETER			TEST CONDITIONS V_I (V)	V_{DD} (V)	T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ.	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	UNIT
I_L	Quiescent device current (All switches ON or all switches OFF)	G, H types	0/ 5	5		0.25		0.01	0.25		7.5	μA
			0/10	10		0.5		0.01	0.5		15	
			0/15	15		1		0.01	1		30	
			0/20	20		5		0.02	5		150	
		E, F types	0/ 5	5		1		0.01	1		7.5	
			0/10	10		2		0.01	2		15	
			0/15	15		4		0.01	4		30	

Signal inputs (V_{is}) and Outputs (V_{os})

PARAMETER		TEST CONDITIONS	V_{DD} (V)	T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ.	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	UNIT
R_{ON} On resistance	G, H types	$V_C = VDD$ $R_L = 10\ k\Omega$ return to $\frac{V_{DD}-V_{SS}}{2}$	5		800		470	1050		1300	Ω
			10		310		180	400		550	
			15		200		125	240		320	
	E, F types	$V_{is} = V_{SS}$ to V_{DD}	5		850		470	1050		1200	
			10		330		180	400		500	
			15		210		125	240		300	
Δ_{ON} Resistance Between Any 2 switches, ΔR_{ON}		$R_L = 10k\Omega$, $V_C = V_{DD}$	5				15				Ω
			10				10				
			15				5				
TDH Total Harmonic Distorsion		$V_C=V_{DD}=5V$, $V_{SS}=-5V$, V_{is} (p–p)=5V (Sine wave centered in 0V) $R_L = 10\ k\Omega$ $f_{is} = 1$ kHz sine wave					0.4				%
-3dB Cutoff Frequency (switch on)		$V_C=V_{DD}=5V$, $V_{SS}=-5V$, V_{is} (p–p)=5V (Sine wave centered on 0V) $R_L = 1\ k\Omega$					40				MHz
-50dB Fedthrough Frequency (switch off)		$V_C=V_{DD}=5V$, V_{is} (p–p)=5V (Sine wave centered on 0V) $R_L = 1\ k\Omega$					1				MHz
-50dB Crosstalk Frequency		$V_C(A) = V_{DD} = +5V$ $V_C(B) = V_{SS} = -5V$ $V_{is}(A) = 5Vp$-p, 50Ω source $R_L = 1\ k\Omega$					8				MHz
t_{pd} Propagation delay (Signal Input to Signal output)		$R_L = 200\ k\Omega$ $V_C=V_{DD}$, V_{SS} = GND, C_L=50 pF, V_{is} = 10V (Square wave centred on 5V) t_r, = t_r = 20 ns	5				20	40			ns
			10				10	20			
			15				7	15			
C_{is} Input capacitance		V_{DD}= +5V					8				pF
C_{os} Output capacitance		$V_C=V_{SS}$= -5V					8				
C_{ios} Feedthrough							0.5				

PARAMETER		TEST CONDITIONS	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
Input/Output Leakage current switch OFF	G, H types	V_C=0V; V_{is}= 18V; V_{os}= 0V; V_{is} = 0V; V_{os}= 18V	18		±0.1		$\pm10^{-3}$	±0.1		±1	μA
	E, F types	V_C=0V; V_{is}= 15V; V_{os}= 0V; V_{is} = 0V; V_{os}= 15V	15		±0.3		$\pm10^{-3}$	±0.3		±1	μA
Control (V_C)											
V_{ILC} Control input Low voltage		$\lvert I_{is}\rvert < 10\ \mu$A; $V_{is} = V_{SS}$, $V_{os} = V_{DD}$ and $V_{is} = V_{DD}$, $V_{os} = V_{SS}$	5		1			1		1	V
			10		2			2		2	V
			15		2			2		2	V
V_{IHC} Control input High voltage			5	3.5		3.5			3.5		V
			10	7		7			7		V
			15	11		11			11		V
I_{IH}, I_{IL} Input leakage current	G, H types	$V_{is} \leq V_{DD}$; $V_{DD} - V_{SS} = 18$ V	18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
	E, F types	$V_{DD} - V_{SS} = 15$ V; $V_{CC} \leq V_{DD} - V_{SS}$	15		±0.3		$\pm10^{-5}$	±0.3		±1	μA
Crosstalk (control input to signal output)		$V_C = 10$ V (Sq. wave); t_r, $t_f = 20$ ns; $R_L = 10$ kΩ	10				50				mW
Turn-On propagation delay		$V_{IN} = V_{DD}$, t_r, $t_f = 20$ ns; $C_L = 50$ pF, $R_L = 1$ kΩ	5				35	70			ns
			10				20	40			ns
			15				15	30			ns
Control input Repetition rate		$V_{is} = V_{DD}$, V_{SS}=GND; $R_L = 1$ kΩ to gnd; $C_L = 50$ pf; $V_C = 10$ V (Square wave centered on 5 V); t_r, $t_f = 20$ ns; $V_{os} = {}^1/_2 V_{os}$ O 1 KHZ	5				6				MHz
			10				9				MHz
			15				9.5				MHz
C_I Input capacitance		Any input					5	7.5			pF

* T_{LOW} = - 55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

ANALOG MULTIPLEXERS/DEMULTIPLEXERS: MMC 4067: SINGLE 16-CHANNEL MMC 4097: DIFFERENTIAL 8-CHANNEL

GENERAL DESCRIPTION

The MMC 4067, MMC 4097 are monolithic integrated circuits, available in 24-lead dual-in-line plastic package.

The MMC 4067, MMC 4097 analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The MMC 4067 is a 16-channel multiplexer with four binary control inputs A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The MMC 4097 is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches. A logic „1" present at the inhibit input turns all channels off.

FEATURES

- Low on resistance: 125Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{SS} = 15$ V
- High off resistance: channel leakage of +/−10 pA (typ.) for $V_{DD}-V_{SS} = 15$ V
- Matched switch characteristics: $\Delta R_{on} = 5\Omega$ (typ). for $V_{DD}-V_{SS} = 15$ V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2. μW (typ.) for $V_{DD}-V_{SS} = 10$ V
- Binary address decoding on chip

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

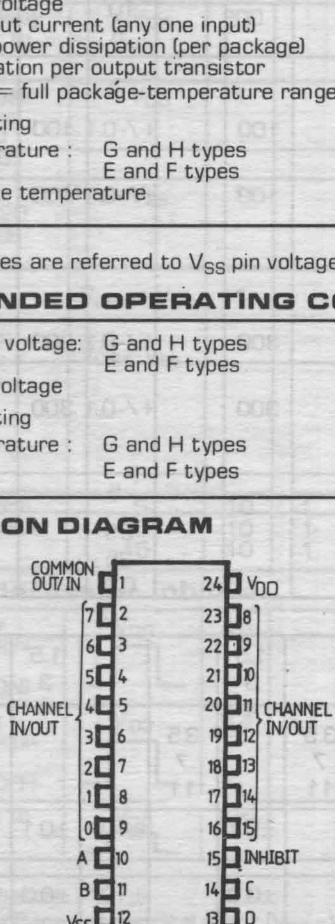
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

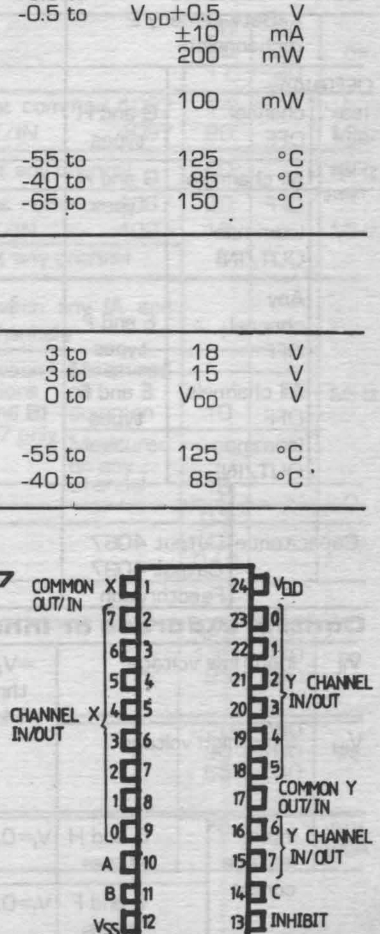
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

MMC 4067



MMC 4097



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_{LOW}(●) min.	T_{LOW}(●) max.	25°C min.	25°C typ	25°C max.	T_{HIGH}(●) min.	T_{HIGH}(●) max.	
I_L Quiescent device current	G and H types				5		5		0.04	5		150	µA
					10		10		0.04	10		300	
					15		20		0.04	20		600	
					20		100		0.08	100		3000	
	E and F types				5		20		0.04	20		150	
					10		40		0.04	40		300	
					15		80		0.04	80		600	
Switch													
ON Resistance	G and H types	$0 \leq V_I \leq V_{DD}$	0	0	5		800		470	1050		1300	Ω
					10		310		180	400		580	
					15		200		125	240		320	
	E and F types	$0 \leq V_I \leq V_{DD}$	0	0	5		850		470	1050		1200	
					10		330		180	400		520	
					15		210		125	240		300	
ΔON Resistance (Between any 2 channels)			0	0	5				10				Ω
					10				10				
					15				5				
OFF(●) leakage current: Any channel OFF	G and H types		0	0	18		100		+/-0.1	100		1000	nA
All channels OFF (common OUT/IN)	G and H types		0	0	18		100		+/-0.1	100		1000	nA
Any channel OFF	E and F types		0	0	15		300		+/-0.1	300		1000	nA
All channels OFF (common OUT/IN)	E and F types		0	0	15		300		+/-0.1	300		1000	nA
C Capacitance	Input								5				pF
	Output 4067								55				
	Output 4097								35				
	Feedthrough			−5	5				0.2				
Control (Address or Inhibit)													
V_{IL} Input low voltage		$=V_{DD}$ thru 1 kΩ	$V_{EE}=V_{SS}$ $R_L = 1K$ to V_{SS}		5		1.5			1.5		1.5	V
			$I_{IS}<2\mu A$ (on all OFF channels)		10		3			3		3	
					15		4			4		4	
V_{IH} Input high voltage					5	3.5		3.5			3.5		
					10	7		7			7		
					15	11		11			11		
I_{IH}, I_{IL} Input leakage current	G and H types	$V_I=0/18$			18		±0.1		$\pm 10^{-3}$	±0.1		±1	µA
	E and F types	$V_I=0/15$			15		±0.3		$\pm 10^{-3}$	±0.3		±1	µA

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
CI	Input capacitance	Any address or inhibit input							5	7.5			pF

(●) Determined by minimum feasible leakage measurement for automatic testing
✲ T_{LOW} = −55°C for G and H types; −40°C for E and F types
T_{high} = +125°C for G and H types; +85°C for E and F types

DYNAMIC ELECTRICAL CHARACTERISTICS

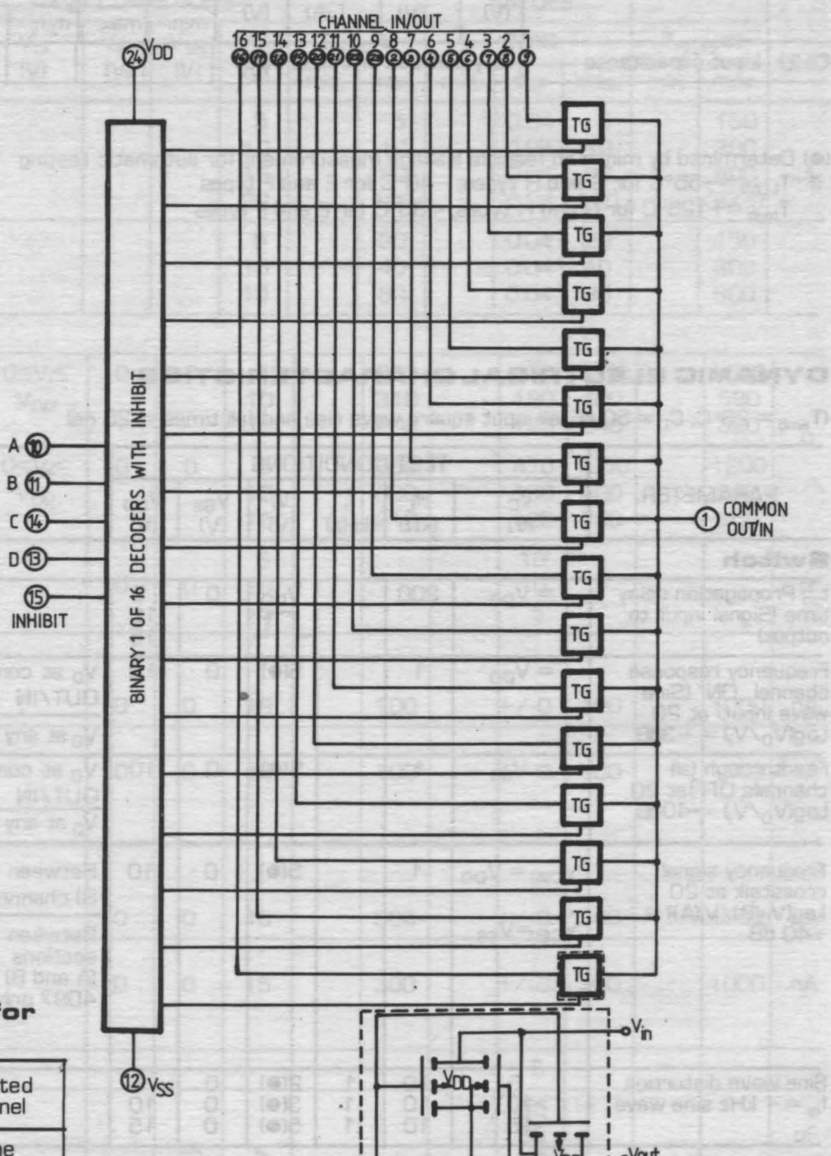
(T_{amb} = 25°C, C_L = 50 pF, all input square wave rise and fall times = 20 ns)

PARAMETER	TEST CONDITIONS V_C (V)	R_L (kΩ)	f_i (kHz)	V_i (V)	V_{SS} (V)	V_{DD} (V)		VALUES TYP.	VALUES MAX.	UNIT
Switch										
t_{pd} Propagation delay time (Signal input to output)	= V_{DD}	200		V_{DD}	0	5 10 15		30 15 11	60 30 20	ns
Frequency response channel „ON" (Sine wave input) at 20 Log(V_O/V_i) = −3dB	= V_{DD}	1		5(●)	0	10	V_O at common OUT/IN 4067 4097	14 20		MHz
							V_O at any channel	60		MHz
Feedthrough (all channels OFF) at 20 Log(V_O/V_i) = −40dB	= V_{SS}	1		5(●)	0	10	V_O at common OUT/IN 4067 4097	20 12		MHz
							V_O at any channel	8		
Frequency signal crosstalk at 20 Log(V_O(B)/V_i(A)) = −40 dB	$V_{C(A)}$ = V_{DD} $V_{C(B)}$ = V_{SS}	1		5(●)	0	10	Between any (A and B) channels	1		MHz
							Between sections (A and B) 4097 only — Measured on common	10		MHz
							Between sections (A and B) 4097 only — Measured on any channel	18		
Sine wave distortion f_{is} = 1 kHz sine wave	5 10 15	10 10 10	1 1 1	2(●) 3(●) 5(●)	0 0 0	5 10 15		0.3 0.2 0.12		%
Control (Address or inhibit)										
Propagation delay time: address or inhibit to signal OUT (channel turning ON)	V_{DD}	10			0 0 0	5 10 15		325 135 95	650 270 190	ns
Propagation delay time: address or inhibit to signal OUT (channel turning OFF)	V_{DD}	0.3			0 0 0	5 10 15		220 90 65	440 180 130	ns
Address or inhibit to signal crosstalk	V_{DD}	10✲			0	10		75		mV peak

✲ Both ends of channel
(●) peak to peak voltage symmetrical about (V_{DD}−V_{SS})/2

LOGIC DIAGRAM

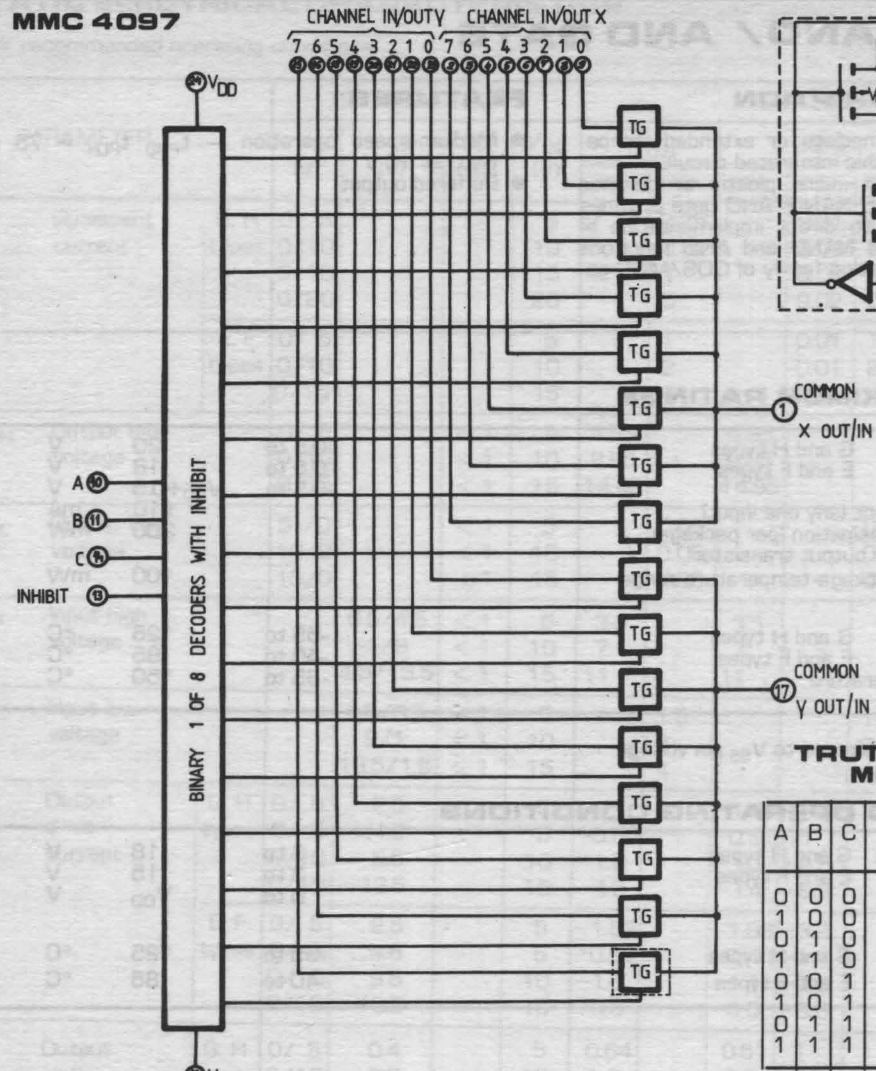
MMC 4067

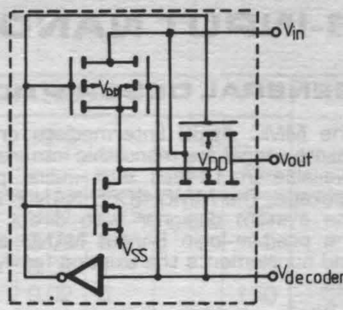


TRUTH TABLE for MMC 4067

A	B	C	D	Inh	Selected channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	1	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

MMC 4097





TRUTH TABLE for MMC 4097

A	B	C	Inh	Selected channel
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

APPLICATIONS INFORMATION

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the MMC 4067 or MMC 4097.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS}. The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at V_{DD}-V_{SS} = 10V, a 100 pF capacitor connected to the input or output of the channel will lose3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt

8-INPUT NAND / AND GATE

GENERAL DESCRIPTION

The MMC 4068 (intermediate or extended temperature range) are monolithic integrated circuit, available in 14-lead dual-in-line plastic or ceramic package. The MMC 4068 NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of COS/MOS gates.

FEATURES

- Medium-speed operation — t_{PHL}, t_{PLH} = 75 ns (typ.) at 10 V
- Buffered output

ABSOLUTE MAXIMUM RATINGS

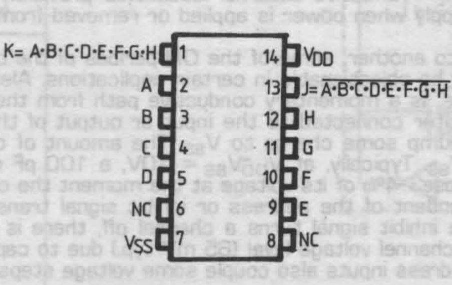
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time		5		150	300	ns
			10		75	150	
			15		55	110	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	

HEX INVERTER

GENERAL DESCRIPTION

The MMC 4069 is a monolithic integrated circuit processed in standard Al-gate CMOS technology. The MMC 4069 consists of six CMOS inverter circuits. This device is intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as MMC 4049 Hex Inverter/Buffer are not required.

FEATURES

- Medium-speed operation t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- Quiescent current specified to 20 V
- 5 V, 10 V, 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

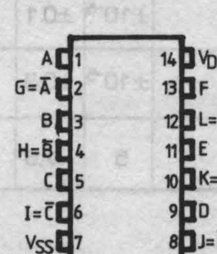
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

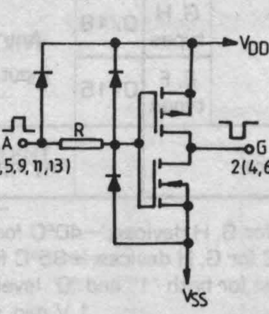
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				1.5/13.5	< 1	15	12.5		12.5			12.5		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13.5/1.5	< 1	15		2.5			2.5		2.5	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

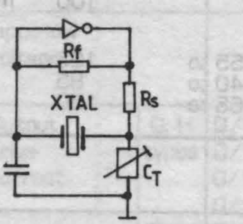
($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall times = 20 ns).

	PARAMETER	TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		55	110	ns
		10		30	60	
		15		25	50	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

APPLICATIONS

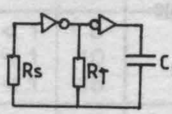
Typical crystal oscillator circuit

1/6 MMC 4069



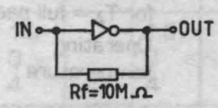
Typical RC oscillator circuit

1/3 MMC 4069

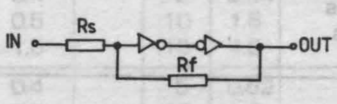


High-input impedance amplifier

1/6 MMC 4069



Input pulse shaping circuit (Schmitt trigger)



UPPER SWITCHING POINT

$$V_P = \frac{R_f + R_S}{R_f} \cdot \frac{V_{DD}}{2}$$

LOWER SWITCHING POINT

$$V_N = \frac{R_f - R_S}{R_f} \cdot \frac{V_{DD}}{2}$$

$$R_f > R_S$$

QUAD EXCLUSIVE-OR GATE 4070
QUAD EXCLUSIVE-NOR GATE 4077

GENERAL DESCRIPTION

The MMC 4070/4077 are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.
The MMC 4070 contains four independent exclusive-OR gates.
The MMC 4077 contains four independent exclusive-NOR gates.
The MMC 4070 and MMC 4077 provide the system designer with a means for direct implementation of exclusive-OR and exclusive-NOR function, respectively.

FEATURES

- Medium-speed operation $t_{PHL} = t_{PLH} = 65$ ns (TYP.) at $V_{DD} = 10$ V, $C_L = 50$ pF
- 100% tested for quiescent current

APPLICATIONS

- Logical comparators
- Adders/substractors
- Parity generators and checkers

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

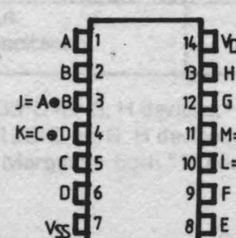
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

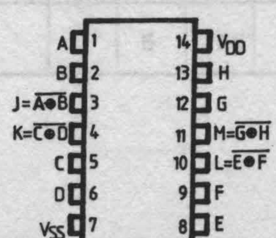
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

MMC 4070



MMC 4077



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Parameter			Test conditions: V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	Unit
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS V_{CC}(V)	VALUES MIN.	TYP.	MAX.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	5 10 15		140 65 50	280 130 100	ns
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns

TRUTH TABLE

(1 of 4 gates)

for 4070

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High level
0 = Low level
$J = A \oplus B$

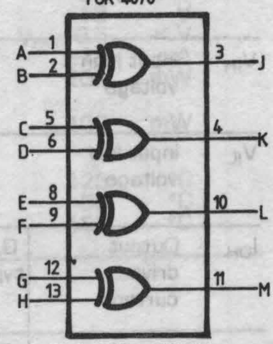
for 4077

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High level
0 = Low level
$J = \overline{A \oplus B}$

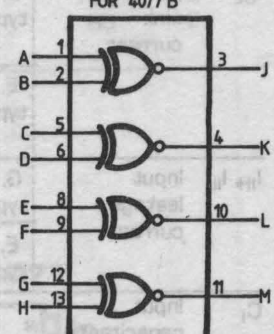
FUNCTIONAL DIAGRAM

FOR 4070



$J = A \oplus B$ $K = C \oplus D$
$L = E \oplus F$ $M = G \oplus H$
$V_{SS} = 7$ $V_{DD} = 14$

FOR 4077 B



$J = \overline{A \oplus B}$ $K = \overline{C \oplus D}$
$L = \overline{E \oplus F}$ $M = \overline{G \oplus H}$
$V_{SS} = 7$ $V_{DD} = 14$

OR Gates: QUAD 2 INPUT MMC 4071
DUAL 4 INPUT MMC 4072
TRIPLE 3 INPUT MMC 4075

GENERAL DESCRIPTION

These OR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.
The MMC 4071 MMC 4072 and MMC 4075E/F/G/H/OR gates provide the system designer with direct implementation of the OR function.
All inputs and outputs are buffered.

The MMC 4071, MMC 4072 and MMC 4075 E/F/G/H types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages.

FEATURES

- Medium-Speed Operation-t_{PLH}, t_{PLH} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

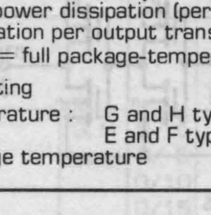
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

MMC 4071

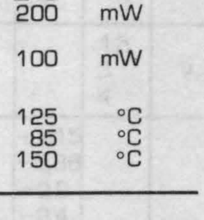


J = A + B
K = C + D
L = E + F
M = G + H

MMC 4072

J = A + B + C + D
K = E + F + G + H

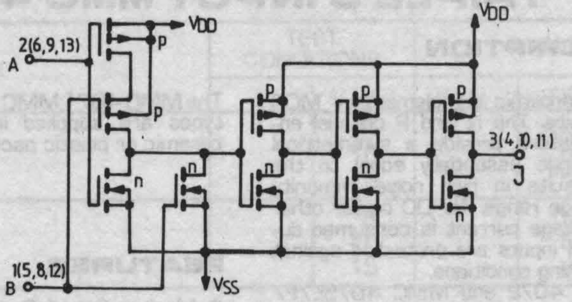
MMC 4075



J = A + B + C
K = D + E + F
L = G + H + I

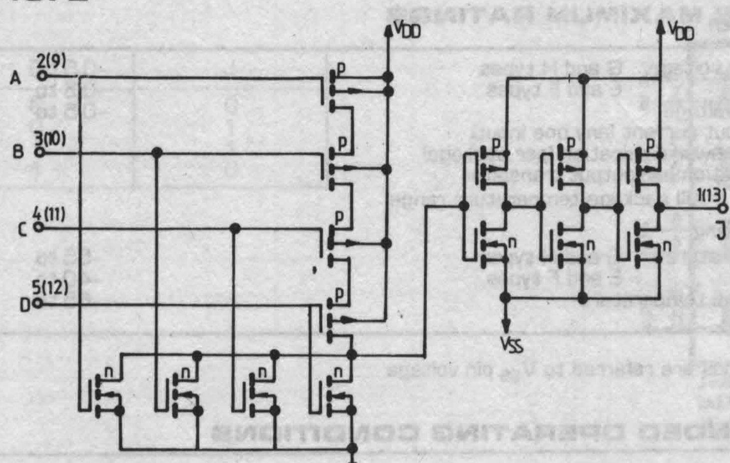
SCHEMATIC DIAGRAMS

MMC 4071

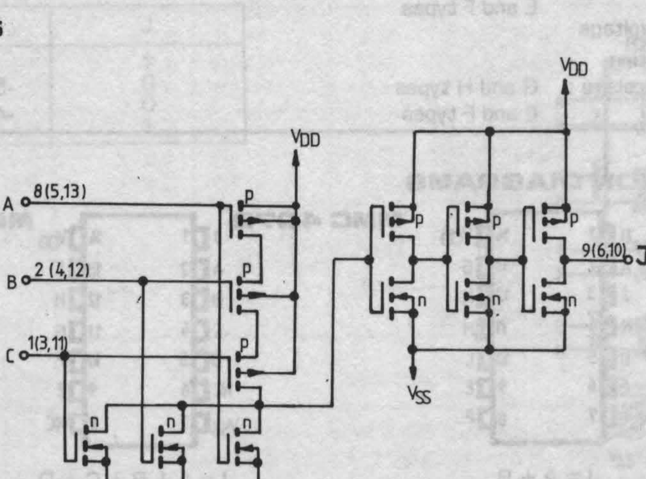


J = A + B
LOGIC 1 = HIGH
LOGIC 0 = LOW

MMC 4072



MMC 4075



1 = HIGH LEVEl
0 = LOW LEVFl

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PHL}	Propagation delay time	5		125	250	ns
		10		60	120	
		15		45	90	
t_{PLH}	Propagation delay time	5		175	350	ns
		10		70	140	
		15		50	110	
t_{THL} t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

4BIT D-TYPE REGISTERS

GENERAL DESCRIPTION

The MMC 4076 (intermediate or extended temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4076 types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disble inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

FEATURES

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs.

ABSOLUTE MAXIMUM RATINGS

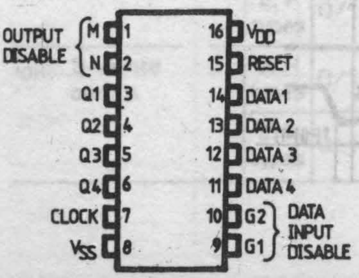
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



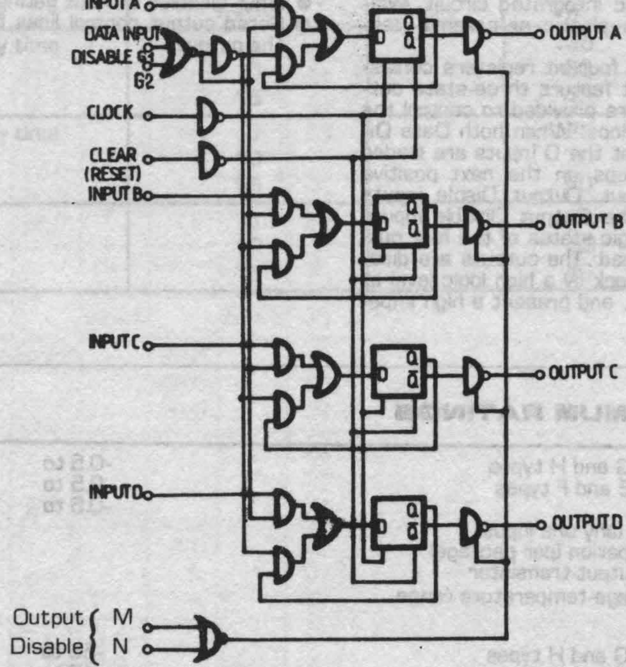
TRUTH TABLE

Reset	Clock	Data Input Disable G_1	Data Input Disable G_2	Data D	Next State Output Q	
1	x	x	x	x	0	
0	0	x	x	x	Q	NC
0	↑	1	x	x	Q	NC
0	↑	x	1	x	Q	NC
0	↑	0	0	1	1	
0	↑	0	0	0	0	
0	1	x	x	x	Q	NC
0	↓	x	x	x	Q	NC

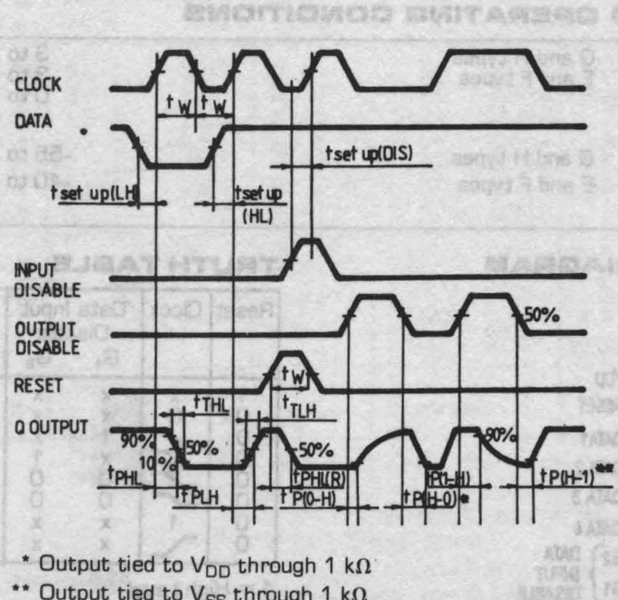
1 = High Level
0 = Low Level

X = Don't Care
NC = No Change

LOGIC DIAGRAM



WAVEFORMS



* Output tied to V_{DD} through 1 kΩ

** Output tied to V_{SS} through 1 kΩ

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm10^{-4}$	±1.0		±7.5	

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{LOW}* Min.	T_{LOW}* Max.	25°C Min.	25°C Typ	25°C Max.	T_{HIGH}* Min.	T_{HIGH}* Max.	
C_I	Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q output)		5 10 15		300 125 90	600 250 180	ns
$t_{PHL}(R)$	Propagation delay time (Reset)		5 10 15		230 100 75	460 200 150	ns
$t_{P(1-H)}$, $t_{P(0-H)}$	3-state output 1 or 0 to high impedance	$R_L = 1\ k\Omega$	5 10 15		150 75 60	300 150 120	ns
$t_{P(H-1)}$, $t_{P(H-0)}$	3-state high impedance to 1 or 0 output	$R_L = 1\ k\Omega$	5 10 15		150 75 60	300 150 120	ns
t_{TLH}, t_{THL}	Transition time		5 10 15		100 50 40	200 100 80	ns
t_w	Clock pulse width		5 10 15	200 100 80	100 50 40		ns
t_w	Reset pulse width		5 10 15	120 50 40	60 25 20		ns
t_{setup}	Data setup time		5 10 15	200 80 60	100 40 30		ns
t_{setup}	Data input disable setup time		5 10 15	180 100 70	90 50 35		ns
f_{max}	Maximum clock frequency		5 10 15	3 6 8	6 12 16		MHz
t_r, t_f	Clock input rise or fall time		5 10 15	15 5 5			μs

8-INPUT NOR/OR GATE

GENERAL DESCRIPTION

The MMC 4078 (intermediate or extended temperature range) are monolithic integrated circuits available in 14-lead dual-in-line plastic or ceramic package.

The MMC 4078 NOR/OR Gate provides the system designer with direct implementation of the positive-logic-8-input NOR and OR function and supplements the existing family of COS/MOS gates.

FEATURES

- Medium-speed operation t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

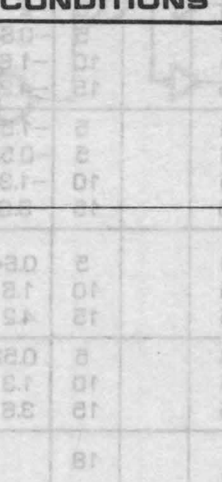
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Parameter			Test conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	Unit
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

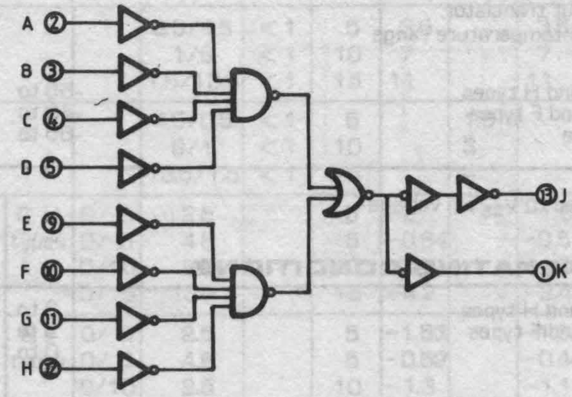
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time		5		150	300	ns
			10		75	150	
			15		55	110	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	

LOGIC DIAGRAM



CMOS AND GATES:
4081 QUAD 2 - INPUT AND GATE
4082 DUAL 4 - INPUT AND GATE
4073 TRIPLE 3 - INPUT AND GATE

GENERAL DESCRIPTION

The MMC 4081, MMC 4082 and MMC 4073, AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.
The MMC 4081, MMC 4082 and MMC 4073 types are supplied in 14 — lead dual — in — line ceramic or plastic packages.

FEATURES

- Medium speed operation t_{PLH} = 85 ns (TYP); t_{PHL} = 65 ns (TYP) at 10 V
- Quiescent current specified to 20 V

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

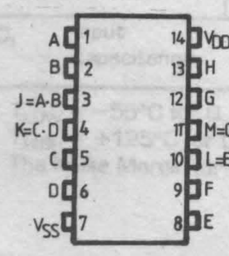
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

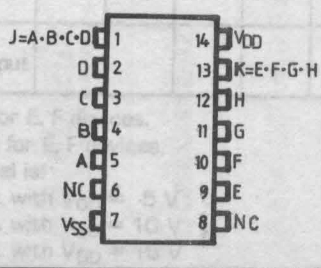
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

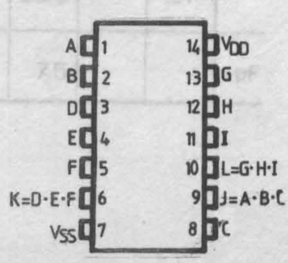
MMC 4081



MMC 4082



MMC 4073



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

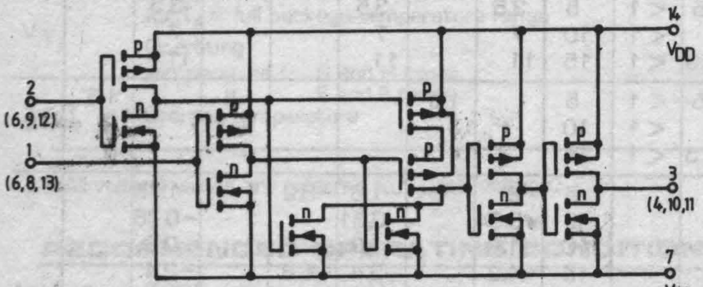
DYNAMIC ELECTRICAL CHARACTERISTICS

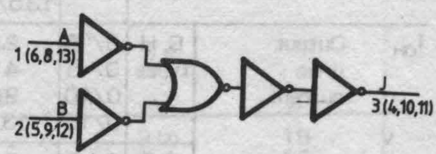
(T_{amb} = 25°C, C_L = 50 pF, R_L = 200k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min	typ	max	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	5		125	250	ns
		10		60	120	
		15		45	90	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

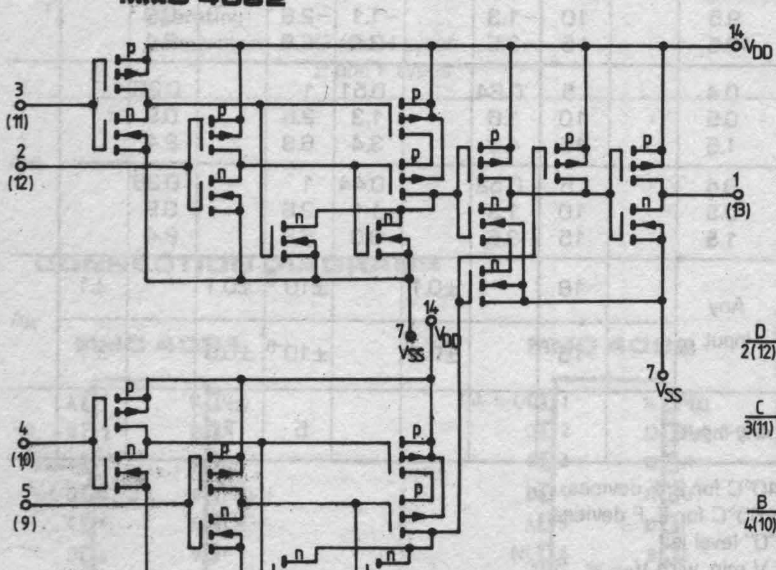
SCHEMATIC AND LOGIC DIAGRAMS

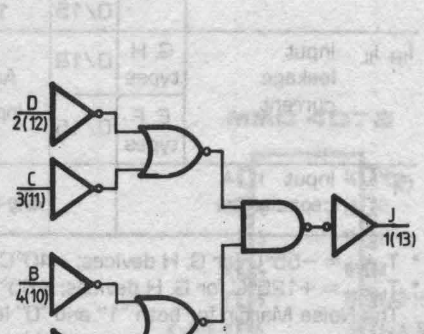
MMC 4081



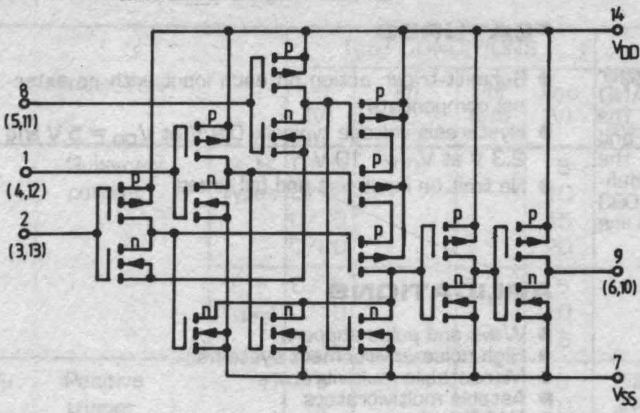


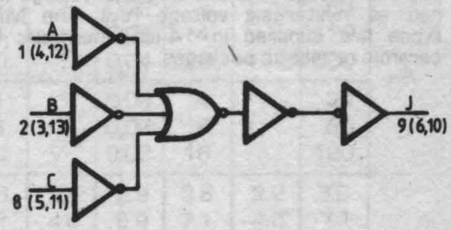
MMC 4082





MMC 4073





QUAD 2-INPUT NAND SCHMITT TRIGGERS

GENERAL DESCRIPTION

The MMC 4093 consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative going signals. The difference between the positive voltage (V_P) and negative voltage (V_N) is defined as hysteresis voltage (V_H). The MMC 4093 types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages.

FEATURES

- Schmitt-triger action on each input with no external components
- Hysteresis voltage typically 0.9 V at V_{DD} = 5 V and 2.3 V at V_{DD} = 10 V
- No limit on input rise and fall times

APLICATIONS

- Wave and pulse shapers
- High-noise-environment systems
- Monostabile multivibrators
- Astable multivibrators
- NAND logic

ABSOLUTE MAXIMUM RATINGS

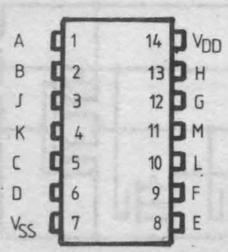
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



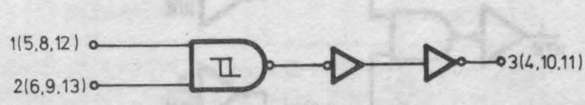
$J = \overline{A \cdot B}$

$K = \overline{C \cdot D}$

$L = \overline{E \cdot F}$

$M = \overline{G \cdot H}$

FUNCTIONAL DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_P	Positive trigger threshold voltage		a			5	2.2	3.6	2.2	2.9	3.6	2.2	3.6	V
			a			10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
			a			15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
			b			5	2.6	4	2.6	3.3	4	2.6	4	
			b			10	5.6	8.2	5.6	7	8.2	5.6	8.2	
			b			15	6.3	12.7	6.3	9.4	12.7	6.3	12.7	
V_N	Negative trigger threshold voltage		a			5	0.9	2.8	0.9	1.9	2.8	0.9	2.8	V
			a			10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
			a			15	4	7.4	4	5.8	7.4	4	7.4	
			b			5	1.4	3.2	1.4	2.3	3.2	1.4	3.2	
			b			10	3.4	6.6	3.4	5.1	6.6	3.4	6.6	
			b			15	4.8	9.6	4.8	7.3	9.6	4.8	9.6	
V_H	Hysteresis voltage		a			5	0.3	1.6	0.3	0.9	1.6	0.3	1.6	V
			a			10	1.2	3.4	1.2	2.3	3.4	1.2	3.4	
			a			15	1.6	5	1.6	3.5	5	1.6	5	
			b			5	0.3	1.6	0.3	0.9	1.6	0.3	1.6	
			b			10	1.2	3.4	1.2	2.3	3.4	1.2	3.4	
			b			15	1.6	5	1.6	3.5	5	1.6	5	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		

a: input on terminals 1, 5, 8, 12 or 2, 6, 9, 13; other inputs to V_{DD}.
b: input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	V
			15/0		<1	15		0.05			0.05		0.05	V
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		mA
			0/15	1.5		15	4.2		3.4	6.8		2.4		mA
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		mA
			0/10	0.5		10	1.3		1.1	2.6		0.9		mA
			0/15	1.5		15	3.6		3.0	6.8		2.4		mA
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

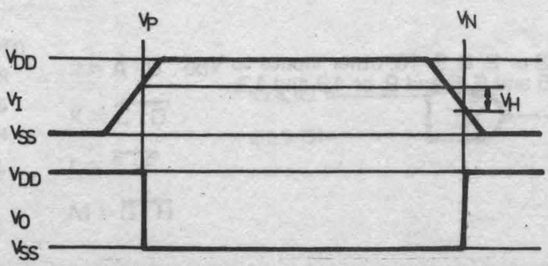
* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

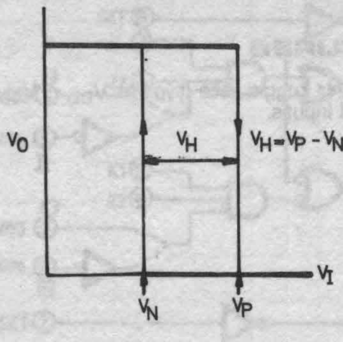
($T_A = 25°C$; input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kohm)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	5		190	380	ns
		10		90	180	ns
		15		65	90	ns
t_{THL}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	ns
		15		40	80	ns

Fig. 1` Hysteresis definition, characteristic and test setup
(a) Definition of V_P, V_N and V_H



(b) Transfer characteristic of 1 of 4 gates



(c) Test setup

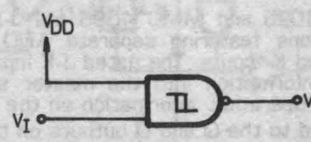
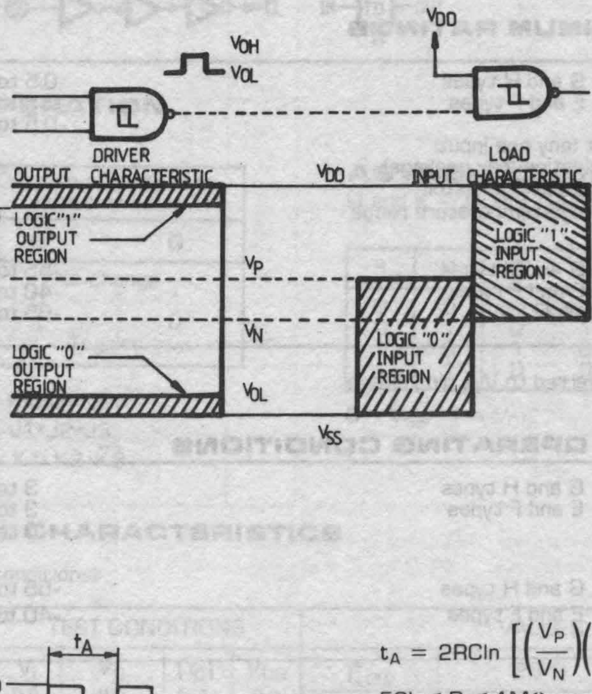
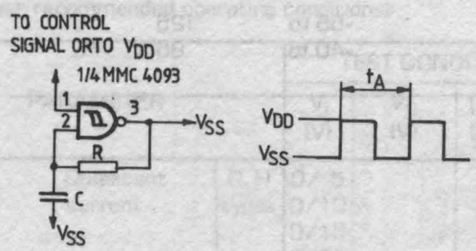


Fig. 2 Input and output characteristics



APPLICATION

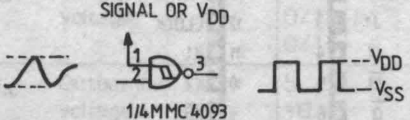
Astable multivibrator



$$t_A = 2RC\ln\left[\left(\frac{V_P}{V_N}\right)\left(\frac{V_{DD}-V_N}{V_{DD}-V_P}\right)\right]$$

$50k \le R \le 1M\Omega$
$100pF \le C \le 1\mu F$
For the range of R and C given $2\mu s < t_A < 0{,}4s$

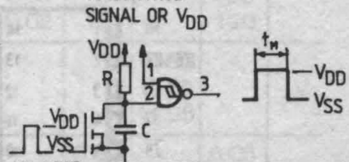
Wave shaper
Frequency range of wave shaperis from DC to 1MHz



$$t_M = RC\ln\frac{V_{DD}}{V_{DD}-V_P}$$

$50k \le R \le 1M\Omega$
$100pF \le C \le 1\mu F$

Monostable multivibrator



For the range of R and C given $5\mu s \le t_M \le 1s$

GATED J-K MASTER-SLAVE FLIP-FLOPS

GENERAL DESCRIPTION

The MMC 4095/4096 (intermediate or extended temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.

The MMC 4095 and MMC 4096 are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control tansfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

FEATURES

- 16 MHz toggle rate (typ.) at $V_{DD} - V_{SS} = 10$ V
- Gated inputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

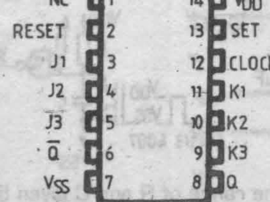
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

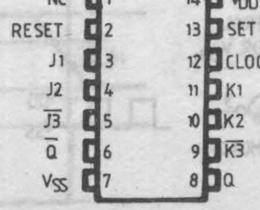
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

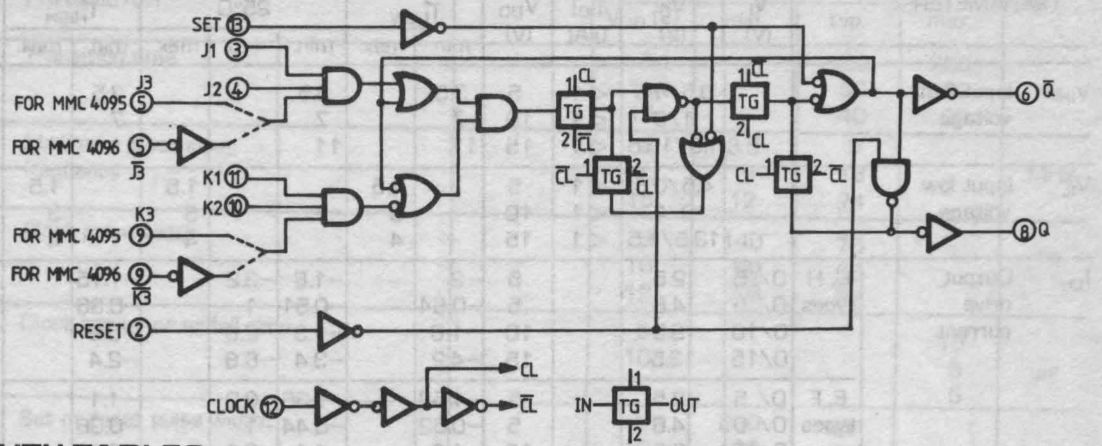
MMC 4095



MMC 4096



LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS OPERATION

(S = 0 R = 0)

Inputs before positive clock transition		Outputs after positive clock transition	
J*	K*	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For MMC 4095
$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

For MMC 4096
$J = J1 \cdot J2 \cdot \overline{J3}$
$K = K1 \cdot K2 \cdot \overline{K3}$

ASYNCHRONOUS OPERATION

(J and K — DON'T CARE)

S	R	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	0	0

$0 = V_{SS}$, $1 = V_{DD}$

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance		Any input							5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

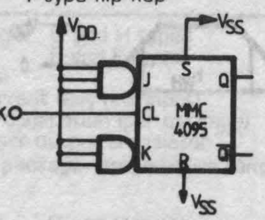
(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	5		250	500	ns
		10		100	200	
		15		75	150	
t_{PLH}, t_{PHL}	Propagation delay time (Set or reset)	5		150	300	ns
		10		75	150	
		15		50	100	

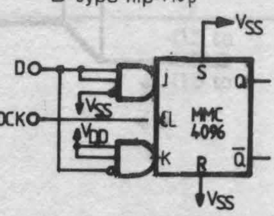
	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{CL}	Maximum clock input frequency	5 10 15	3.5 8 12	7 16 24		MHz
t_W	Clock pulse width	5 10 15	140 60 40	70 30 20		ns
t_r, t_f	Clock input rise or fall time	5 10 15			15 5 5	μs
t_W	Set or reset pulse width	5 10 15	200 100 50	100 50 25		ns
t_{setup}	Data setup time	5 10 15	400 160 100	200 80 50		ns

TYPICAL APPLICATIONS

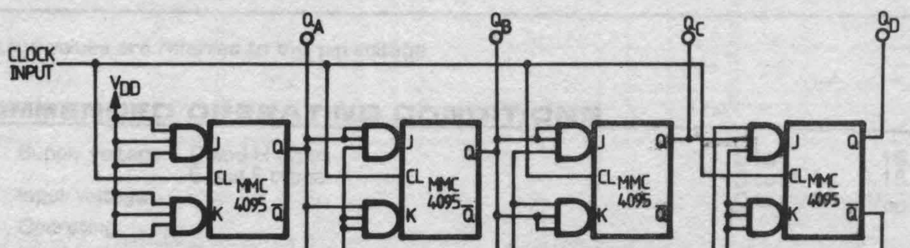
T-type flip-flop

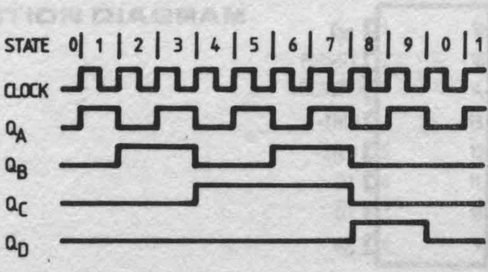


D-type flip-flop



Synchronous binary divide-by-ten counter



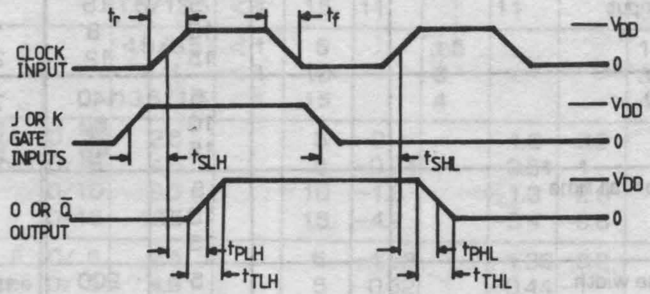


STATE	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

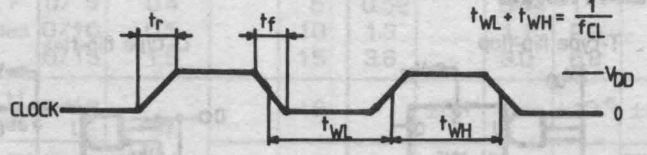
In all MMC 4095 units the Set and Reset are connected to V_{SS}

WAVEFORMS

Propagation delay, transition and setup-time



Clock pulse rise and fall time



DUAL MONOSTABLE MULTIVIBRATOR

GENERAL DESCRIPTION

The MMC 4098 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package. The MMC 4098 dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_x and C_x.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS} An unused −TR input should be tied to V_{DD}. A $\overline{RESET}$ (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the MMC 4098 is not used, its RESET should be tied to V_{SS}. See Table I. In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-triggerable mode, Q is connected to −TR when leading-edge triggering(+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used. The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01 \mu F$. Values of T vary from unit to unit and as a function of voltage, temperature, and R_x C_x. The minimum value of external resistance, R_x, is 5 kΩ. The maximum value of external capacitance, C_x, is 100 μF. The output pulse width has variations of ±2,5% typically over the temperature range of −55°C to 125°C for C_x = 1000 pF and Rx = 100 kΩ.

For power supply variations of ±5%, the output pulse width has variations of ±0,5% tipically, for V_{DD} = 10 V and 15 V and ±1% typically, for V_{DD} = 5 V at C_x = 1000 pF and R_x = 5 kΩ.

FEATURES

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of R_X,C_X
- Triggering from leading or trailing edge
- Q and $\overline{Q}$ buffered outputs available
- Separate resets
- Wide range of output-pulse widths

ABSOLUTE MAXIMUM RATINGS

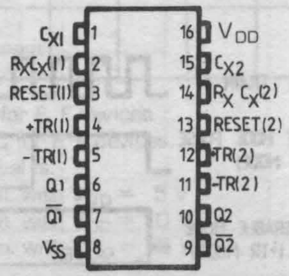
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

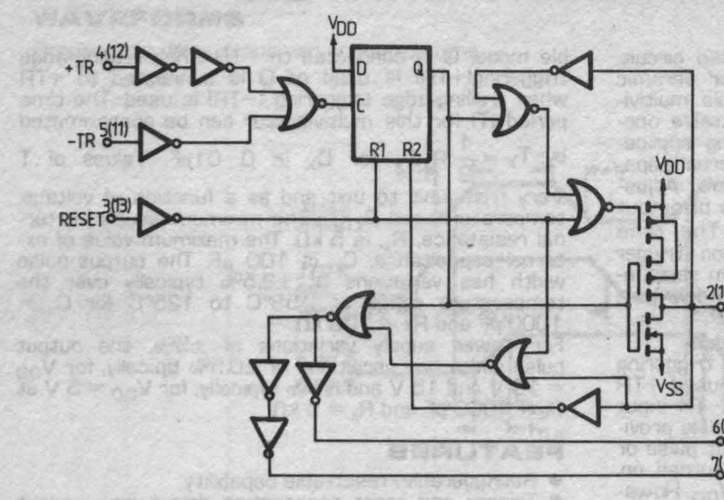
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM



FUNCTIONAL DIAGRAM

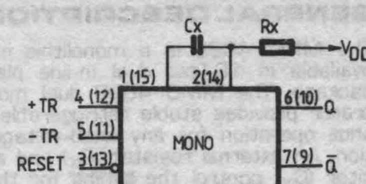


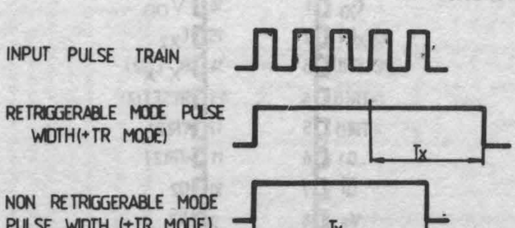
TABLE I

— Functional terminal connections

FUNCTION	TERMINAL CONNECTIONS						OTHER CON- NECTIONS	
	TO	V_{DD}	TO	V_{SS}	INPUT PULSE TO			
	Mono (1)	Mono (2)	Mono (1)	Mono (2)	Mono (1)	Mono (2)	Mono (1)	Mono (2)
Leading-Edge Trigger/Retriggerable	3,5	11,13			4	12		
Leading-Edge Trigger/Non-retriggerable	3	13			4	12	5,7	11,9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-retriggerable	3	13			5	11	4,6	12,10
Unused Section	5	11	3,4	12,13				

NOTES: 1) A Retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T_X) after application of the last trigger pulse.

2) A Non-retriggerable one-shot multivibrator has a time period T_X referenced from the application of the first trigger pulse.



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

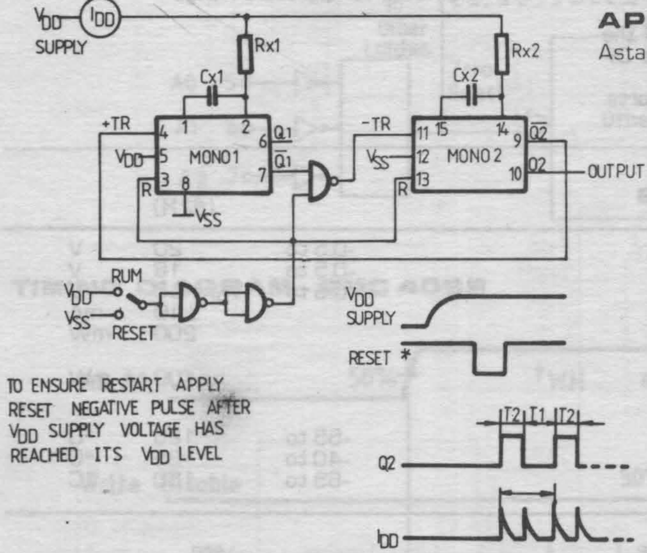
(T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS			VALUES			UNIT
		R_X (kΩ)	C_X (pF)	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Trigger propagation delay time (+TR, −TR to Q, $\overline{Q}$)	5 to 10 000	≥15	5		250	500	ns
				10		125	250	
				15		100	200	
t_{WH}, t_{WL}	Trigger pulse width	5 to 10 000	≥15	5	140	70		ns
				10	60	30		
				15	40	20		
t_{TLH}	Transition time	5 to 10 000	≥15	5		100	200	
				10		50	100	
				15		40	80	
t_{THL}	Transition time	5 to 10 000	15 to 10 000	5		100	200	
				10		50	100	
				15		40	80	ns
		5 to 10 000	0.01 µF to 0.1 µF	5		150	300	
				10		75	150	
				15		65	130	
		5 to 10 000	0.1 µF to 1 µF	5		250	500	
				10		150	300	
				15		80	160	
t_{PLH}, t_{PHL}	Propagation delay time (Reset)	5 to 10 000	≥15	5		225	450	ns
				10		125	250	
				15		75	150	
t_{WR}	Pulse width (Reset)		15	5	200	100		ns
				10	80	40		
				15	60	30		
		100	1 000	5	1 200	600		
				10	600	300		
				15	500	250		
			0.1 µF	5	50	25		µs
				10	30	15		
				15	20	10		
t_r, t_f	(TR) Rise or fall time (Trigger)			5 to 15			100	µs

PARAMETER	TEST CONDITIONS			VALUES			UNIT
	R_X (kΩ)	C_X (pF)	V_{DD} (V)	Min.	Typ.	Max.	
Pulse width match between circuits in same package	10	10 000	5		5	10	%
			10		7.5	15	
			15		7.5	15	

APPLICATIONS

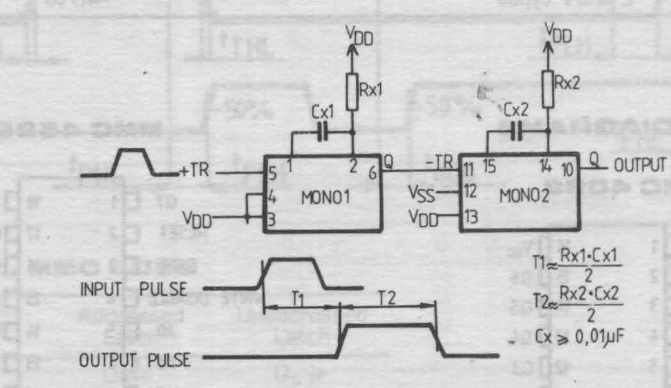
Astable multivibrator with restart after reset capability



R_X	I_{DD} (Avg)	T_X (T1+T2)	V_{DD}
10 kΩ	1 mA / 0.05 mA	3.8 μs / 0.5 s	5 V
	2.5 mA / 0.5 mA	3.2 μs / 0.5 s	10 V
10 MΩ	5 mA / 1 mA	3 μs / 0.5 s	15 V

NOTE:
ALL VALUES ARE TYPICAL
C_x RANGE: 0,0001 μF TO 0,1 μF

Pulse delay



8-BIT ADDRESSABLE LATCHES

GENERAL DESCRIPTION

The MMC 4099 and MMC 4599 are 8 bit addressable latches. Data is entered in serial form when the appropiate latch is addressed (via address pins A0, A1, A2), and write disable is in the low state.
Chip enable must be high for writing into MMC 4599. For the MMC 4599 the data pin is a bidirectional data port and for the MMC 4099 the input is a unidirectional write only port.
The Write/Read line controls this port in the MMC 4599.
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.
A Master Reset capability is available on both parts.

FEATURES

- Serial Data Input
- Parallel Output
- Low Input Capacitance` 5.0 pF typical
- Master Reset
- Noise Immunity` 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low Power TTL Loads, One Low Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

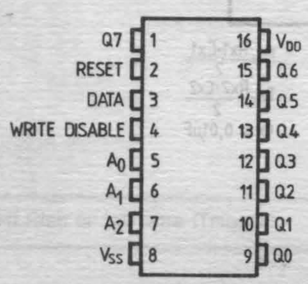
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

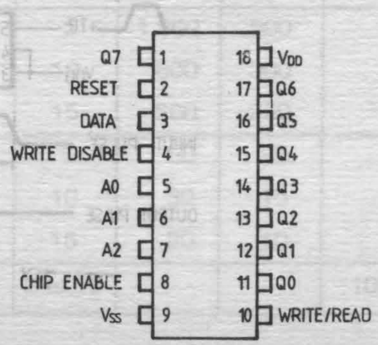
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

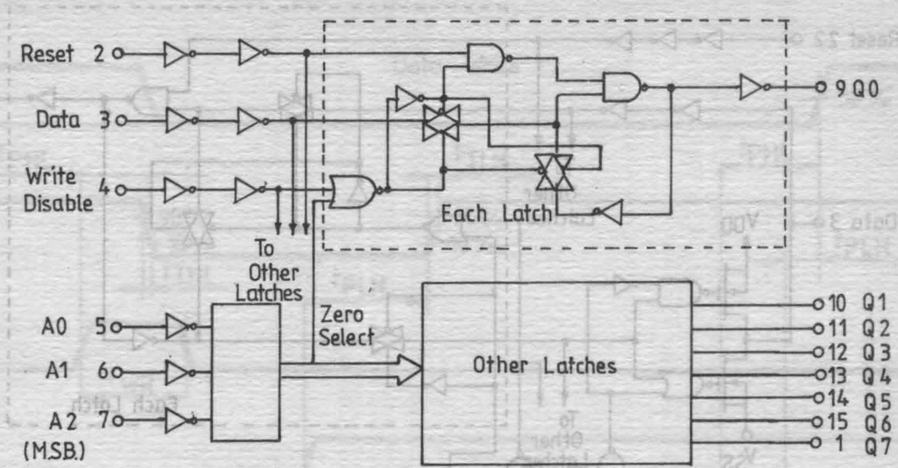
MMC 4099



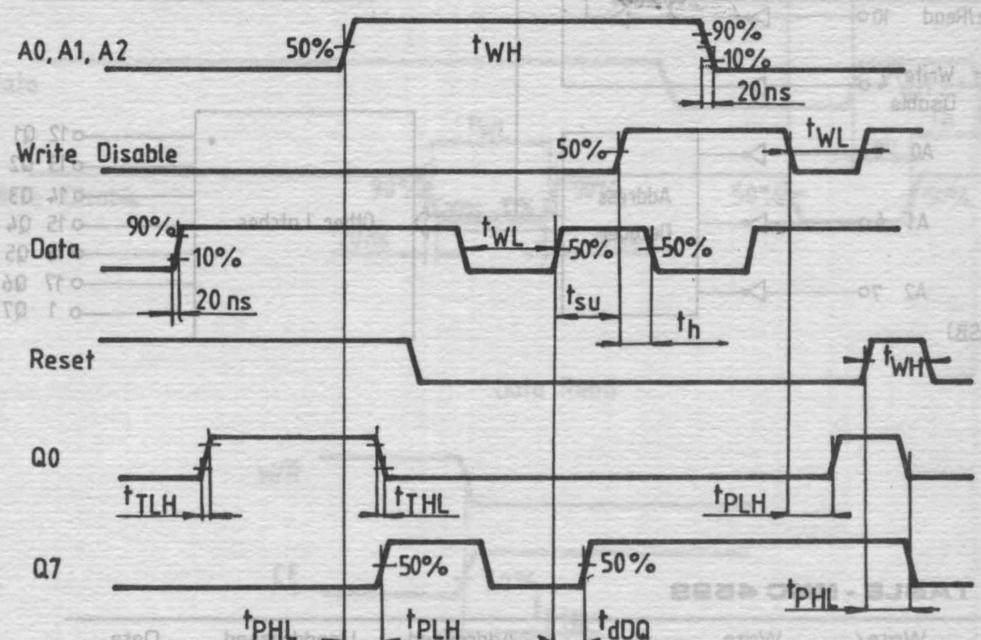
MMC 4599



FUNCTIONAL DIAGRAM - MMC 4099



TIMING DIAGRAM - MMC 4099

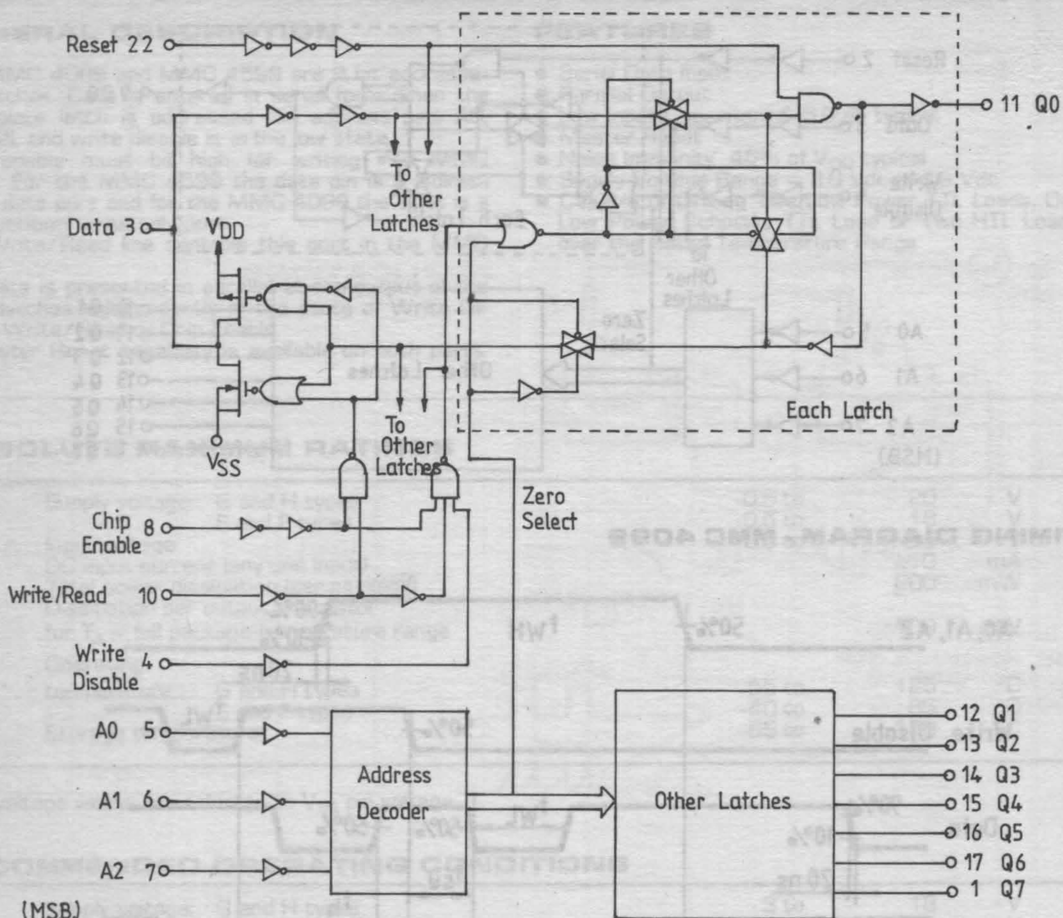


TRUTH TABLE - MMC 4099

Write Disable	Reset	Addressed Latch	Unaddressed Latch
0	0	Data	Q_n ✲
0	1	Data	Reset
1	0	Q_n ✲	Q_n ✲
1	1	Reset	Reset

✲ Q_n is previous state of latch

FUNCTIONAL DIAGRAM - MMC 4599

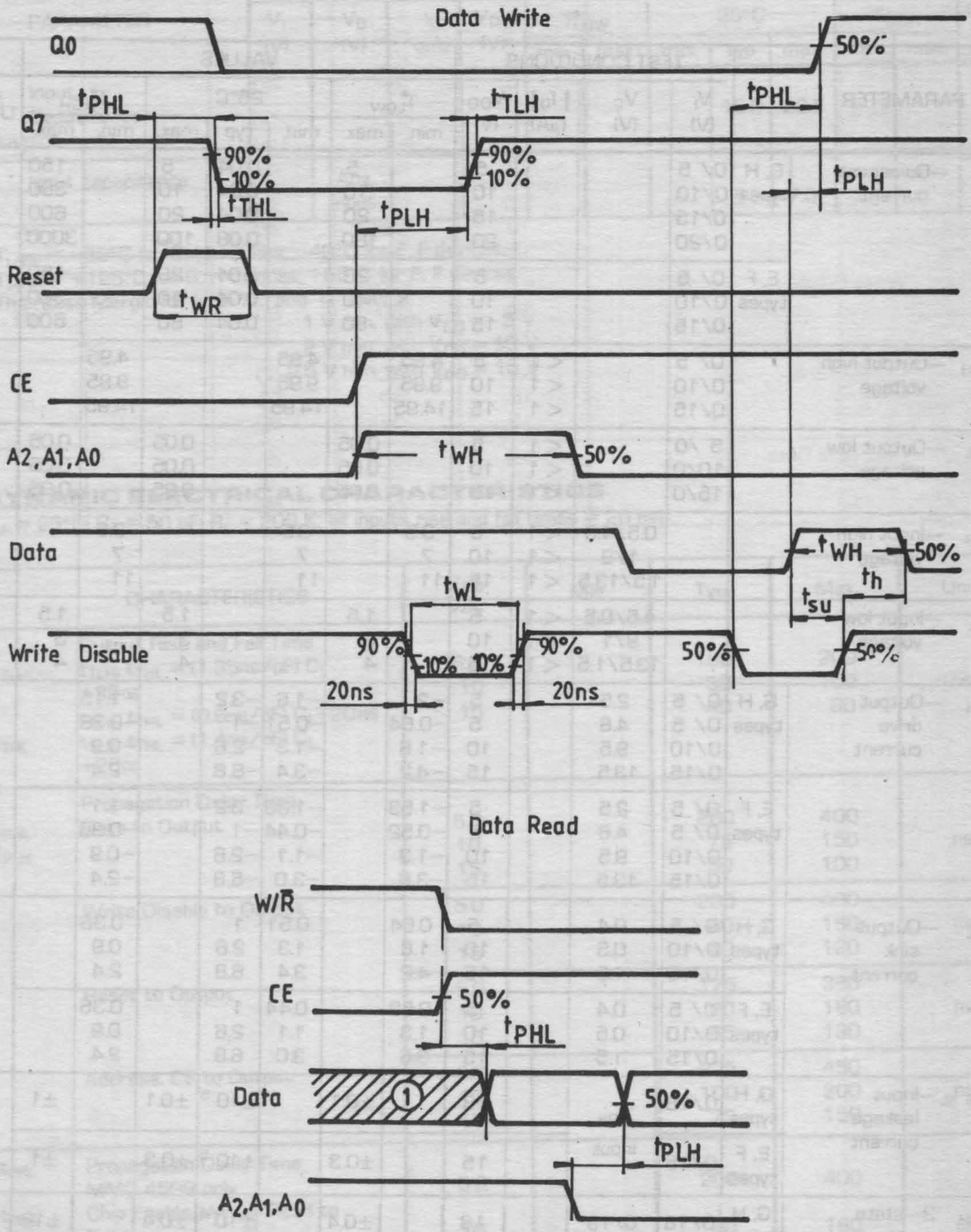


TRUTH TABLE - MMC 4599

Chip Enable	Write/ Read	Write Disable	Reset	Addressed Latch	Unaddressed Latch	Data Pin
0	X	X	0	✲	✲	Z
1	1	0	0	Data	✲	Input
1	1	1	0	✲	✲	Z
1	0	X	0	✲	✲	Q_n
X	X	X	1	0	0	Z/O

X = Don't care
✲ = No change in state of latch
Z = High impedance
Q_n = State of addressed latch

TIMING DIAGRAM - MMC4599



NOTE: 1. Invalid Data Output
2. Reset in LOW State

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
I_L —Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000	
	E, F types	0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V_{OH} —Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL} —Output low voltage		5 /0		≤ 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH} —Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL} —Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH} —Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
		0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
		0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
		0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
	E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
		0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
		0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
		0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL} —Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL} —Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
	E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH} 3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
	E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
C_{in} Input Capacitance (Data pin)								15.0	22.5			pF
C_I Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$; $C_L = 50$ pF; $R_L = 200$ K; all inputs rise and fall times = 20 ns)

	CHARACTERISTICS	V_{DD} Vdc	Min.	Typ.	Max.	Unit
t_{TLH} t_{THL}	Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35\text{ns/pF})\ C_L + 32\text{ns}$ $t_{TLH}, t_{THL} = (0.6\text{ns/pF})\ C_L + 20\text{ns}$ $t_{TLH}, t_{THL} = (1.4\text{ns/pF})\ C_L + 20\text{ns}$	5.0 10 15		100 50 40	200 100 80	ns
t_{PHL} t_{PLH}	Propagation Delay Time Data to Output	5.0 10 15		200 75 50	400 150 100	ns
	Write Disable to Output	5.0 10 15		200 80 80	400 160 120	ns
	Reset to Output	5.0 10 15		175 80 65	360 160 130	ns
	Address, CE to Output	5.0 10 15		225 100 75	450 200 150	ns
t_{PHL} t_{PLH}	Propagation Delay Time MMC 4599 only Chip Enable, Write/Read to Data	5.0 10 15		200 80 65	400 160 130	ns
	Address to Data	5.0 10 15		200 90 75	400 180 150	ns

	CHARACTERISTICS	V_{DD} Vdc	Min.	Typ.	Max.	Unit
t_{WH} t_{WL}	Minimum Pulse Widths Data	5.0 10 15	200 100 80	100 50 40		ns
	Address	5.0 10 15	400 200 125	200 100 65		ns
	Reset	5.0 10 15	150 75 50	75 40 25		ns
	Write Disable	5.0 10 15	320 160 120	160 80 60		ns
t_{su}	Set Up Time Data	5.0 10 15	100 50 35	50 25 20		ns
t_h	Hold Time Data	5.0 10 15	150 75 50	75 40 25		ns

1 BIT INDUSTRIAL CONTROL UNIT

GENERAL DESCRIPT'ON

The MMC 4500 is a single bit, one-chip static CMOS processor. The industrial Control Unit (ICU) is design for the use in systems requiring decisions based on succesive single bit information. The control program is stored in an external ROM. With a program counter, output latches and input multiplexers, the ICU in a system, forms a stored program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control.

FEATURES

- 16 instructions
- Fully static operation
- Wide range of clock frequencies, typical 1 MHz operation at V_{DD} 5 V
- Executes one instruction per clock cycle
- Capable of driving one Low-Power Schottky load or two Low-Power TTL loads
- 3 to 18 V operation
- High noise immunity
- Low quiescent current

ABSOLUTE MAXIMUM RATINGS

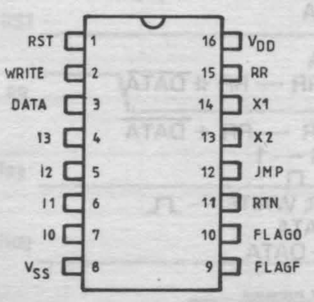
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

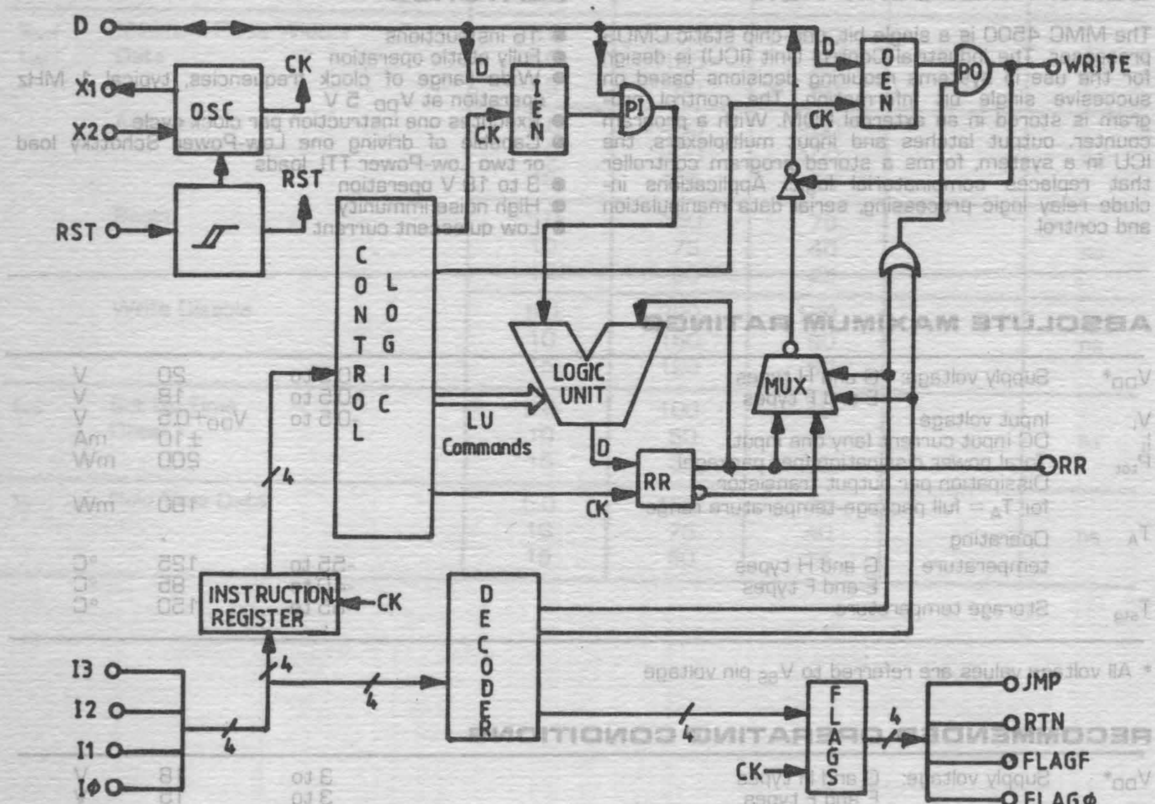
CONNECTION DIAGRAM



PIN FUNCTION

Pin No.	Function	Symbol
1	Chip Reset	RST
2	Write Pulse	WRITE
3	Data In/Out	DATA
4	MSB Instruction Word	I3
5	Bit 2 Instruction Word	I2
6	Bit 1 Instruction Word	I1
7	LSB Instruction Word	I0
8	Ground	V_{SS}
9	Flag on NOPF	FLAGF
10	Flag on NOPO	FLAGO
11	Subroutine Return	
	Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V_{DD}

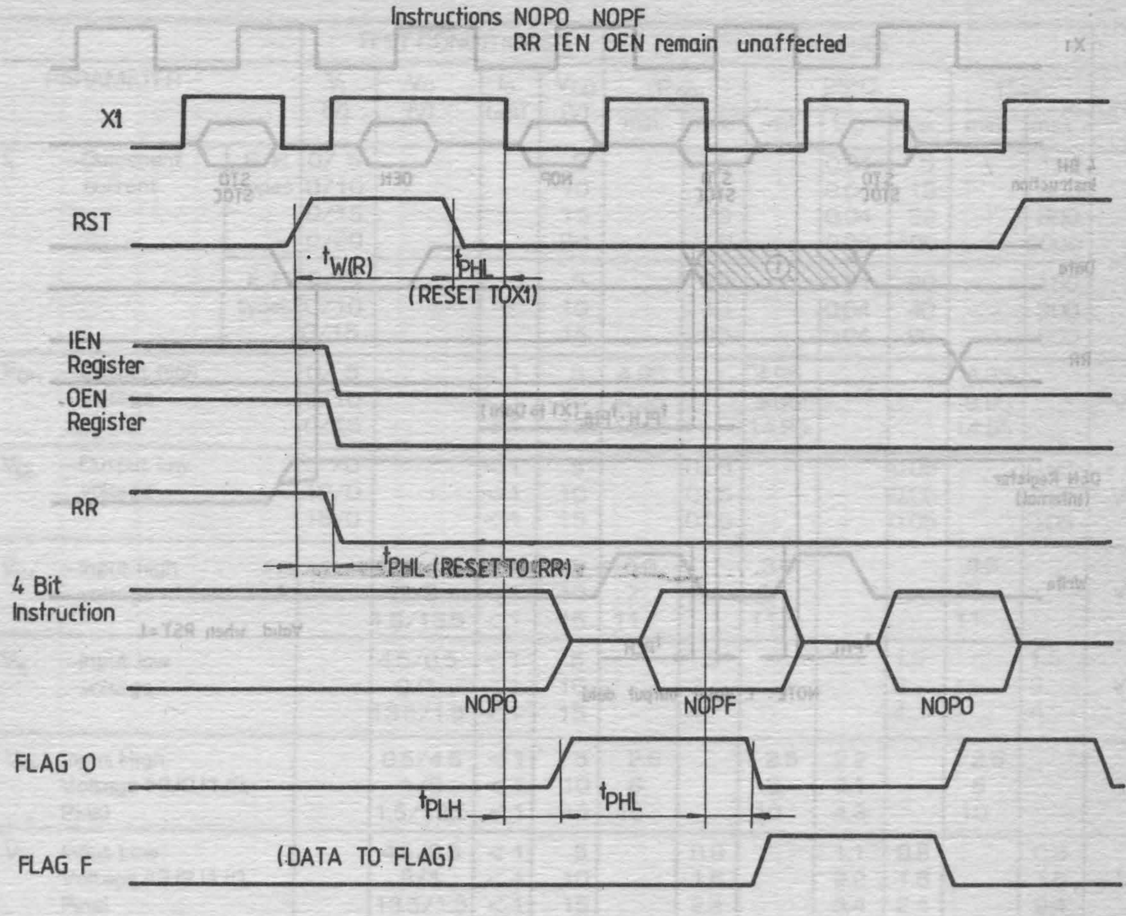
BLOCK DIAGRAM

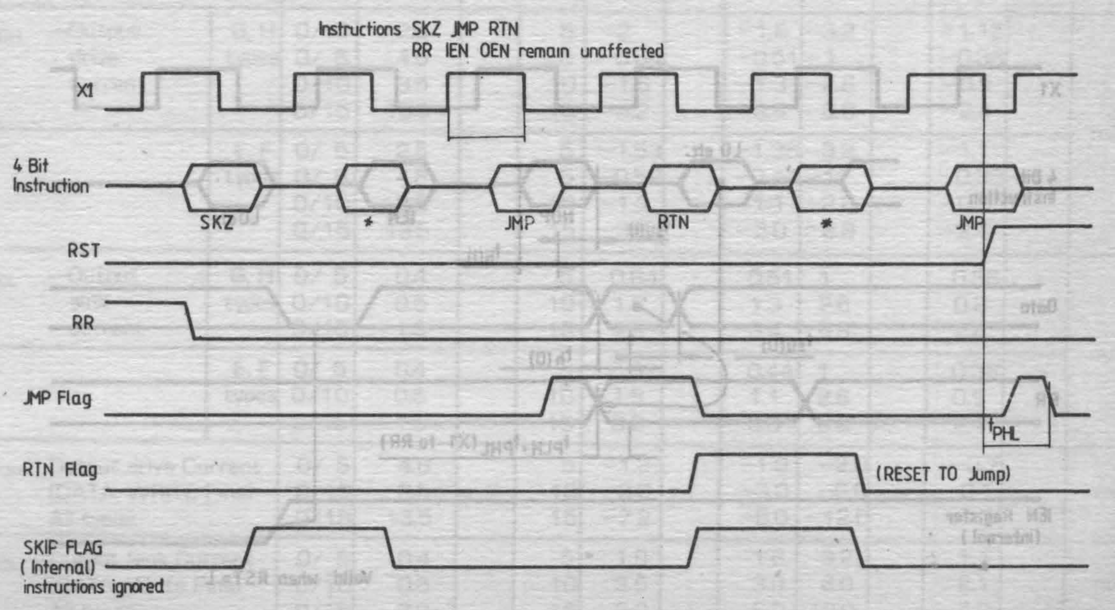


MMC 4500 - INSTRUCTION SET

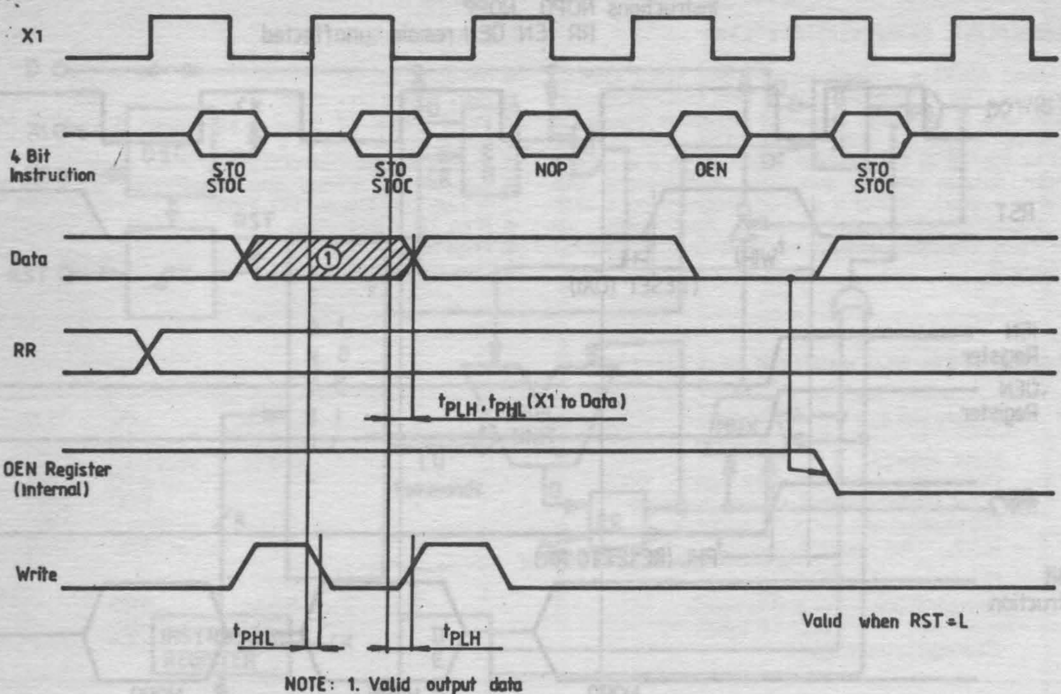
Instruction	Code	Mnemonic	Action
0	0000	NOPO	No Change in registers; RR ←— RR; FLAGO ←— ⎍
1	0001	LD	Load result register; RR ←— DATA
2	0010	LDC	Load complement; RR ←— $\overline{\text{DATA}}$
3	0011	AND	Logical AND; RR ←— RR ✻ DATA
4	0100	ANDC	Logical AND with complement; RR ←— RR ✻ $\overline{\text{DATA}}$
5	0101	OR	Logical OR; RR ←— RR + DATA
6	0110	ORC	Logical OR vith complement; RR ←— RR + $\overline{\text{DATA}}$
7	0111	XNOR	Exclusiv NOR; if RR = DATA, RR ←— 1
8	1000	STO	Store; DATA ←— RR; WRITE ←— ⎍
9	1001	STOC	Store complement; DATA ←— RR; WRITE ←— ⎍
10	1010	IEN	Input enable; IEN Register ←— DATA
11	1011	OEN	Output enable; OER Register ←— DATA
12	1100	JMP	Jump; JMP Flag ←— ⎍
13	1101	RTN	Return; RTN Flag ←— ⎍ *and skip next instruction*
14	1110	SKZ	Skip next instruction if RR = 0
15	1111	NOPF	No change in registers; RR ←— RR; FLAGF ←— ⎍

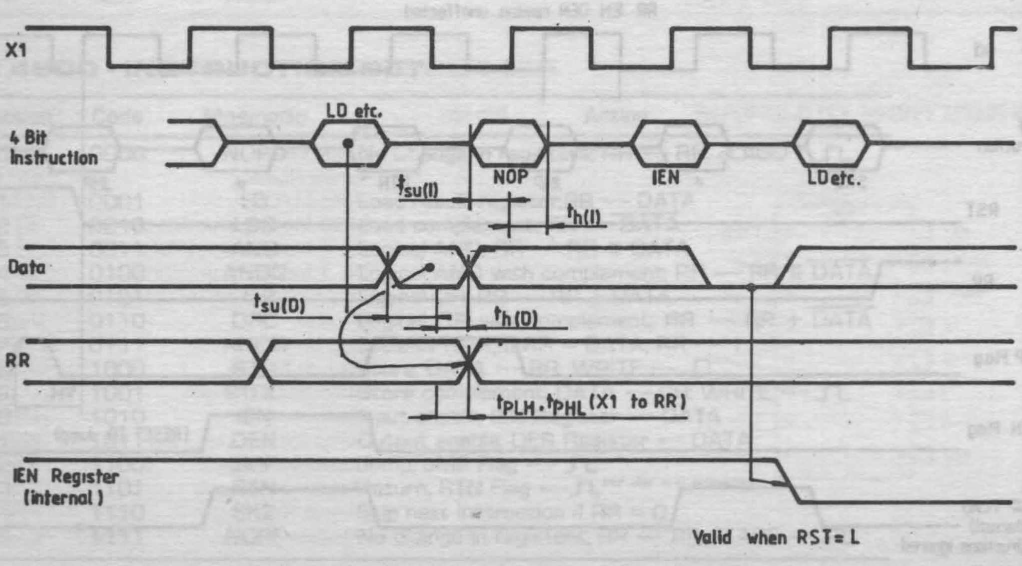
TIMING DIAGRAM





TIMING DIAGRAM





STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L —Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000	
	E, F types	0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V_{OH} —Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL} —Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH} —Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL} —Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
V_{IH} Input High Voltage (I3,I2,I1,I0, Pins)			0.5/4.5	< 1	5	2.5		2.5	2.2		2.5		V
			1/9	< 1	10	6		6	3.1		6		
			1.5/13.5	< 1	15	15		10	4.3		10		
V_{IL} Input Low Voltage (I3,I2,I1,I0, Pins)			4.5/0.5	< 1	5		0.8		1.1	0.8		0.8	V
			9/1	< 1	10		1.6		2.2	1.6		1.6	
			13.5/1.5	< 1	15		2.4		3.4	2.4		2.4	
I_{OH} —Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
		0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
		0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
		0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
	E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
		0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
		0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
		0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL} —Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{OH} Output drive Current (DATA, WRITE Pins) All types		0/ 5	4.6		5	−1.2		−1.0	−2.0		−0.7		mA
		0/10	9.5		10	−3.6		−3.0	−6.0		−2.1		
		0/15	13.5		15	−7.2		−6.0	−12.0		−4.2		
I_{OL} Output Sink Current (DATA, Write Pins) All types		0/ 5	0.4		5	1.9		1.6	3.2		1.1		mA
		0/10	0.5		10	3.6		3.0	6.0		2.1		
		0/15	7.2		15	6.0		6.0	12.0		4.2		

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T_{LOW}^* min.	T_{LOW}^* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}^* min.	T_{HIGH}^* max.	UNIT
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	
I_{in}	Input Current (RST Pin)					15	25			150			250	μA
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	—Input capacitance			Any input						5	7.5			pF
C_{in}	Input Capacitance (DATA Pin)									15				pF
I_T ※	Total Supply Current at on External Load Capacitance (CL) on All outputs					5 10 15	I_T=(1.5μA/kHz)xf+I_L I_T=(3.0μA/kHz)xf+I_L I_T=(4.5μAk/Hz)xf+I_L							μA

※ The formulas given are for the typical characteristics only at 25°C

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

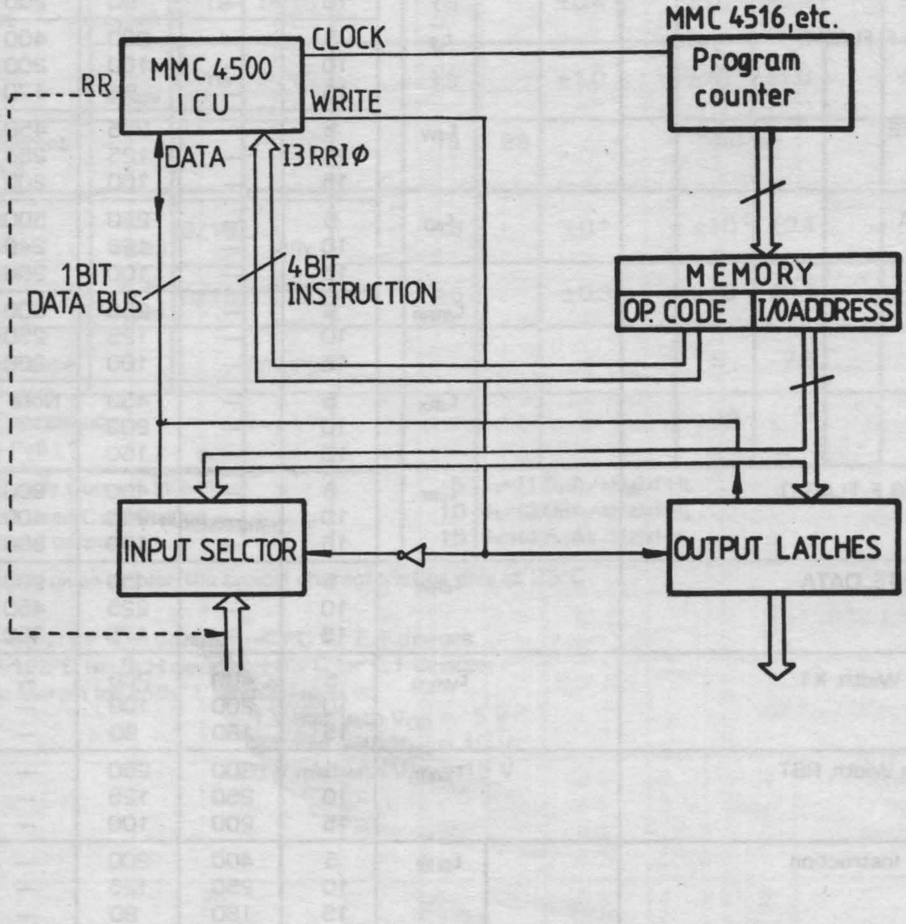
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A=25°C; C_L=50pF for JMP, X1, RR, FLAGO, FLAGF; C_L=130pF+1TTL load for DATA and WRITE; R_L=200K; all inputs rise and fall times=20 ns).

CHARACTERISTICS	SYMBOL	V_{DD}	VALUES			UNITS
			Min.	Typ.	Max.	
Propagation delay Time X1 to RR	t_{dR}	5	—	250	500	ns
		10	—	125	250	
		15	—	100	200	
X1 to FLAG F, FLAG O RTN, JMP	t_{dF}	5	—	200	400	
		10	—	100	200	
		15	—	85	170	
X1 to WRITE	t_{dW}	5	—	225	450	
		10	—	125	250	
		15	—	100	200	
X1 to DATA	t_{dD}	5	—	250	500	
		10	—	120	240	
		15	—	100	200	
RST to RR	t_{dRRR}	5	—	250	500	
		10	—	125	250	
		15	—	100	200	
RST to X1	t_{dRX}	5	—	450	Note 1	
		10	—	200		
		15	—	150		
RST to FLAG F, FLAG O, RTN, JMP	t_{dRF}	5	—	400	800	
		10	—	200	400	
		15	—	150	300	
RST to WRITE, DATA	t_{dRW}	5	—	450	900	
		10	—	225	450	
		15	—	175	350	
Clock Pulse Width, X1	$t_{W(c1)}$	5	400	200	—	ns
		10	200	100	—	
		15	180	90	—	
Reset Pulse Width, RST	$t_{W(R)}$	5	500	250	—	ns
		10	250	125	—	
		15	200	100	—	
Setup time. Instruction	$t_{SU(I)}$	5	400	200	—	ns
		10	250	125	—	
		15	180	90	—	
Data	$t_{SU(D)}$	5	200	100	—	
		10	100	50	—	
		15	80	40	—	
Hold Time Instruction	$t_{h(I)}$	5	100	0	—	ns
		10	50	0	—	
		15	50	0	—	
Data	$t_{h(D)}$	5	200	100	—	
		10	100	50	—	
		15	100	50	—	

Note 1: Maximum reset Delay may extend to one half clock period
Data tabelled "Typ" is not to be used for design purposes but is intended as an indication of the IC potential performance

TYPICAL APPLICATIONS



HEX NON-INVERTING TRI-STATE BUFFER

GENERAL DESCRIPTION

The MMC 4503 is a hex non-inverting TRI-STATE buffer with high output current sink and source capability. TRI-STATE outputs make it useful in bus oriented applications. Two separate disable inputs are provided. Buffers 1 to 4 are controlled by the disable A input. Buffers 5 and 6 are controlled by the disable B input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

FEATURES

- Wide supply voltage range 3.0 V_{DC} to 18 V_{DC}
- TRI-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- 1 TTL-load output drive capability
- 2 output-disable controls
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

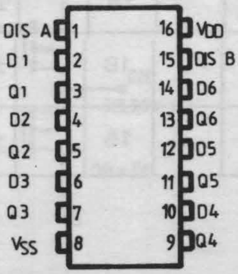
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	-5.8		-4.8	-6.1		-3		mA
			0/ 5	4.6		5	-1.2		-1.02	-1.9		-0.7		
			0/10	9.5		10	-3.1		-2.6	-3.7		-1.8		
			0/15	13.5		15	-8.2		-6.8	-14.1		-4.8		
		E, F types	0/ 5	2.5		5	-4.8		-4.1	-5.2		-2.9		
			0/ 5	4.6		5	-1		-0.8	-1.6		-0.6		
			0/10	9.5		10	-2.5		-2.2	-3.1		-1.6		
			0/15	13.5		15	-6.8		-5.8	-11.9		-4.2		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	2.6		2.1	2.3		1.3		mA
			0/10	0.5		10	6.5		5.5	2.6		3.8		
			0/15	1.5		15	19.2		16.1	23		11.2		
		E, F types	0/ 5	0.4		5	2.1		1.8	1.9		1.2		
			0/10	0.5		10	5.4		4.7	5.3		3.3		
			0/15	1.5		15	1.6		13.7	19.5		9.7		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	max.	25°C min.	typ	max.	T^*_{HIGH} min.	max.	UNIT
C_I	Input capacitance		Any input						5	7.5			pF

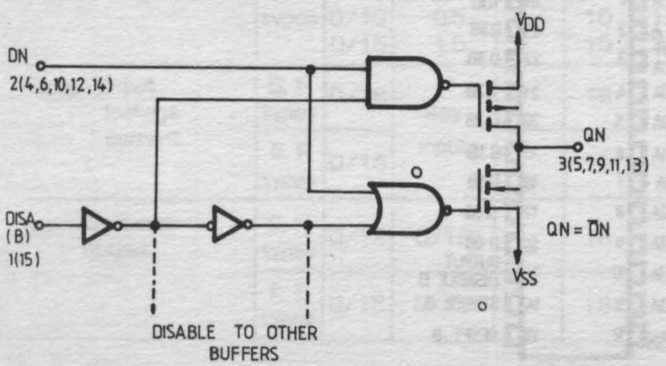
* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time Low-to-High	5		75	150	
		10		35	70	
		15		25	50	
	High-to-Low	5		55	110	ns
		10		25	50	
		15		17	35	
t_{PHZ}, t_{PZH}	3—state propagation delay time	5		70	140	
		10		30	60	
		15		25	50	
t_{PZL}, t_{PLZ}	3—state propagation delay time	5		90	180	ns
		10		40	80	
		15		35	70	
t_{TLH}, t_{THL}	Transition time Low-to-High	5		50	90	
		10		30	45	
		15		25	35	
	High-to-Low	5		35	70	ns
		10		20	40	
		15		13	25	

LOGIC DIAGRAM AND TRUTH TABLE



DN	DISA(B)	QN
0	0	0
1	0	1
X	1	HIGH Z

DUAL 4-BIT LATCH

The MMC 4508 dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET and OUTPUT DISABLE controls. With the STROBE line in high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the RESET line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line application by a high level on the DISABLE input.
The MMC 4508 E/F/G/H types are supplied in the 24-lead dual-in-line ceramic or plastic packages.

FEATURES

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation: $t_{PLH} = t_{PHL} = 70$ ns (typ.) at $V_{DD} = 10$ V and $C_L = 50$ pF

APPLICATIONS

- Buffer storage
- Holding register
- Data storage and multiplexing

ABSOLUTE MAXIMUM RATINGS

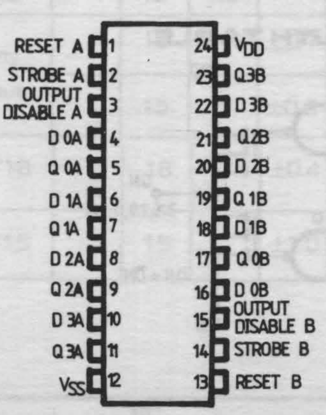
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
C_I	—Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

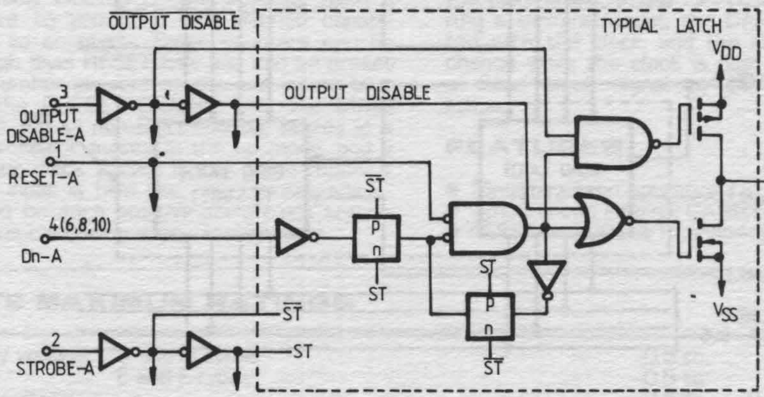
($T_A = 25°C$, input t_r t_f = 20 ns, C_L = 50 pF, R_l = 200 kΩ, unless otherwise specified)

PARAMETER			TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{THL}, t_{TLH}	Transition time		5 10 15		100 50 40	200 100 80	ns
t_W(R)	Reset pulse width		5 10 15	200 140 100	100 70 50		ns
t_W(st)	Strobe pulse width		5 10 15	140 80 70	70 40 35		ns
t_{setup}	Setup time		5 10 15	50 30 20	25 15 10		ns
t_H	Hold time		5 10 15	0 0 0	0 0 0		ns
t_{PHL}, t_{PLH}	Propagation delay times:	Strobe to data out	5 10 15		130 70 50	260 140 100	ns
		Data in to data out	5 10 15		105 60 45	210 120 90	ns
		Reset to data out	5 10 15		90 50 40	180 100 80	ns
t_{PHZ}	3-state propagation delay times: output high to high impedance		5 10 15		90 50 35	180 100 70	ns
t_{PZH}	High impedance to output high		5 10 15		90 50 35	180 100 70	ns
t_{PLZ}	Output low to high impedance		5 10 15		90 50 35	180 100 70	ns

PARAMETER		TEST CONDITIONS	V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PZL}	High impedance to output low		5 10 15		90 50 35	180 100 70	ns

LOGIC DIAGRAM (A Section)

1 of 4 identifical latches with common output disable, reset and strobe

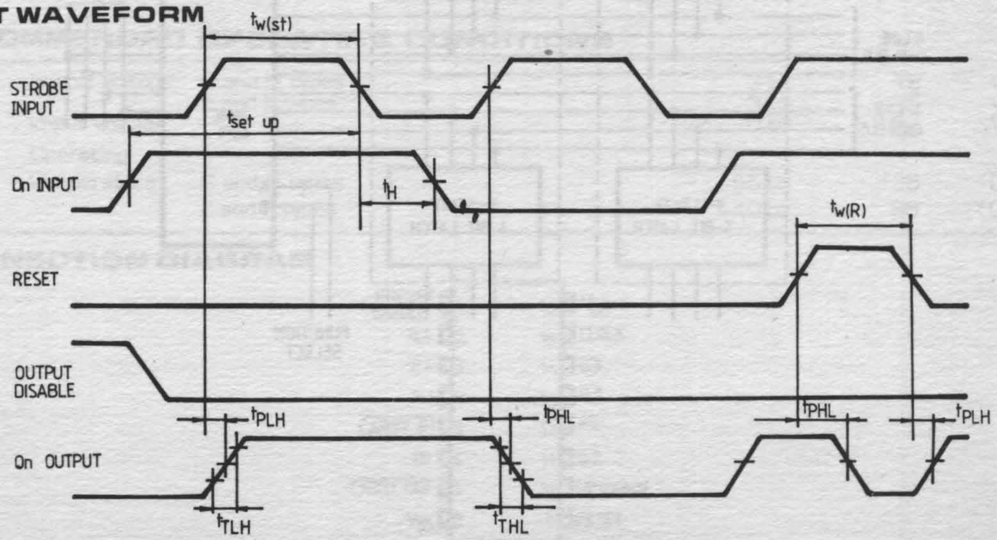


TRUTH TABLE

RESET	DISAB	STROBE	D INPUT	Q INPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	Latched
1	0	X	X	0
X	1	X	X	Z

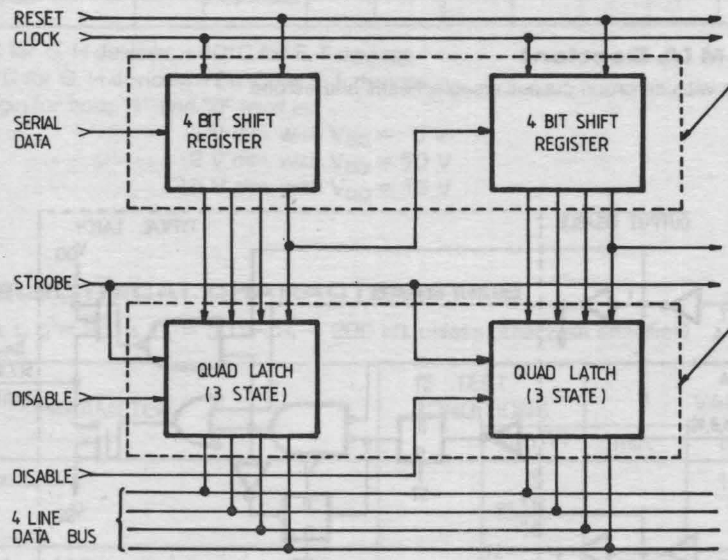
1 = High level
0 = Low level
X = Don't care
Z = High impedance

TEST WAVEFORM

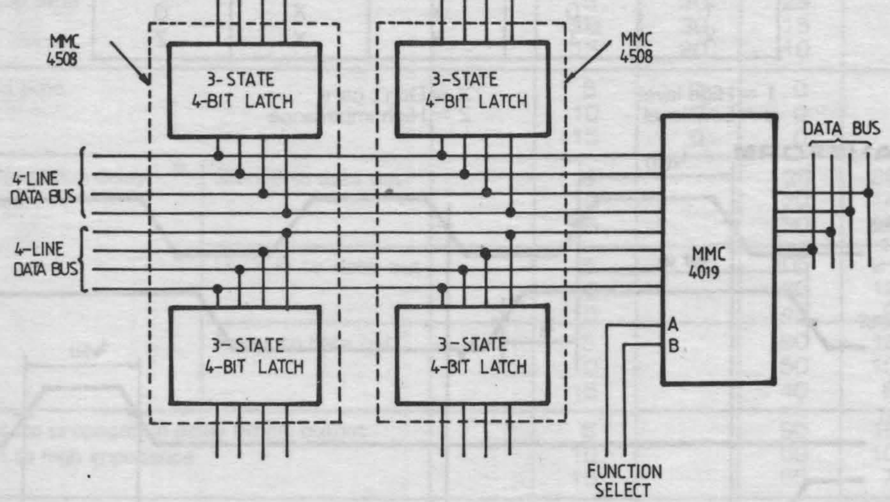


TYPICAL APPLICATIONS

Bus register



Dual multiplexed bus register with function select



PRESETTABLE UP/DOWN COUNTERS: MMC 4510 PRESETTABLE BCD UP/DOWN COUNTERS MMC 4516 PRESETTABLE BINARY UP/DOWN COUNTER

GENERAL DESCRIPTION

The MMC 4510, MMC 4516 are monolithic integrated circuits available in 16-lead dual in-line plastic package.
The MMC 4510 Presetable BCD Up/Down Counter and MMC 4516 Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The MMC 4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode. If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage. The MMC 4510 and MMC 4516 can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

FEATURES

- Medium speed operation $f_{c1} = 8$ MHz typ. at 10 V
- Synchronous internal $\overline{\text{CARRY}}$ propagation
- RESET and PRESET capability

ABSOLUTE MAXIMUM RATINGS

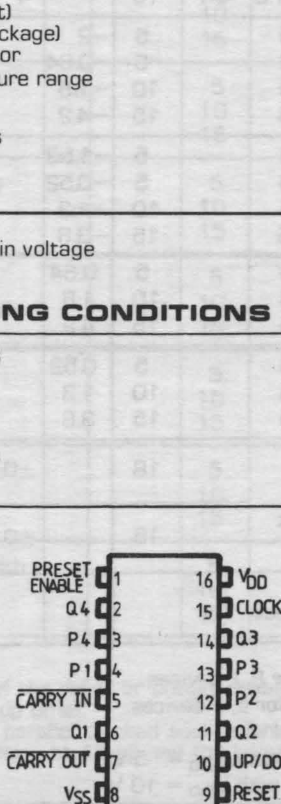
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

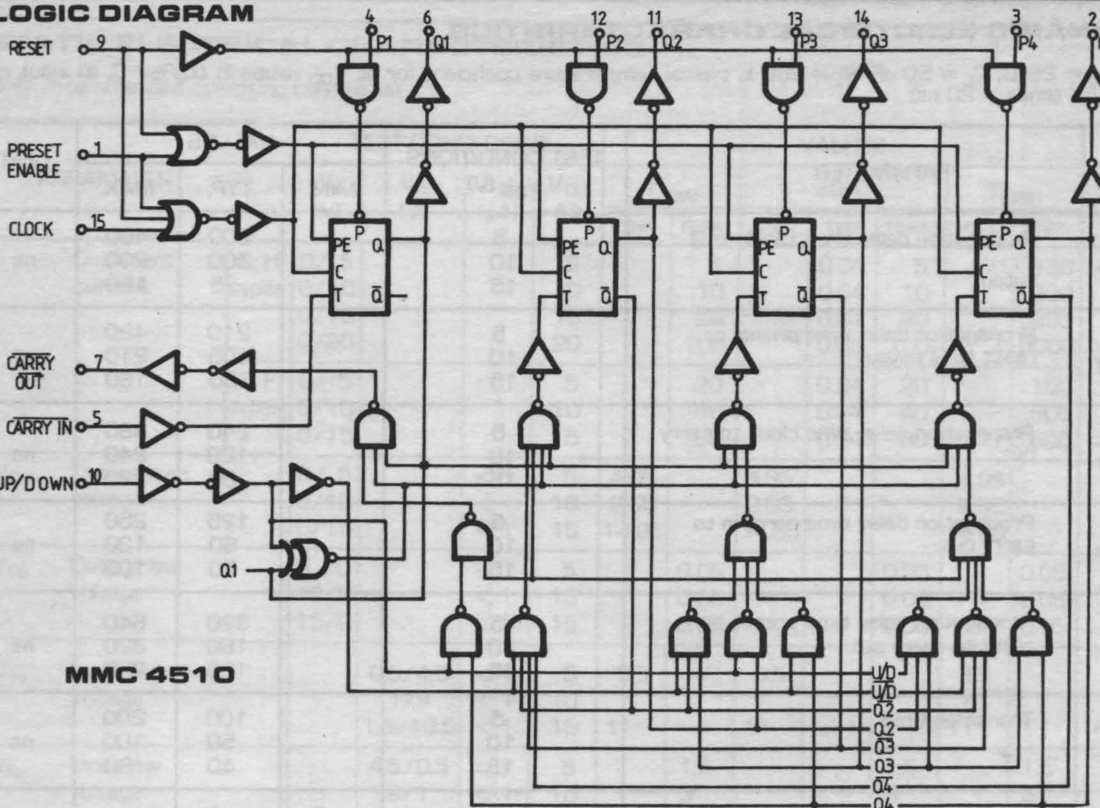
(T_{amb} = 25°C, C_L = 50 pF, R_L = 200 k, typical temperature coeficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES MIN.	TYP.	MAX.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time Clock to Q output	5 10 15		200 100 75	400 200 150	ns
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to Q output	5 10 15		210 105 80	420 210 160	ns
t_{PHL}, t_{PLH}	Propagation delay time clock to carry out	5 10 15		240 120 90	480 240 180	ns
t_{PHL}, t_{PLH}	Propagation delay time carry in to carry out	5 10 15		125 60 50	250 120 100	ns
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to carry out	5 10 15		320 160 125	640 320 250	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{max},	Max. clock frequency	5 10 15	2 4 5.5	4 8 11		MHz
t_W,	Clock pulse width	5 10 15	150 75 60			ns
	(•) Preset enble or removal time	5 10 15	150 80 60			ns
t_r, t_f	•• Clock rise and fall time	5 10 15			15 5 5	ns
t_{setup}	Carry in setup time	5 10 15	130 60 45			ns
t_{setup}	Up-down setup time	5 10 15	360 160 110			ns
t_W	Preset enable or reset pulse width	5 10 15	220 100 75			ns

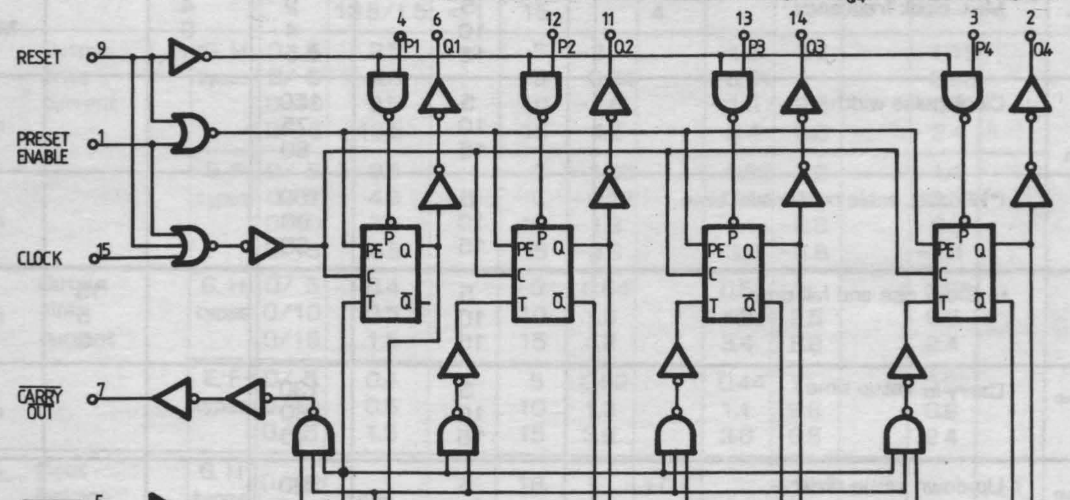
(•) Time required atter the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

•• If more than unit is cascaded in the parallel clocked application, t_r clock should be made less than or equal to the sum of the fixed propayation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

LOGIC DIAGRAM



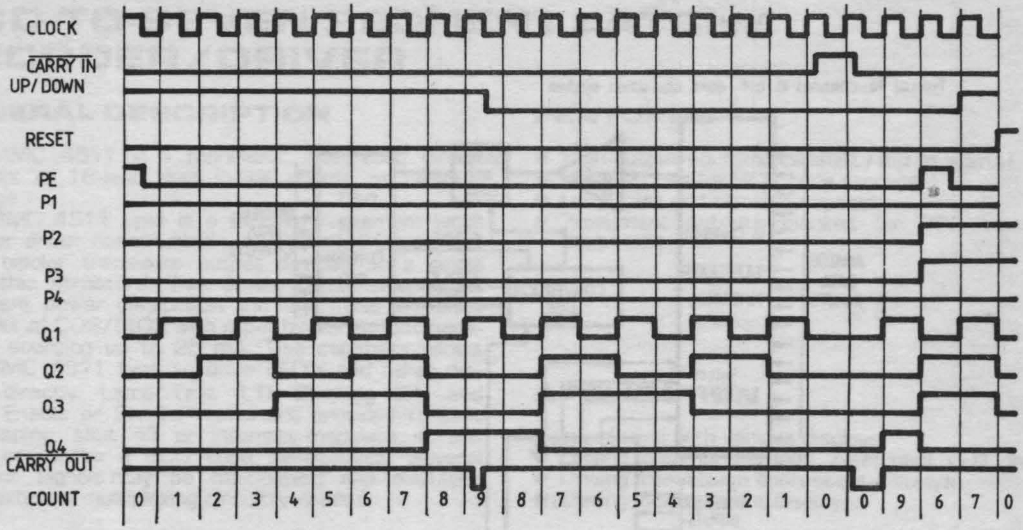
MMC 4510



MMC 4516

TIMING DIAGRAMS

MMC 4510



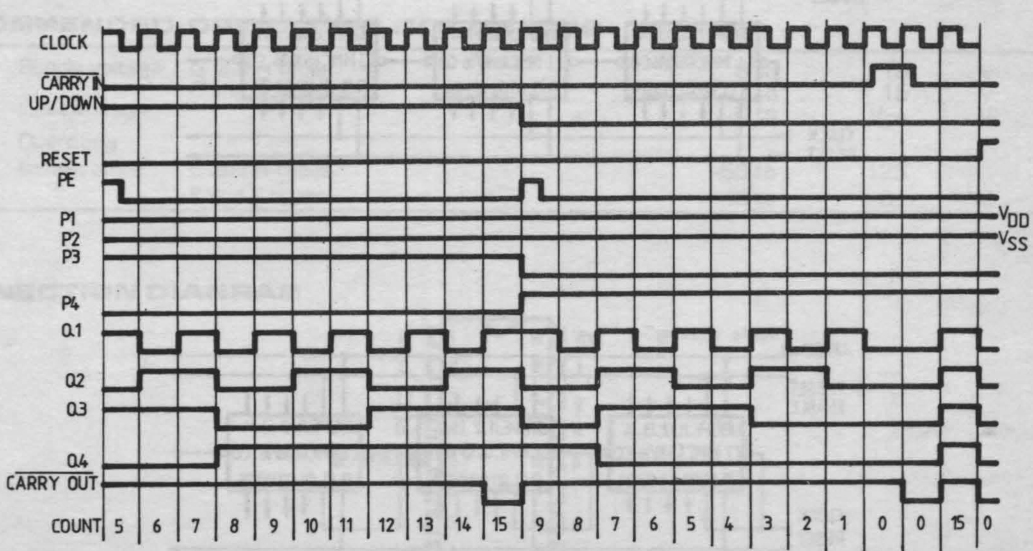
TRUTH TABLE

CL	CI	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
_/‾	0	1	0	0	COUNT UP
_/‾	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = Don't care

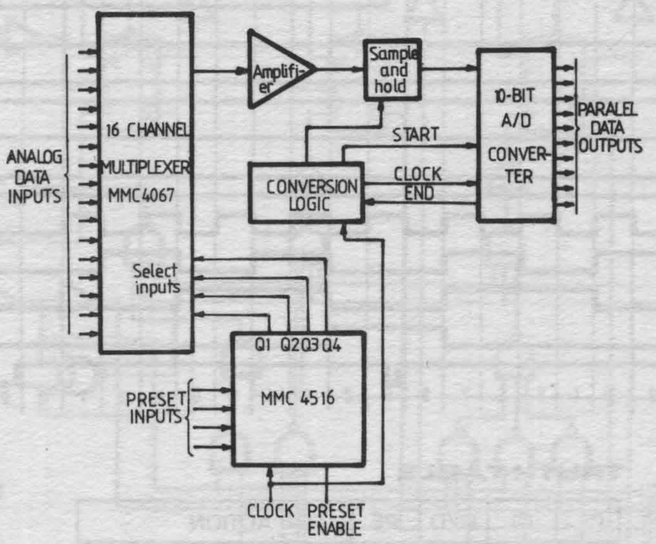
TIMING DIAGRAM

MMC 4516



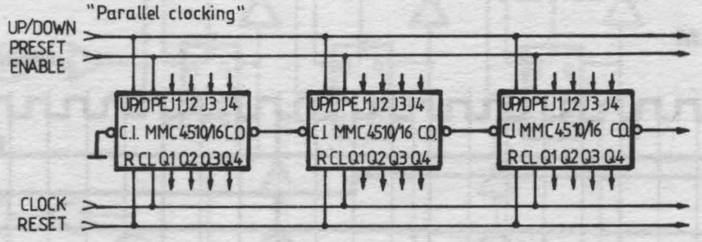
TYPICAL APPLICATIONS

Typical 16-channel 10 bit data aquisition system

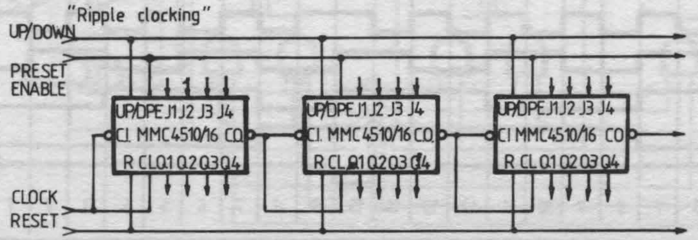


This aquisition system can be operated in the random access mode by jamming in the channel number at the present inputs. or in the sequential mode by clocking the MMC 4516.

"Parallel clocking"



"Ripple clocking"



BCD-TO-SEVEN SEGMENT LATCH/ DECODER/DRIVER

GENERAL DESCRIPTION

The MMC 4511 is a monolithic integrated circuit available in 16-lead dual in-line plastic or ceramic package
The MMC 4511 type is a BCD-to-7-segment latch decoder driver constructed with COS/MOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. This device combines the low quiescent power dissipation and high noise immunity features of COS/MOS with n-p-n bipolar output capable of sourcing up to 25 mA. This capability allows the MMC 4511 type to drive LED's and other displays directly. Lamp Test (LT), Blanking (BL) and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

FEATURES

- High-output-sourcing capability (up to 25mA)
- Input latches for BCD code storage
- Lamp test and blanking capability
- 7-segment outputs blanked for BCD input codes>1001

APPLICATION

- Interfacing with various displays
- Driving common-cathode 7-segment LED displays
- Driving low-voltage fluorescent displays
- Driving incandescent displays.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

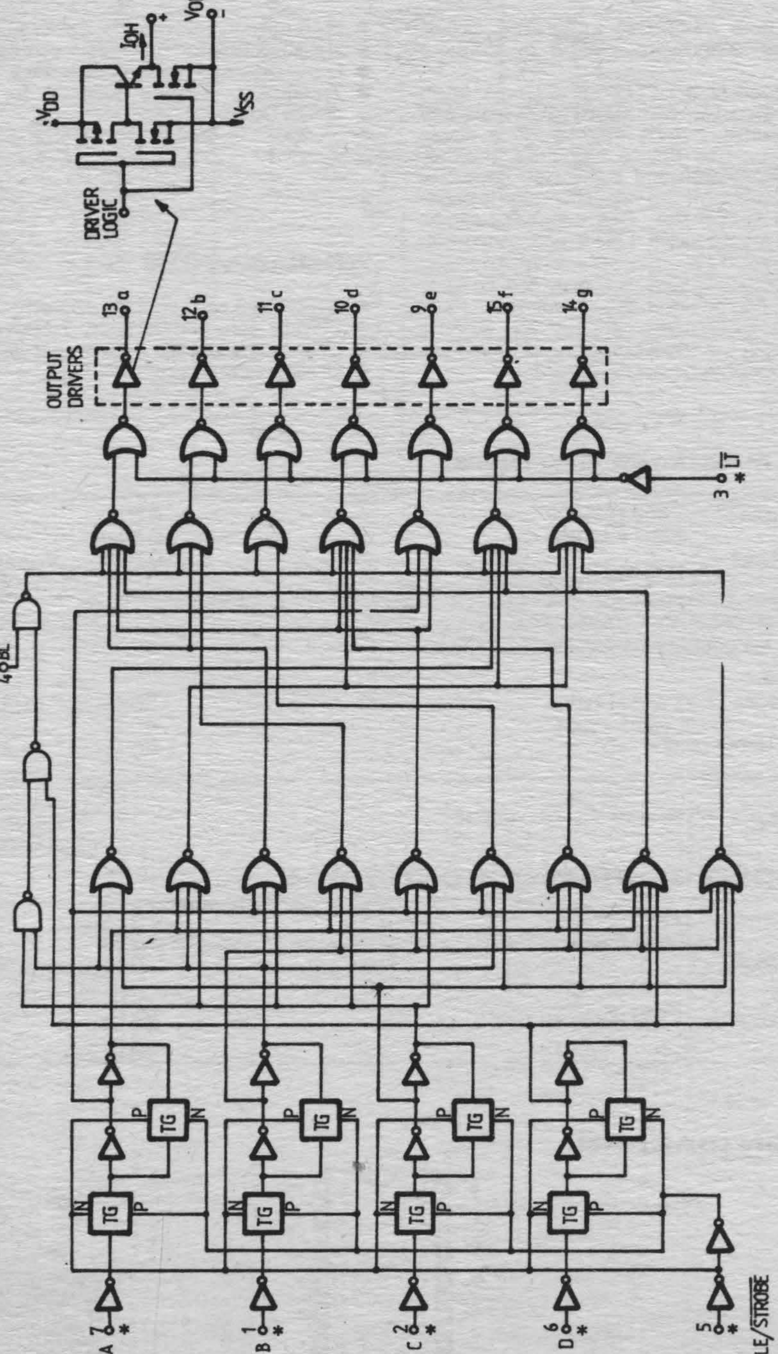
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

LOGIC DIAGRAM

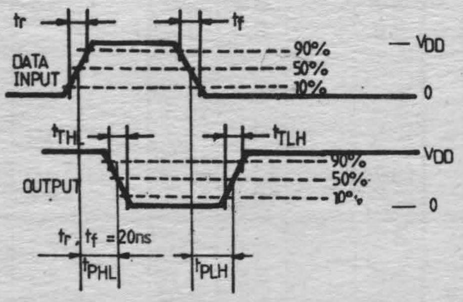


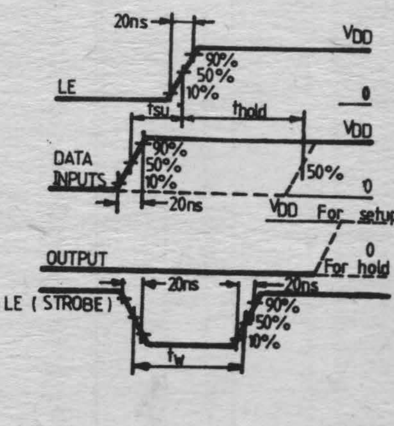
TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				⁎				⁎

X = Don't care
⁎ = Depends on BCD code previously applied when LE = 0
Note : Display is blank for all illegal input codes (BCD > 1001)

WAVEFORMS





STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNI
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5			5	4		4.1	4.55		4.2		V
			0/10			10	9		9.1	9.55		9.2		
			0/15			15	14		14.1	14.55		14.2		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
V_{OH}	Output drive voltage	G, H types			0	5	4.1		4.1	4.55		4.2		V
					5					4.25				
					10		3.8		3.9	4.10		3.9		
					15					3.95				
					20		3.55		3.4	3.75				
					25		3.4		3.1	3.55				
					0	10	9		9.1	9.55		9.2		V
					5					9.25				
					10		8.85		9	9.15				
					15					9.05				
					20		8.7		8.6	8.9		8.4		
					25		8.6		8.3	8.75				
					0	15	14		14.1	14.55		14.2		V
					5					14.3				
					10		13.9		14	14.2		14.0		
					15					14.1				
					20		13.75		13.7	13.95		13.5		
					25		13.65		13.5	13.8		13.1		
		E, F types			0	5	4.1		4.1	4.57		4.1		V
					5					4.24				
					10		3.6		3.6	4.12		3.3		
					15					3.94				
					20		2.8		2.8	3.75		2.5		
					25					3.54				
					0	10	9.1		9.1	9.58		9.1		V
					5					9.26				
					10		8.75		8.75	9.17		8.45		
					15					9.04				
					20		8.1		8.1	8.9		7.8		
					25					8.75				

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	
		E, F types			0	15	14.1		14.1	14.59		14.1		V
					5					14.27				
					10		13.75		13.75	14.18		13.45		
					15					14.07				
					20		13.1		13.1	13.95		12.8		
					25					13.8				
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

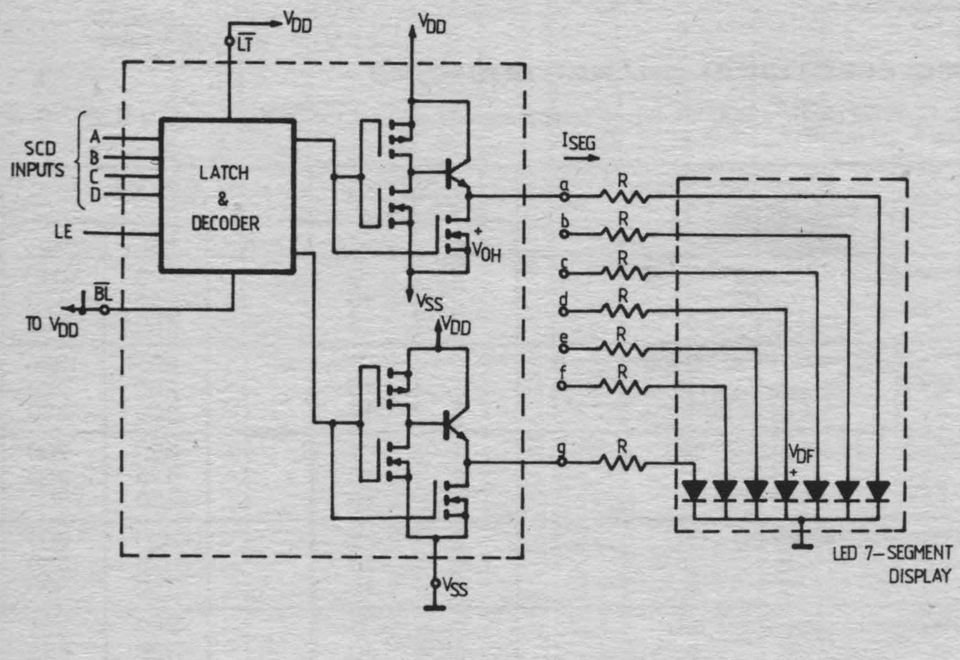
($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNIT
t_{PHL}	Propagation delay time (Data)	5		520	1040	ns
		10		210	420	
		15		150	300	
t_{PLH}	Propagation delay time (Data)	5		660	1320	ns
		10		260	520	
		15		180	360	
t_{PHL}	Propagation delay time ($\overline{BL}$)	5		350	700	ns
		10		175	350	
		15		150	300	
t_{PLH}	Propagation delay time ($\overline{BL}$)	5		400	800	ns
		10		175	350	
		15		150	300	
t_{PHL}	Propagation delay time ($\overline{LT}$)	5		250	500	ns
		10		125	250	
		15		85	170	
t_{PLH}	Propagation delay time ($\overline{LT}$)	5		150	300	ns
		10		75	150	
		15		50	100	

PARAMETER		TEST CONDITIONS VDD(V)	VALUES min.	typ.	max.	UNIT
t_{TLH}	Transition time	5 10 15		40 30 20	80 60 50	ns
t_{THL}	Transition time	5 10 15		125 75 65	310 185 160	ns
t_{setup}	Setup time	5 10 15	150 70 40	75 35 20		ns
t_{hold}	Hold time	5 10 15	0 0 0	-75 -35 -20		ns
t_W	Strobe pulse width	5 10 15	400 160 100	200 80 50		ns

APPLICATION

Driving common-cathode 7-segment LED displays



8 - CHANNEL DATA SELECTOR

GENERAL DESCRIPTION

The MMC 4512 (G and H types) and MMC 4512 (E and F types) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4512 is an 8-channel data selector featuring a tri-state output that can interface directly with, and drive, date lines of bus oriented systems.

FEATURES

- 3-state output
- Quiescent current specified to 20 V for G and H types
- 5 V, 10 V and 15 V parametric ratings
- Input current of 100 nA at 18 V and 25° C for G and H types, 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

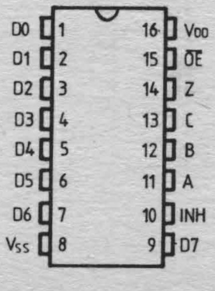
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

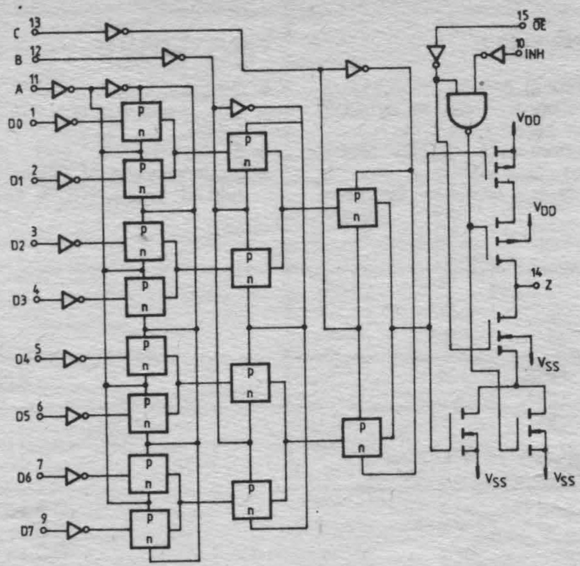
RECOMMENDED OPERATING CONDITIONS

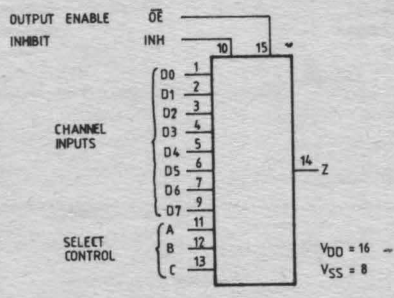
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM





TRUTH TABLE

SEL. CONT.			INH.	3— STATE DISABLE	SEL. OUTPUT
A	B	C			
0	0	0	0	0	D0
1	0	0	0	0	D1
0	1	0	0	0	D2
1	1	0	0	0	D3
0	0	1	0	0	D4
1	0	1	0	0	D5
0	1	1	0	0	D6
1	1	1	0	0	D7
X	X	X	1	0	0
X	X	X	X	1	High Z

1 = High level

0 = Low level

X = Don't Cavre

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
I_L —Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000	
	E, F types	0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V_{OH} —Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL} —Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH} —Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL} —Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH} Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
		0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
		0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
		0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
	E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
		0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
		0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
		0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL} Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL} Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
	E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH} 3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
	E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
C_I	Input capacitance		Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25° C, C_L = 50 pF, R_L = 200 k typical temperature coefficient for all V_{DD} values is 0.3/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS	VALUES V_{DD}(V)	Min.	Typ.	Max.	Unit
t_{PHL}, t_{PLH}	Propagation delay time inhibit to output		5		140	280	ns
			10		70	140	
			15		50	100	
t_{PHL}, t_{PLH}	Propagation delay time „A" select to output		5		200	400	ns
			10		85	170	
			15		60	120	
t_{PHL}, t_{PLH}	Propagation delay time data to output		5		180	360	ns
			10		75	150	
			15		55	110	
t_{PZL}, t_{PLZ}, t_{PHZ}, t_{PZH}	3—state disable delay time		5		60	120	ns
			10		30	60	
			15		20	40	
t_{THL}, t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	

DUAL UP-COUNTERS:
MMC 4518 DUAL BCD UP-COUNTER
MMC 4520 DUAL BINARY UP-COUNTER

GENERAL DESCRIPTION

The MMC 4518/4520 are monolithic integrated circuits available in 16-lead dual in-line plastic package.
The MMC 4518 Dual BCD Up Counter and MMC 4520 Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained „high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines. The counter can be cascaded in the ripple mode by connecting Q4 to the Enable input of the subsequent counter while the clock input of the latter is held low.

FEATURES

- Medium-speed operation-6 MHz typ. clock frequency at 10 V
- Positive or negative edge triggering
- Synchronous internal CARRY propagation

ABSOLUTE MAXIMUM RATINGS

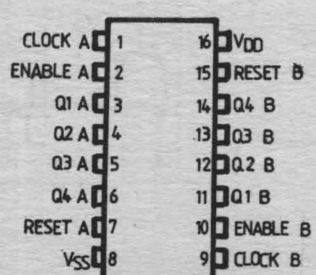
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

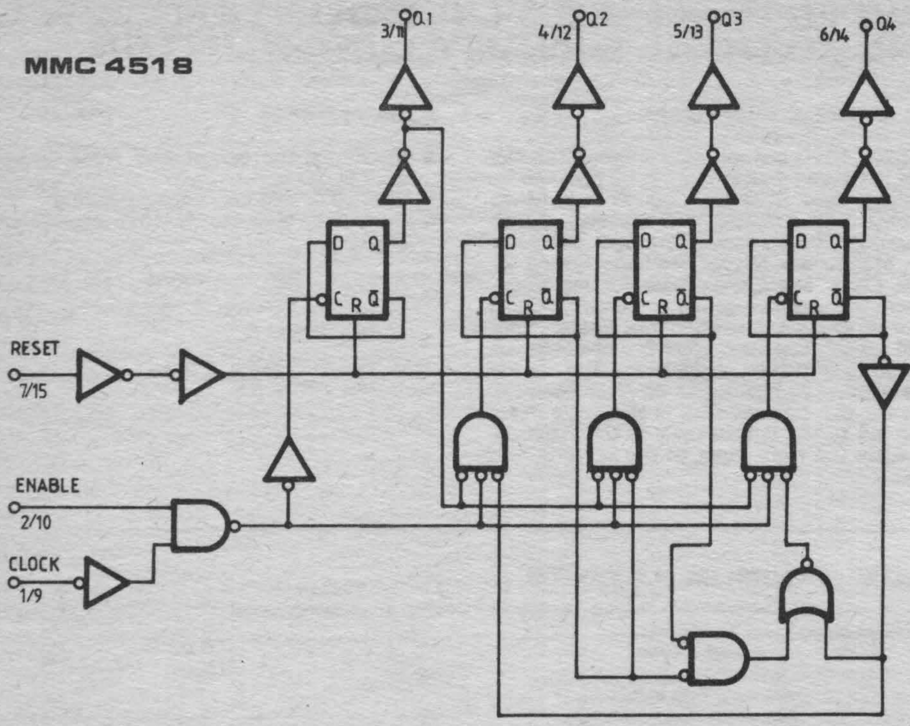
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

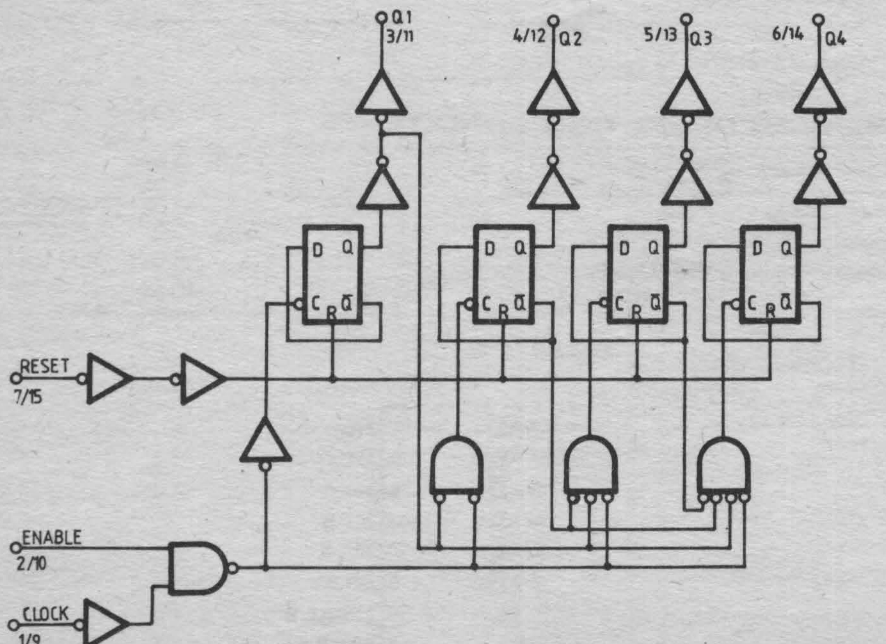


LOGIC DIAGRAMS

MMC 4518



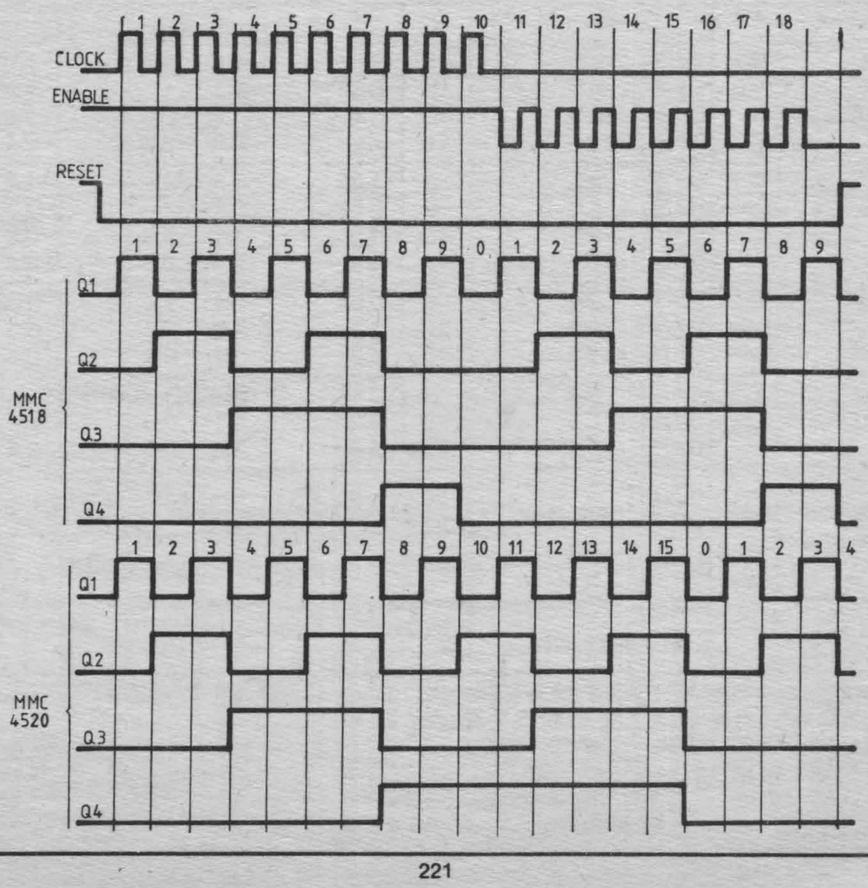
MMC 4520



TRUTH TABLE for MMC 4518/4520

CLOCK	ENABLE	RESET	ACTION
↑	1	1	Increment counter
0	↓	0	Inter counter
X	↑	0	No change
↓	X	0	No change
↑	0	0	No change
1	↓	0	No change
X	X	1	Q1 thru Q4 = 0

TIMING DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	µA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	µA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

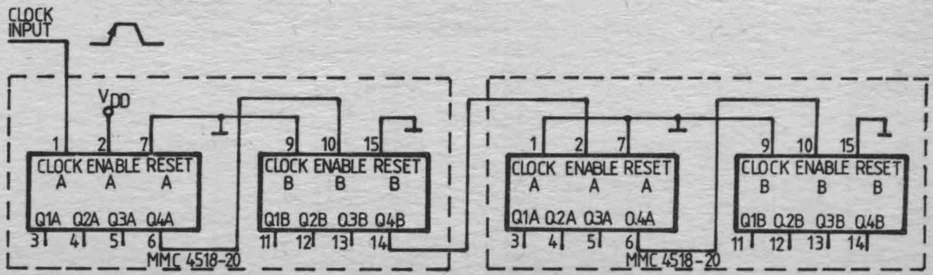
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

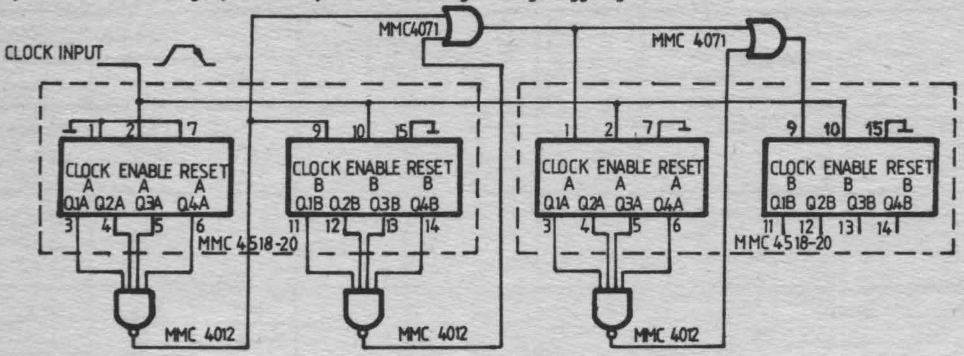
PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES			UNIT
			Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	propagation delay time (Reset to output)	5 10 15		280 115 80	560 230 160	ns
t_{PLH}, t_{PHL}	Propagation delay time (Clock or Enable to output)	5 10 15		330 130 90	650 225 170	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
t_W,	Clock pulse width	5 10 15	200 100 70	100 50 35		ns
t_W,	Enable pulse width	5 10 15	400 200 140	200 100 70		ns
t_r, t_f	Clock or enable rise and fall time	5 10 15			15 15 5	μs
f_{max},	Maximum clock frequency	5 10 15	1.5 3 4	3 6 8		MHz
t_r, t_f	Clock input rise and fall time	5 10 15			15 5 5	μs
t_W,	Reset pulse width	5 10 15	250 110 80	125 55 40		ns

TYPICAL APPLICATIONS

Ripple cascading of four counters with positive-edge triggering



Synchronous cascading of four binary counters with negative-edge triggering



BCD-TO-SEVEN SEGMENT LATCH/ DECODER/DRIVER

GENERAL DESCRIPTION

The MMC 4543 BCD-to-7 Segment Latch/Decoder /Driver is designed for use with liquid crystal readouts and is constructed with complementary MOS (CMOS) enchancement-mode devices. The circuit provides the functions of a 4-bit storage latch and a 8421 BCD-to 7 segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The Phase (Ph), Blanking (BI), and Latch Disable (LD) inputs are used to reverse the truth-table phase, blank the display, and store a BCD code, respectively. For liquid crystal readouts, a square wave is applied to the Ph input of the circuit and the electrically common back plane of the display. The outputs of the circuit are connected directly to the segments of the readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts connections diagrams are given on this data sheet

FEATURES

- Phase input signal reproduced on outputs for liquid crystal display
- Latched storage of input code
- Blanking input for display intensity modulation
- Readout blanking for illegal input combinations
- Balanced output drive current specifications

APPLICATIONS

Aplications include instrument (e.g. counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

ABSOLUTE MAXIMUM RATINGS

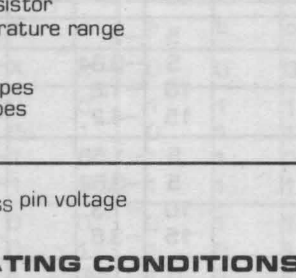
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	µA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	µA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(C_L = 5 pF, T_A = 25°C)

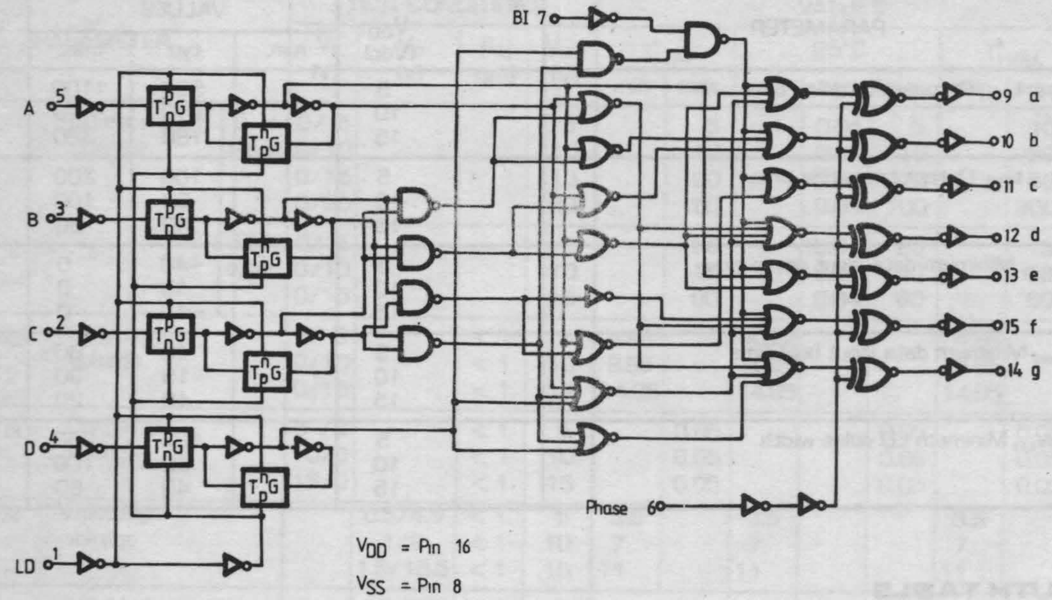
PARAMETER	V_{DD} (Vdc)	VALUES			UNIT
		min.	typ.	max.	
t_{PHL}, t_{PLH} Propagation delay time	5 10 15		550 210 160	1100 420 320	ns
t_{TLH}, t_{THL} Output transition time	5 10 15		100 50 40	200 100 80	ns
t_{setup} Minimum data input setup time	5 10 15		−40 −15 −10	0 0 0	ns
t_{hold} Minimum data input hold time	5 10 15		40 15 10	80 30 20	ns
PW_{LD} Minimum LD pulse width	5 10 15		125 50 40	250 100 80	ns

TRUTH TABLE

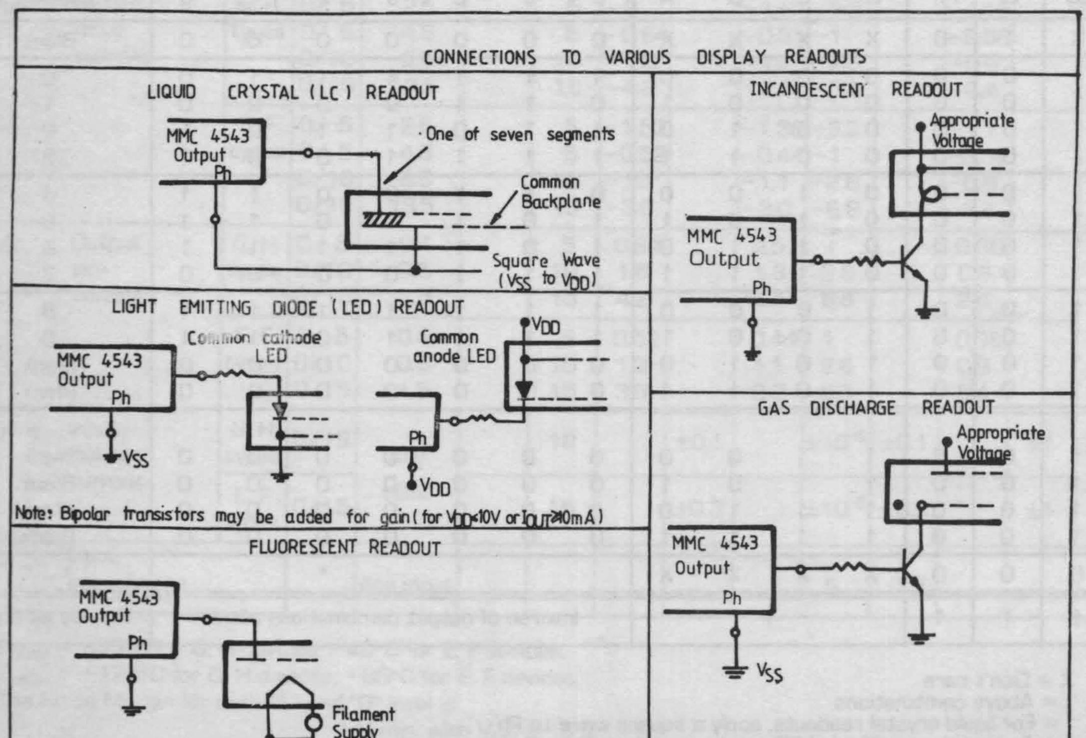
INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X			*		*			* *
†	†	1	†				Inverse of output combinations above							Display as above

X = Don't care
† = Above combinations
* = For liquid crystal readouts, apply a square wave to Ph
For common cathode LED readouts, select Ph = 0
For common anode LED readous, select Ph = 1
** = Depends upon the BCD code previously applied when LD = 1

LOGIC DIAGRAM



TYPICAL APPLICATIONS



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 40104 is a monolithic i.c., available in 16-lead dual in-line plastic or ceramic package The MMC 40104 is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register When the output enable input is low, all outputs assume the high impedance state.

FEATURES

- Medium-speed operation: f_{CL} = 9 MHz, V_{DD} = 10 V
- Fully static operation
- Synchronous parallel or serial operation
- Three-state outputs

APPLICATIONS

Control circuitry

ABSOLUTE MAXIMUM RATINGS

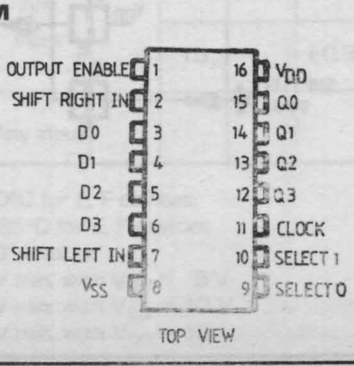
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

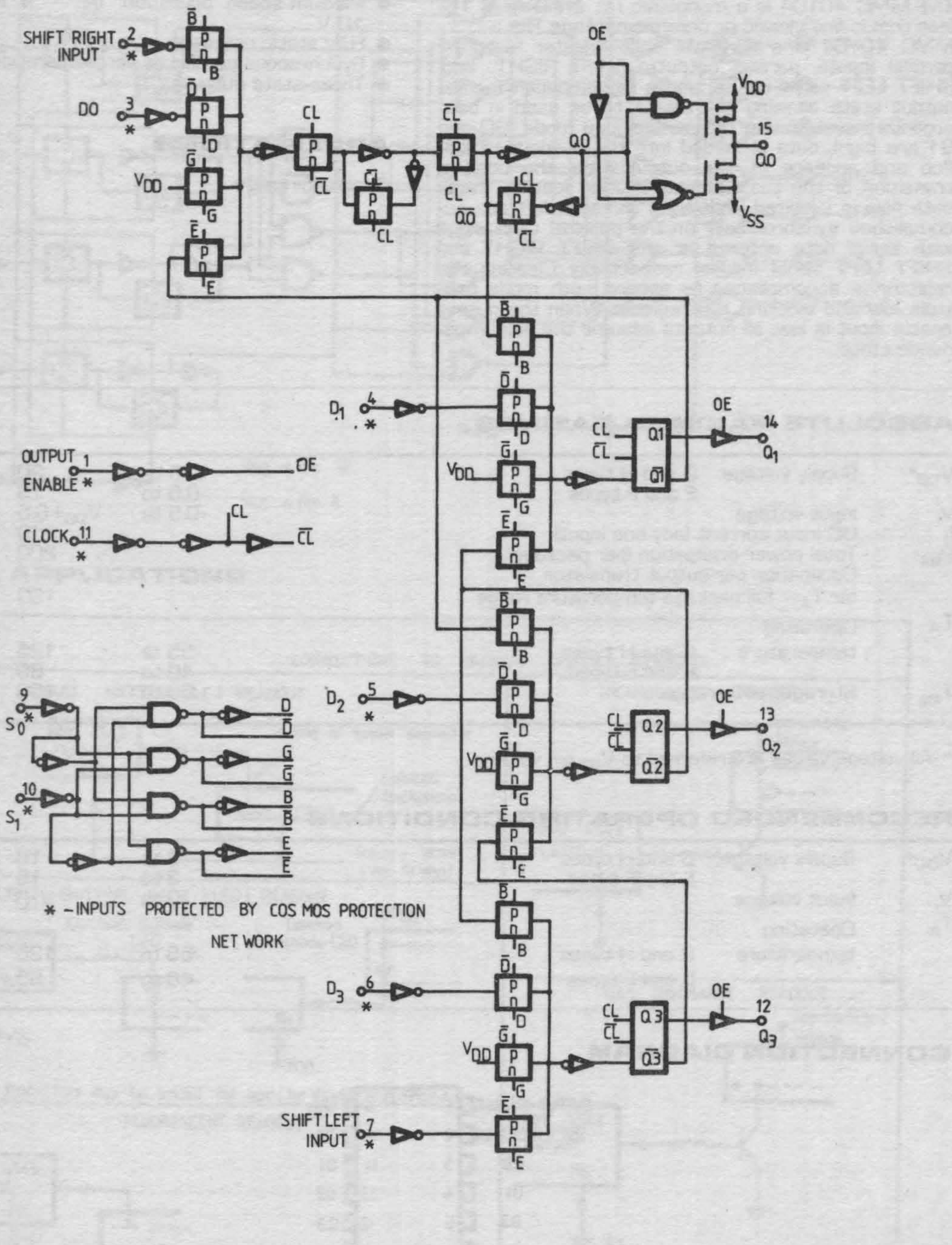
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns).

	PARAMETER	TEST CONDITIONS V_{DD}(V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time Clock to Q	5 10 15		220 100 70	440 200 140	ns
t_{PZH}, t_{PZL}, t_{PLZ}	3—state outputs High impedance	5 10 15		80 35 25	160 70 50	ns
t_{PHZ}		5 10 15		45 25 20	90 50 40	ns
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns
t_{setup}	Setup time D0, D3, SR, SL to Clock	5 10 15		80 35 20	100 70 50	ns
	S0, S1 to Clock	5 10 15		200 110 65	400 220 130	ns
t_{hold}	Hold time D0, D3, SR, SL	5 10 15		−65 −25 −15	0 0 0	ns
	S0, S1 to Clock	5 10 15		−170 −95 −55	0 0 0	ns
t_w	Clock pulse width	5 10 15		90 40 25	180 180 50	ns
f_{CL}	Clock input frequency	5 10 15	3 6 8	6 12 15		MHz
t_r, t_f	Clock input rise or fall time	5 10 15			1000 100 100	μs

TRUTH TABLE

CLOCK	MODE SELECT S0	MODE SELECT S1	OUTPUT ENABLE	ACTION
	0	0	1	Reset
	1	0	1	Shift right (Q0 toward Q3)
	0	1	1	Shift left (Q3 toward Q0)
	1	1	1	Parallel load
x	x	x	0	Operations occur as shown above, but outputs assume high impedance

DUAL 2-INPUT NAND BUFFER/DRIVER

GENERAL DESCRIPTION

The MMC 40107 is a monolithic i.c. available in 14-lead dual in-line ceramic package and plastic package.
The MMC 40107 is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs
This device features a wired-OR capability and high output sink current capability (136 mA typ at V_{DD} = 10 V, V_{DS} = 1 V)

FEATURES

- quiescent current specified to 20 V
- maximum input leakage of 1 μA at 18 V (full package temperature range)
- standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

APPLICATIONS

Driver circuits

ABSOLUTE MAXIMUM RATINGS

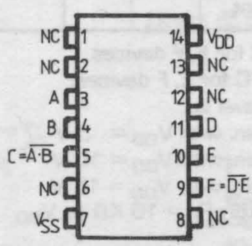
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
		0/10			10		2		0.02	2		60	
		0/15			15		4		0.02	4		120	
		0/20			20		20		0.04	20		600	
	E, F types	0/ 5			5		4		0.02	4		30	
		0/10			10		8		0.02	8		60	
		0/15			15		16		0.02	16		120	
V_{IH}** Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL}** Input low voltage			4.5	< 1	5		1.5			1.5		1.5	V
			9	< 1	10		3			3		3	
			13.5	< 1	15		4			4		4	
I_{OL} Output sink current	G, H types	5	0.4		5	21		16	32		12		
		5	1		5	44		30	68		25		
		10	0.5		10	49		37	74		28		
		10	1		10	89		68	136		51		
		15	0.5		15	66		50	100		38		
	E, F types	5	0.4		5	17		13.6	32		12		
		5	1		5	35.7		25.5	68		22		
		10	0.5		10	39.1		31.4	74		27		
		10	1		10	72.2		57.8	136		51		
		15	0.5		15	53.5		42.5	100		37		
I_{OH} Output drive current						No internal pull-up device							mA
I_{IH}, I_{IL} Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
	E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
I_{OH}, I_{OL}*** 3-state output leakage current	G, H types	0/18	18		18		2		10^{-4}	2		20	μA
	E, F types	0/15	15		15		2		10^{-4}	2		20	
C_I Input capacitance		Any input							5	7.5			pF
C_O Output capacitance		Any output							30				

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

** Measured with external pull-up resistor, $R_L = 10\ K\Omega$ to V_{DD}

*** Forced output disabled

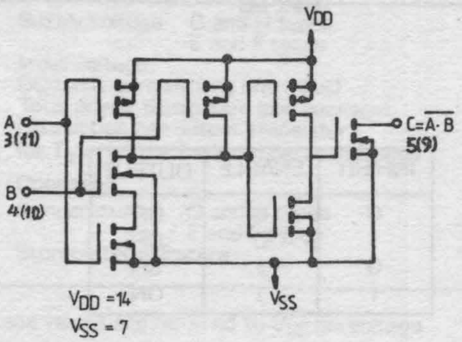
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time High-to-Low	R_L*=120 Ω	5 10 15		100 45 30	200 90 60	ns
	Low-to-High	R_L*=120 Ω	5 10 15		100 60 50	200 120 100	ns
t_{THL} t_{TLH}	Transition time High-to-Low	R_L*=120 Ω	5 10 15		50 20 10	100 40 20	ns
	Low-to-High	R_L*=120 Ω	5 10 15		50 35 25	100 70 50	ns

*R_L is external pull-up resistor to V_{DD}.

SCHEMATIC DIAGRAM AND TRUTH TABLE



TRUTH TABLE

A	B	C	
0	0	1*	Z#
1	0	1*	Z#
0	1	1*	Z#
1	1	0	

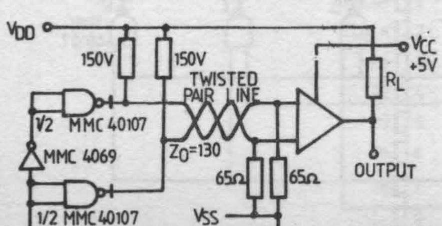
* Requires external pull-up resistor (R_L) to V_{DD}

Without pull-up resistor (3-state)

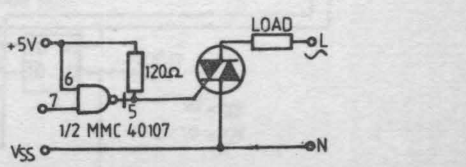
TYPICAL APPLICATIONS

The bar on the output line of this logic diagram indicates that the output is open drain as is shown in the previons schematic diagram and truth table.

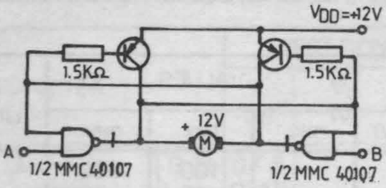
Line-driver circuit



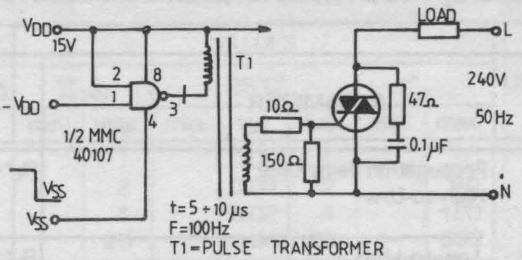
Direct dc drive interface of 40107 with a triac



Motor-controller circuit

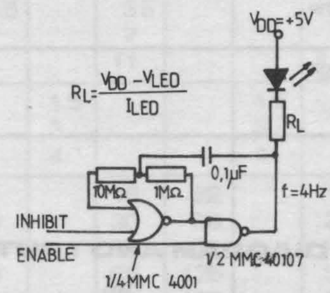


Interface of 40107 with triac whit COS/MOS component and triac isolated

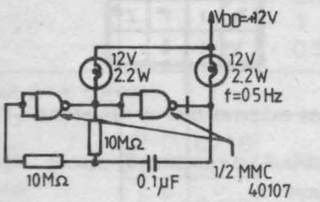


A	B	MOTOR FUNCTION
0	0	OFF
1	0	COUNTER CLOCKWISE
1	1	AS PREVIOUS STATE
0	1	CLOCKWISE
1	1	AS PREVIOUS STATE

LED driver circuit

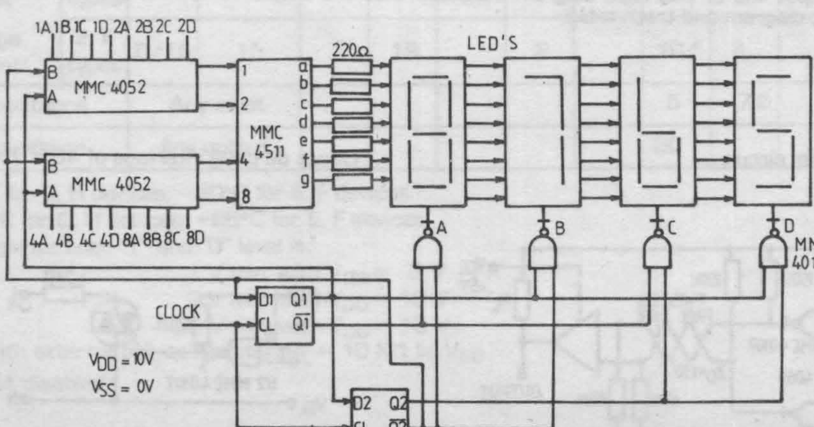


A 2.2 watt incandescent lamp-driver circuit



INHIBIT	ENABLE	OUTPUT
0	0	OFF
1	0	OFF
0	1	OFF
1	1	ON

Multiplexed LED circuit



SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

MMC 40160 - DECADE WITH ASYNCHRONOUS CLEAR
MMC 40161 - BINARY WITH ASYNCHRONOUS CLEAR
MMC 40162 - DECADE WITH SYNCHRONOUS CLEAR
MMC 40163 - BINARY WITH SYNCHRONOUS CLEAR

GENERAL DESCRIPTION

The MMC 40160, 40161, 40162, 40163 are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. MMC 40160, 40161, 40162 and 40163 are 4-bit synchronous programmable counters. The CLEAR function of the MMC 40162 and 40163 is synchronous and a low level at the CLEAR input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the MMC 40161 and 40160 is asynchronous and a low level at the CLEAR input sets all four outputs low regardless of the state of the CLOCK, LOAD, or ENABLE inputs. A low level at the LOAD input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (C_{OUT}). Counting is enable when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable succesive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

FEATURES

- INTERNAL LOOK-AHEAD FOR FAST COUNTING
- CARRY OUTPUT FOR CASCADING
- SYNCHRONOUSLY PROGRAMMABLE
- SYNCHRONOUS LOAD CONTROL INPUT
- LOW-POWER TTL COMPATIBILITY
- 5 V, 10 V AND 15 V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18 V AND 25°C FOR MMC G AND H DEVICES

ABSOLUTE MAXIMUM RATINGS

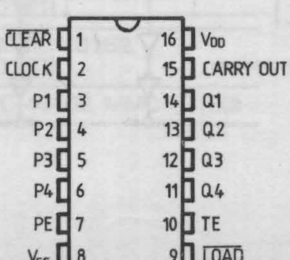
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

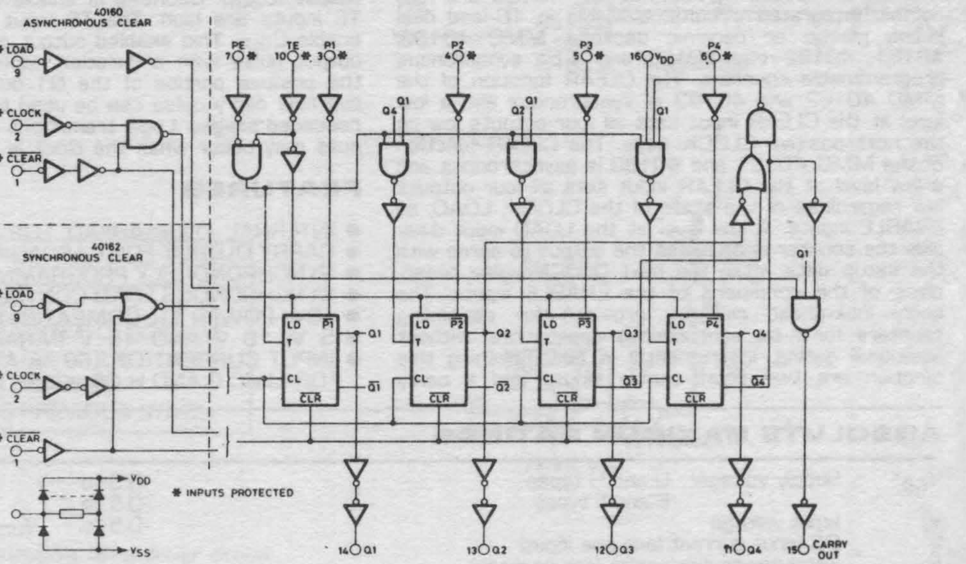
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

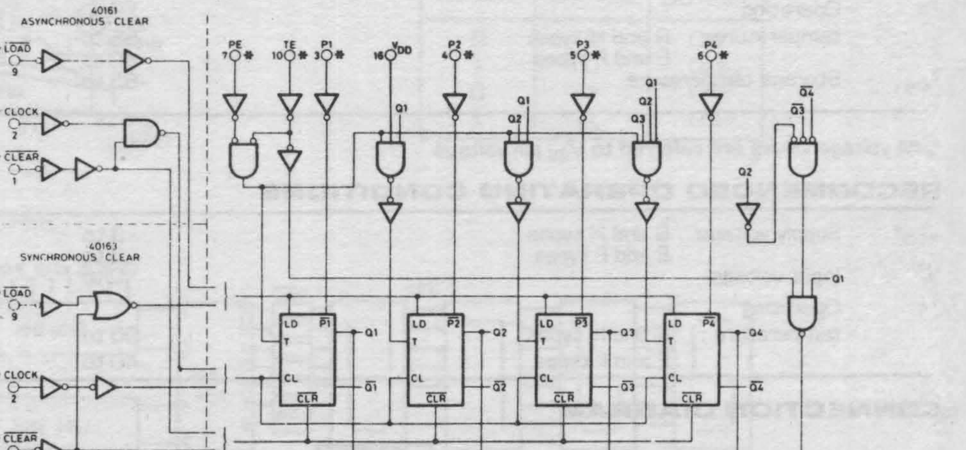


LOGIC DIAGRAMS

For **40160** and **40162** BCD decade counters.

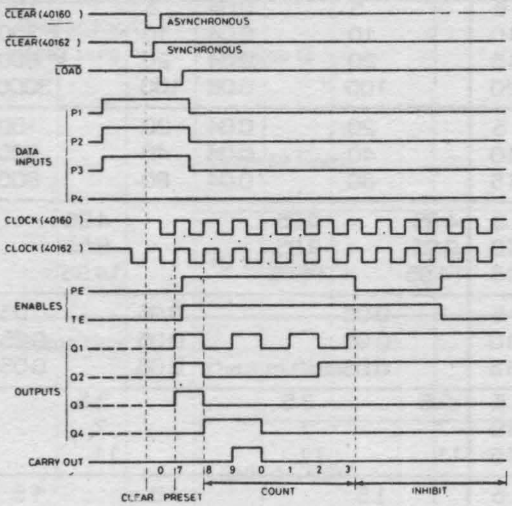


For **40161** and **40163** binary counters.

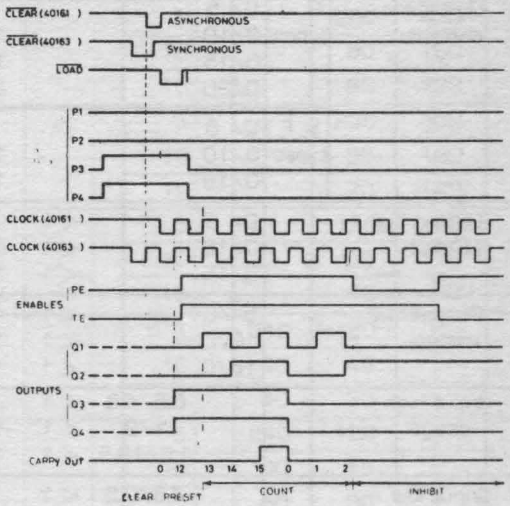


TIMING DIAGRAMS

for **40160** and **40162**



for **40161** and **40163**



TRUTH TABLE

CLOCK	CLR	LOAD	PE	TE	OPERATION
	1	0	x	x	PRESET
	1	1	0	x	NC
	1	1	x	0	NC
	1	1	1	1	COUNT
x	0	x	x	x	RESET (MMC 40160, MMC 40161)
	0	x	x	x	RESET (MMC 40162, MMC 40163)
	1	x	x	x	NC (MMC 40162, MMC 40163)

1 = HIGH LEVEL
0 = LOW LEVEL
x = DONT CARE
NC = NO CHANGE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

PARAMETER			TEST CONDITIONS V_{DD} (V)	VALUES Min.	Typ.	Max.	UNIT
CLOCK OPERATION							
t_{PHL}, t_{PLH}	Propagation delay time	Clock to Q	5		200	400	ns
			10		80	160	
			15		60	120	
		Clock to C_{OUT}	5		225	450	ns
			10		95	190	
			15		70	140	
		TE to C_{OUT}	5		125	250	ns
			10		55	110	
			15		40	80	
t_{setup}	Setup time	Data to Clock	5	240	120		ns
			10	90	45		
			15	60	30		
		Load to Clock	5	240	120		ns
			10	90	45		
			15	60	30		
		PE to TE to Clock	5	340	170		ns
			10	140	70		
			15	100	50		
t_{hold}	Hold time		5	0			ns
			10	0			
			15	0			
t_{THL}, t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Clock input pulse width		5	170	85		ns
			10	70	35		
			15	50	25		
f_{CL}	Maximum clock input freqiency		5	2	3		MHz
			10	5.5	8.5		
			15	8	12		
t_r, t_f	Clock input rise or fall time*		5			200	μs
			10			70	
			15			15	
CLEAR OPERATION							
t_{PHL}	Propagation delay time (MMC 40160, 40161) Clear to Q		5		250	500	ns
			10		110	220	
			15		80	160	

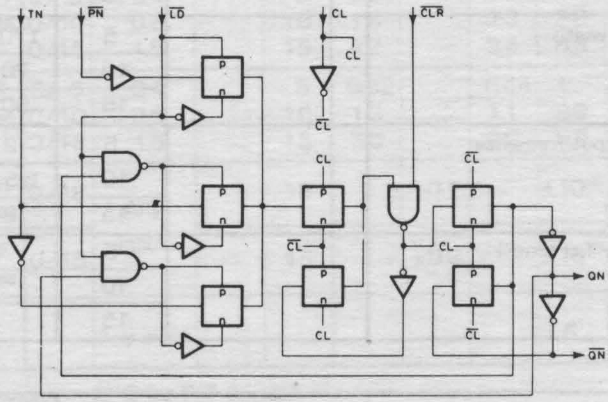
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

	PARAMETER	TEST CONDITIONS	VALUES				UNIT
			V_{DD} (V)	Min.	Typ.	Max.	
t_{setup}	Setup time (MMC 40162, 40163) Clear to clock		5	340	170		ns
			10	140	70		
			15	100	50		
t_{hold}	Hold time (MMC 40162, 40163) Clear to clock		5	0			ns
			10	0			
			15	0			
t_{rem}	Clear removal time (MMC 40160, 40161)		5	200	100		ns
			10	100	50		
			15	70	35		
t_w	Clear input pulse width Low level (MMC 40160, 40161)			170	85		ns
				70	35		
				50	25		

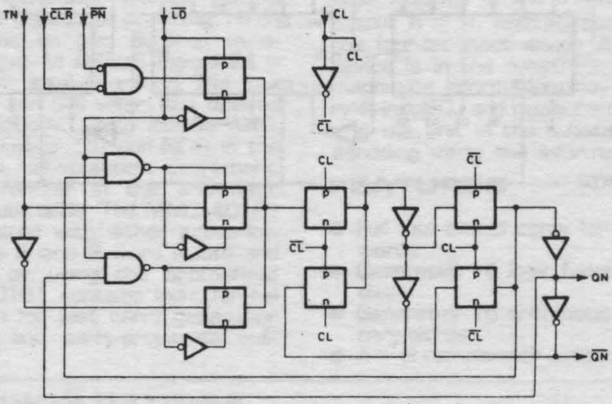
* If more than one unit is cascaded in the parallel clocked application, tr should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

TYPICAL APPLICATIONS

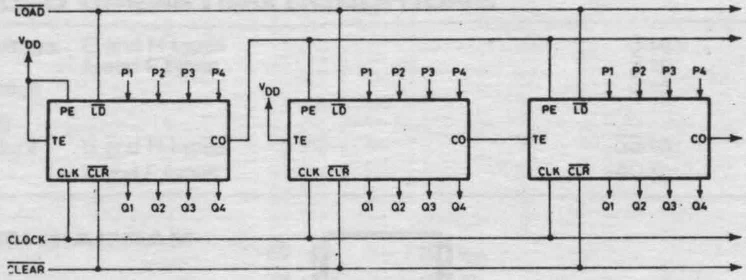
Detail of flip-flops for 40160 and 40161 (asynchronous clear)



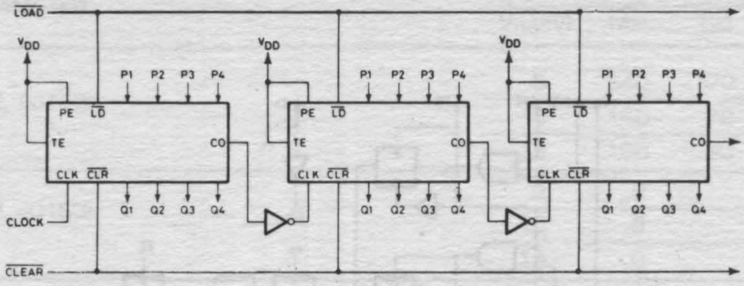
Detail of flip-flops for 40162 and 40163 (synchronous clear)



Cascaded counter packages in the parallel-clocked mode



Cascaded counter packages in the ripple-clocked mode.



4-BIT ARITHMETIC LOGIC UNIT

GENERAL DESCRIPTION

The MMC 40181 is a monolithic integrated circuit, available in 24-lead dual in-line plastic or ceramic package.
The MMC 40181 is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two Boolean variables. The mode control input M selects logical (M = High) or arithmetical (M = Low) operation. The four select inputs (S0, S1, S2 and S3) select the desired logical or arithmetical functions, which include AND, OR, NAND, NOR and exclusive -OR and-NOR in the logical mode, and addition, substraction, decrement, left-shift, and straight transfer in the arithmetic mode, according to the truth table. The MMC 40181 operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table. The MMC 40181 contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and $\overline{P}$ for the four bits of the MMC 40181. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance. Also included in the MMC 40181 is a comparator output A = B, which assumes a high level whenever the four-bit input words A and B are equal and the device is in the substract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the substract mode and externally decoding using the information in Table II.

FEATURES

- Full look-ahead carry for speed operations on long words
- Generates 16 logic functions of two boolean variables
- Generates 16 arithmetic functions of two 4-bit binary words
- A = B comparator output avaible

ABSOLUTE MAXIMUM RATINGS

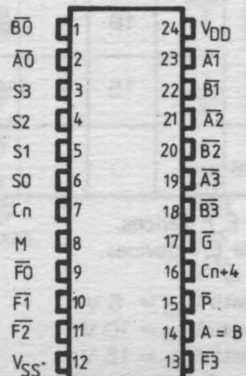
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

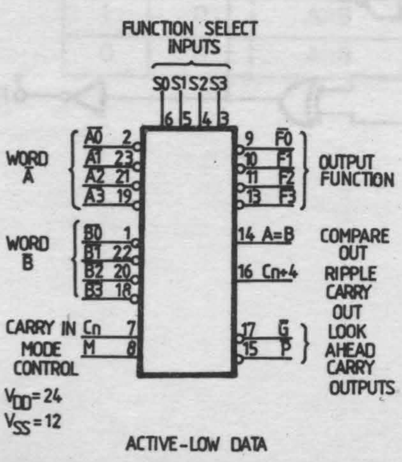
2.5 V min. with V_{DD} = 15 V

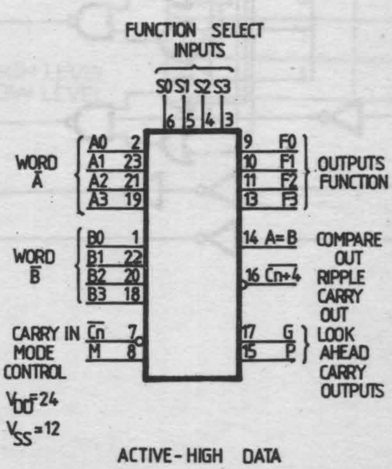
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ all input rise and fall times = 20 ns).

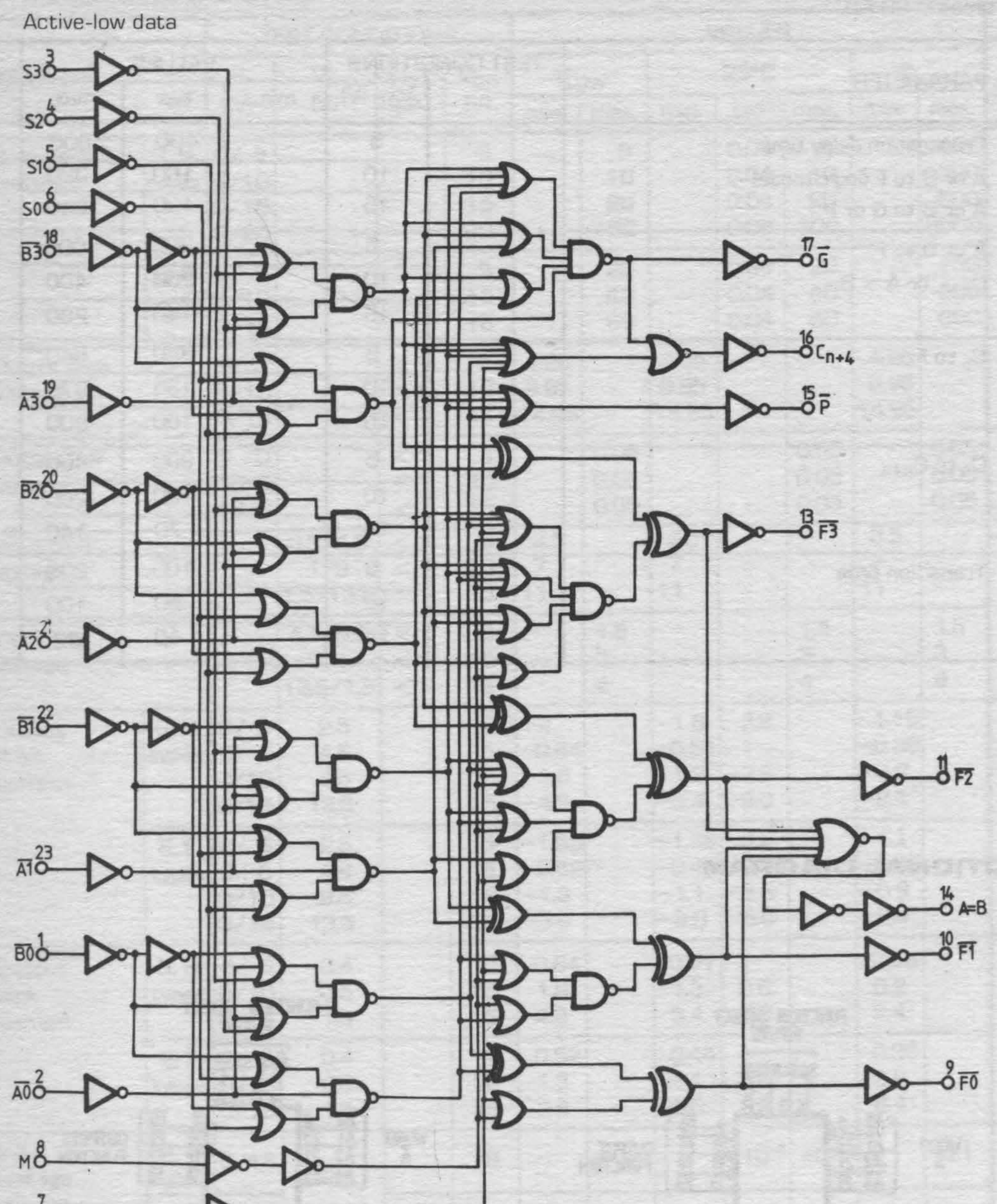
	PARAMETER	TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PLH} t_{PHL}	Propagation delay time A or B to F (logic mode) A or B to G or P		5		400	800	ns
			10		160	320	
			15		120	240	
	A or B to F, C_{n+4}, or A = B		5		300	1000	ns
			10		200	400	
			15		140	280	
	C_n to F		5		320	640	ns
			10		135	270	
			15		100	200	
	C_n to C_{n+4}		5		200	400	ns
			10		100	200	
			15		70	140	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	

FUNCTIONAL DIAGRAM





LOGIC DIAGRAM



TRUTH TABLES Table I

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
S3	S2	S1	S0	LOGIC FUNCTION (M=H)	ARITHMETIC* FUNCTION ($M=L$, $C_n=L$)	LOGIC FUNCTION (M=H)	ARITHMETIC* FUNCTION ($M=L$, $\overline{C}_n=H$)
0	0	0	0	$\overline{A}$	A minus 1	$\overline{A}$	A
0	0	0	1	$\overline{AB}$	AB minus 1	$\overline{A+B}$	$A+B$
0	0	1	0	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
0	0	1	1	Logic 1	minus 1	Logic 0	minus 1
0	1	0	0	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
0	1	0	1	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
0	1	1	0	$\overline{A\oplus B}$	A minus B minus 1	$A\oplus B$	A minus B minus 1
0	1	1	1	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
1	0	0	0	$\overline{A}B$	A plus $(A+B)$	$\overline{A}+B$	A plus AB
1	0	0	1	$A\oplus B$	A plus B	$\overline{A\oplus B}$	A plus B
1	0	1	0	B	$A\overline{B}$ plus $(A+B)$	B	$(A+\overline{B})$ plus AB
1	0	1	1	$A+B$	$A+B$	AB	AB minus 1
1	1	0	0	Logic 0	A plus A	Logic 1	A plus A
1	1	0	1	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
1	1	1	0	AB	$A\overline{B}$ plus A	$A+B$	$(A+\overline{B})$ plus A
1	1	1	1	A	A	A	A minus 1

* Expressed as two's complement. For arithmetic function with C_n in opposite state, the resulting function is as shown plus 1.

Table II — MAGNITUDE COMPARISON

Active-High data

INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
1	1	$A \leq B$
0	1	$A < B$
1	0	$A > B$
0	0	$A \geq B$

Active-Low data

INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
0	0	$A \leq B$
1	0	$A < B$
0	1	$A > B$
1	1	$A \geq B$

1 = HIGH LEVEL
0 = LOW LEVEL

Table III — **AC TEST SETUP REFERENCE (active-low data)**

TEST DELAY TIMES		AC PATHS		DC DATA INPUTS		MODE*
		INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}	
SUM_{IN}	to SUM_{OUT}	$\overline{B0}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All $\overline{A}$'s	ADD
SUM_{IN}	to P	$\overline{A0}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All $\overline{B}$'s	ADD
SUM_{IN}	to G	$\overline{B0}$	$\overline{G}$	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN}	to C_{n+4}	$\overline{B0}$	C_{n+4}	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n	to SUM_{OUT}	C_n	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
C_n	to C_{n+4}	C_n	C_{n+4}	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
SUM_{IN}	to A=B	$\overline{B0}$	A=B	All As, B1, B2, B3, M	C_n	SUBSTRACT
SUM_{IN}	to SUM_{OUT} (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All A's, C_n	M	EXCLUSIVE OR

* ADD Mode: S0, S3 = V_{DD}; S1, S2 = V_{SS}. SUBSTRACT Mode: S0, S3 = V_{SS}; S1, S2 = V_{DD}.

PRESETTABLE UP/DOWN COUNTERS (DUAL CLOCK WITH RESET) 40192-BCD TYPE 40193-BINARY TYPE

GENERAL DESCRIPTION

The MMC 40192, MMC 40193 are monolithic integrated circuits processed in standard Al-gate technology. The MMC 40192 is a 4-Bit Synchronous Up/Down Decade Counter and the MMC 40193 is a 4-Bit Synchronous Up/Down Binary Counter. Counting up and counting down is performed by two count inputs (CLOCK UP and CLOCK DOWN respectively), one being held high while the other is clocked. The outputs (Q_1—Q_4) change on the positive-going transition of this clock. These counters feature preset inputs (J_1—J_4) that are enabled when load ($\overline{\text{PRESET ENABLE}}$) is a logical „0" and a clear (RESET) which forces all outputs to „0" when it is at logical „1". The counters also have CARRY and BORROW inputs so that they can be cascaded using no external circuitry.

FEATURES

- Individual clock lines for counting up or counting down
- Synchronous high-speed carry and borrow propagation delays for cascading
- Active low parallel load
- Active high asynchronous reset
- Quiescent current specified at 20 V
- 5 V, 10 V, 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

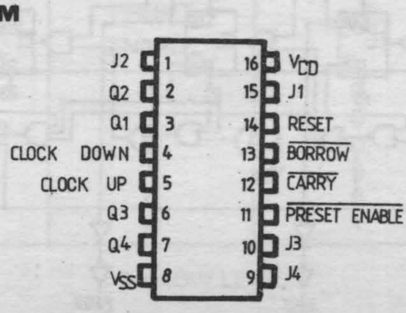
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

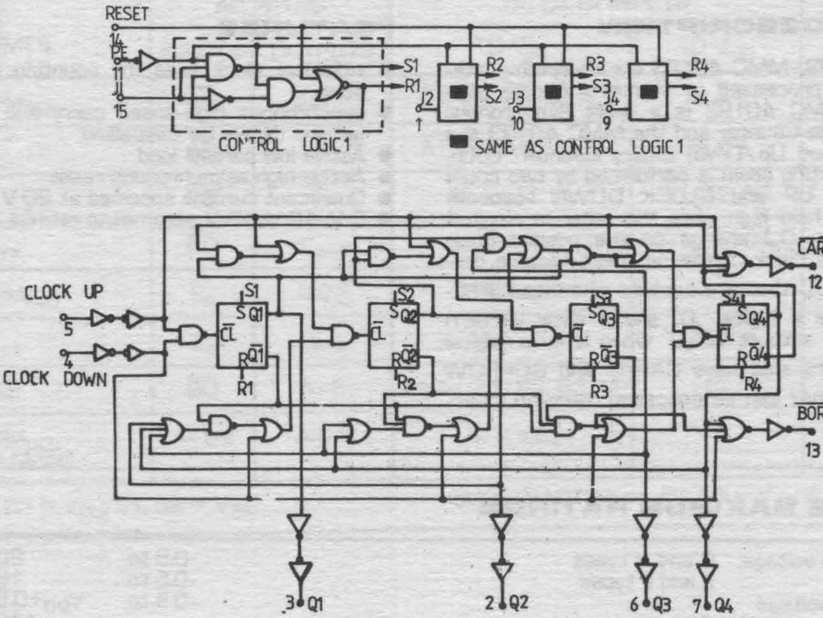
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

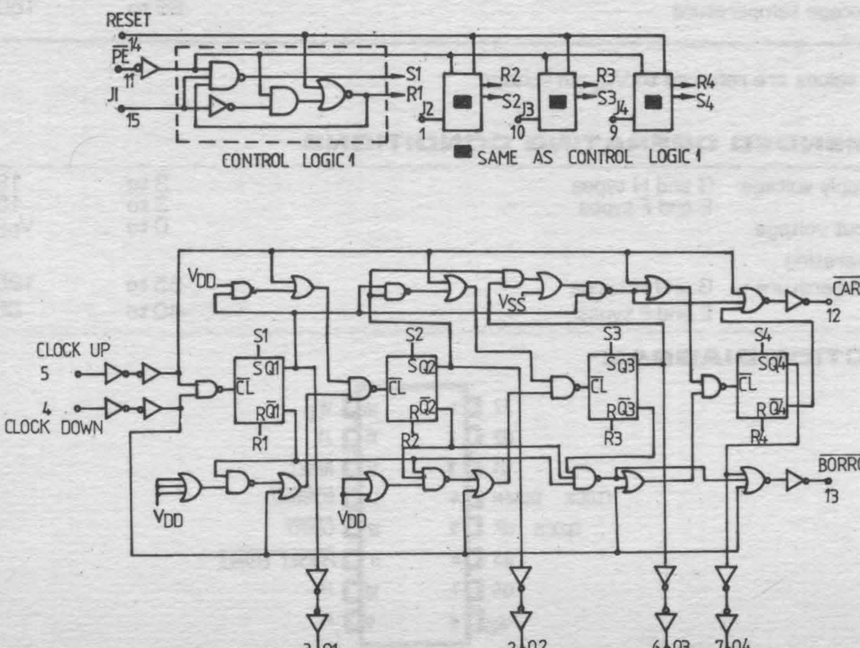


LOGIC DIAGRAM

MMC 40192

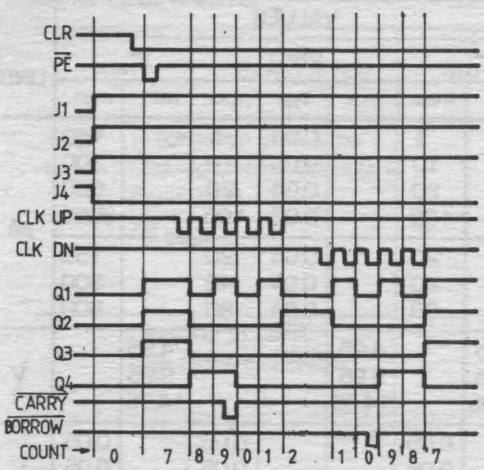


MMC 40193

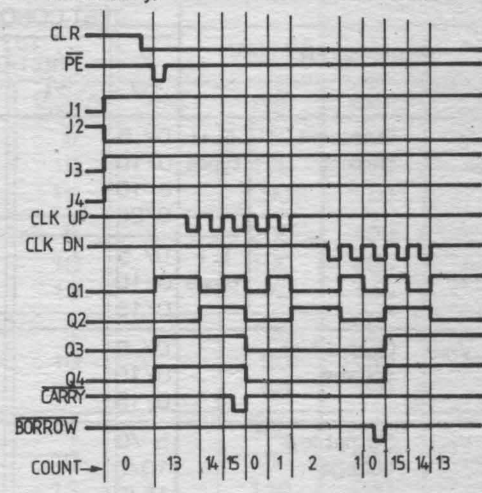


TIMING DIAGRAM

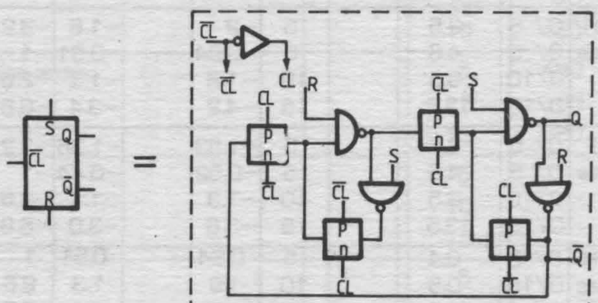
40192 (BCD)



40193 (Binary)



Internal logic of flip-flop



TRUTH TABLE

CLOCK UP	CLOCK DOWN	PRESET ENABLE	RESET	ACTION
	1	1	0	COUNT UP
	1	1	0	NO COUNT
1		1	0	COUNT DOWN
1		1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL   0 = LOW LEVEL   X = DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

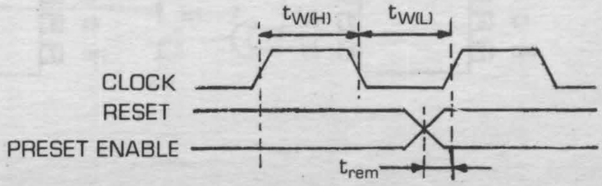
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	min.	typ.	max.	
t_{PHL},	Propagation delay time		5		250	500	
t_{PLH}	Clok Up or Clok Down to Q		10		120	240	ns
	Reset to Q		15		90	180	
	$\overline{PE}$ to Q		5		200	400	
			10		100	200	ns
			15		70	140	
	Clock Up to $\overline{Carry}$		5		160	320	
	Clok Down to $\overline{Borrow}$		10		80	160	ns
			15		60	120	
	$\overline{Reset}$ or $\overline{PE}$ to $\overline{Borrow}$ or $\overline{Carry}$		5		300	600	
			10		150	300	ns
			15		110	220	
t_{THL},	Transition time		5		100	200	
t_{TLH}			10		50	100	ns
			15		40	80	
t_{rem}*	Removal time		5	80	40		
	Reset or $\overline{PE}$		10	40	20		ns
			15	30	15		
t_W	Clock input pulse width		5	480	240		
	Reset		10	300	150		ns
			15	260	130		
	$\overline{PE}$		5		120	240	
			10		85	170	ns
			15		70	140	
	Clock		5		90	180	
			10		45	90	ns
			15		30	60	
t_r, t_f	Clock input rise or fall time		5			15	
			10			15	μs
			15			5	
t_{CL}	Maximum clock input frequency		5	2	4		
			10	4	8		MHz
			15	5.5	11		

* The time required for Reset or Preset Enable control to be removed before clocking (see timing diagram).

Timing diagram defining trem



QUAD TRI-STATE BUS TRANSCEIVER

GENERAL DESCRIPTION

The MMC 40243 and MMC 40943 are monolithic integrated circuits available in 14-lead dual in-line plastic or ceramic package, fabricated with standard Al-gate CMOS technology. The MMC 40243 consist of a quad 3-state bus trasceiver, with high output current sink and source capability. It has 2 control signals DEa/ and OEb. The MMC 40943 consist of a quad 3-state bus transceiver TTL to CMOS with high output current sink and source capability. It has 3 power supply V_{DD}, V_{SS}, V_{CC}, and 2 control signals.

FEATURES

- Wide supply voltage range 3.0 V_{DC} to 18V_{DC}
- Bidirectional inputs-outputs.
- 1 TTL load capability.
- Non-inverting tri-state outputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

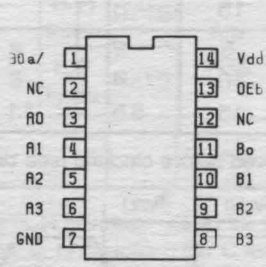
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

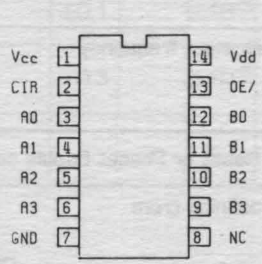
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTIONS DIAGRAMS

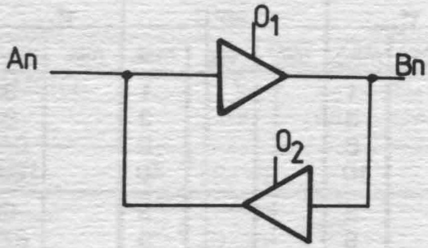
MMC 40243

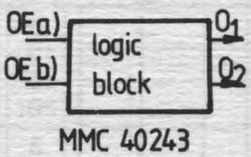


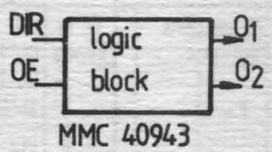
MMC 40943



FUNCTIONAL DIAGRAMS







TRUTH TABLES

MMC 40243

INPUTS		INPUTS/OUTPUTS	
OE_a	OE_b	A_n	B_n
L	L	inputs	B = A
H	L	Z	Z
L	H	Z	Z
H	H	A = B	inputs

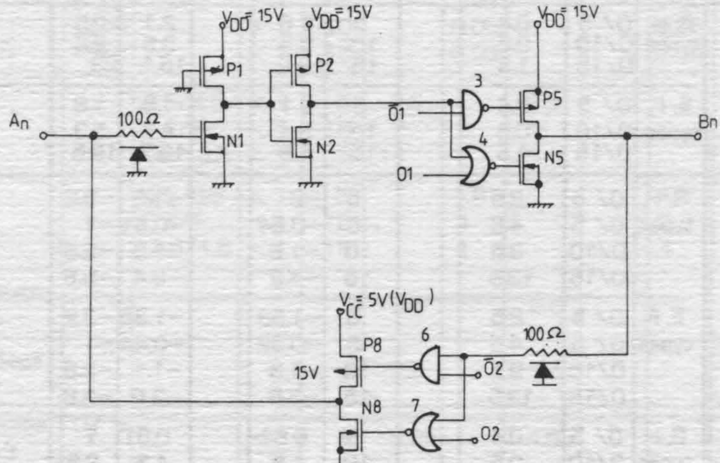
Z = high impedance

MMC 40943

INPUTS		INPUTS/OUTPUTS	
OE	DIR	A_n	B_n
L	L	$A_n = B_n$	inputs
L	H	inputs	$A_n = B_n$
H	X	Z	Z

Z = high impedance

SCHEMATIC DIAGRAMS



STATIC ELECTRICAL CHARACTERISTICS
(over recommended operating conditions)

MMC 40243

	PARAMETER		TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1			1		30	μA
			0/10			10		3			3		90	
			0/15			15		8			8		240	
			0/20			20		40			40		1200	
		E, F types	0/ 5			5		3			3		90	
			0/10			10		9			9		270	
			0/15			15		24			24		720	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current outputs AØ—A3	G, H types	0/ 5	2.5		5	-5.8		-4.8	-6.1		-3		mA
			0/ 5	4.6		5	-1.2		-1.02	-1.9		-0.7		
			0/10	9.5		10	-3.1		-2.6	-3.7		-1.8		
			0/15	13.5		15	-8.2		-6.8	-14.1		-4.8		
		E, F types	0/ 5	2.5		5	-4.8		-4.1	-5.2		-2.9		
			0/ 5	4.6		5	-1		-0.8	-1.6		-0.6		
			0/10	9.5		10	-2.5		-2.2	-3.1		-1.6		
			0/15	13.5		15	-6.8		-5.8	-11.9		-4.2		
I_{OL}	Output sink current outputs AØ—A3	G, H types	0/ 5	0.4		5	2.6		2.1	2.3		1.3		mA
			0/10	0.5		10	6.5		5.5	2.6		3.8		
			0/15	1.5		15	19.2		16.1	23		11.2		
		E, F types	0/ 5	0.4		5	2.1		1.8	1.9		1.2		
			0/10	0.5		10	5.4		4.7	5.3		3.3		
			0/15	1.5		15	1.6		13.7	19.5		9.7		
I_{OH}	Output drive current output BØ—B3	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current output BØ—B3	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm10^{-4}$	±1.0		±7.5	
C_I	—Input capacitance			Any input						5	7.5			pF

MMC 40943

PARAMETER			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1			1		30	mA
			0/10			10		3			3		90	
			0/15			15		8			8		240	
			0/20			20		40			40		1200	
		E, F types	0/ 5			5		3			3		90	
			0/10			10		9			9		270	
			0/15			15		24			24		720	
V_{OH}	Output high voltage outputs BØ—B3		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage outputs BØ—B3		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage inputs BØ—B3			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage inputs BØ—B3			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
V_{IH}	Input high voltage inputs AØ—A3						2.8		2.8			2.8		V
V_{IL}	Input low voltage inputs AØ—A3						1.5		1.5			2.8		V
V_{OH}	Output high voltage outputs AØ—A3		0/ 5		< 1	5	4.95		4.95			4.95		V
V_{OL}	Output low voltage outputs AØ—A3		5 /0		< 1	5		0.05			0.05		0.05	V

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS					VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
		G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm10^{-4}$	±1.0		±7.5	
C_I	Input capacitance			Any input							40			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

MMC 40906 HEX OPEN DRAIN N - CHANNEL BUFFERS

MMC 40907 HEX OPEN DRAIN P - CHANNEL BUFFERS

GENERAL DESCRIPTION

The MMC 40906 and the MMC 40907 are monolithic integrated circuits processed in standard Al-gate CMOS technology. The MMC 40906 and the MMC 40907 are six inverters driving six N-channel devices and six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors.

FEATURES

- Wide supply voltage range 3,0 V to 15 V
- Guaranted noise margin 1,0 V
- High noise immunity 0,45 V_{CC} typ
- High current sourcing and sinking open drain outputs

ABSOLUTE MAXIMUM RATINGS

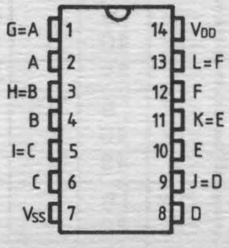
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

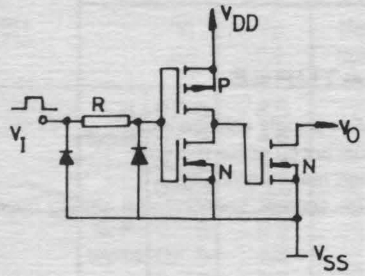
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

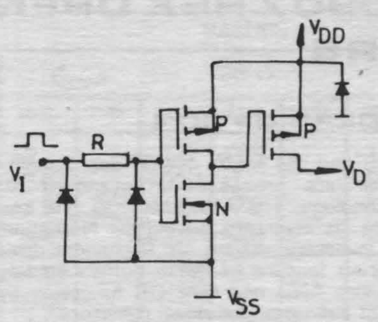


SCHEMATIC DIAGRAM

MMC 40906



MMC 40907



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_{OH}	Output drive current	G, H types	0/ 5	2.5	5	1.6		-1.25	-6.4		-0.9		mA
			0/ 5	4.6	5	0.64		-0.51	-1.6		-0.36		
			0/10	9.5	10	1.6		-1.30	-3.6		-0.9		
			0/15	13.5	15	4.7		-3.75	-12		-2.6		
		E, F types	0/ 5	2.5	5	1.5		-1.25	-6.4		-1		
			0/ 5	4.6	5	0.61		-0.51	-1.6		-0.42		
			0/10	9.5	10	1.5		-1.25	-3.6		-1		
			0/15	13.5	15	4.5		-3.75	-12		-3		
I_{OL}	Output sink current	G, H types	0/ 5	0.4	5	3.75		3.2	6.4		2.2		
			0/10	0.5	10	10		8	16		5.6		
			0/15	1.5	15	30		24	48		17		
		E, F types	0/ 5	0.4	5	3.6		3.2	6.4		2.6		
			0/10	0.5	10	9.6		8	16		6.6		
			0/15	1.5	15	28		24	48		19		
I_{IH},I_{IL}	Input leakage current	G, H types	0/18		18		±0.1		$\pm10^{-5}$	±0.1		±1	µA
		E, F types	0/15		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H device: $-40°C$ for E, F device

* $T_{HIGH} = +125°C$ for G, H device: $+85°C$ for E, F device

The noise margin for both „1" and „0" level is:

1V min. with $V_{DD} = 5V$
2V min. with $V_{DD} = 10V$
2.5V min. with $V_{DD} = 15V$

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_{amb} = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS VI (V)	VDD (V)	VALUES min.	typ.	max.	UNIT
t_{PLH}	Propagation delay time	5	5		70	140	ns
		10	10		40	80	
		10	5		45	90	
		15	15		30	60	
		15	5		40	80	
t_{PHL}	Propagation delay time	5	5		55	110	ns
		10	10		22	55	
		10	5		50	100	
		15	15		15	30	
		15	5		50	100	
t_{TLH}	Transition time	5	5		80	160	ns
		10	10		40	80	
		15	15		30	60	
t_{THL}	Transition time	5	5		30	60	ns
		10	5		20	40	
		15	15		15	30	

± 3 DIGIT A/D CONVERTER

GENERAL DESCRIPTION

The MMC 130 combines both the analog and digital subsystems of a 3 digit A/D system în a single monolithic CMOS I.C. The „Quantized Feedbak" conversion scheme, provides the MMC 130 with an Auto-Zero Autopolarity A/D system requiring only a single reference voltage. External parts are minimized by the on-chip resistors and buffer amplifiers. These high impedance input and reference buffer amplifiers eliminate source loading errors providing the outstanding temperature coefficient and ratio operation inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The MMC 130 3 digit A/D is made functionally complete by the following additions:

1. C_{AZ} (0.10 µF) between AZ and pins
2. C_{INT} (0.033 µF) between INT and pins
3. C_{OSC} (0.001 µF) between OSC and Digital Ground
4. $V_{REF} \cong 2.000$ V
5. ± 5 V supplies (at 3 mA)

FEATURES

- Accuracy of 0.1% ± 1 Count For Full Use of 3 Digits
- Low Power Consumption of 25 mW
- Minimum External Parts Count
- Auto-Zero and Auto. — Polarity
- Buffered Signal and Reference Inputs $Z_{IN} > 10^9 \Omega$
- Internal Oscillator Uses Only One External Capacitor
- Wide Sampling Range of 1 to 60/Second
- Multiplexed BCD Output For Simple Display and µ-P Interface

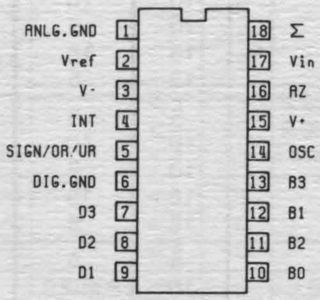
APPLICATIONS

- Digital Voltmeters, Panel Meters
- Digital Thermometers
- General Instrumentation (Noise, Light, pH, etc.)
- Microprocesor Interfaces to Analog Signals

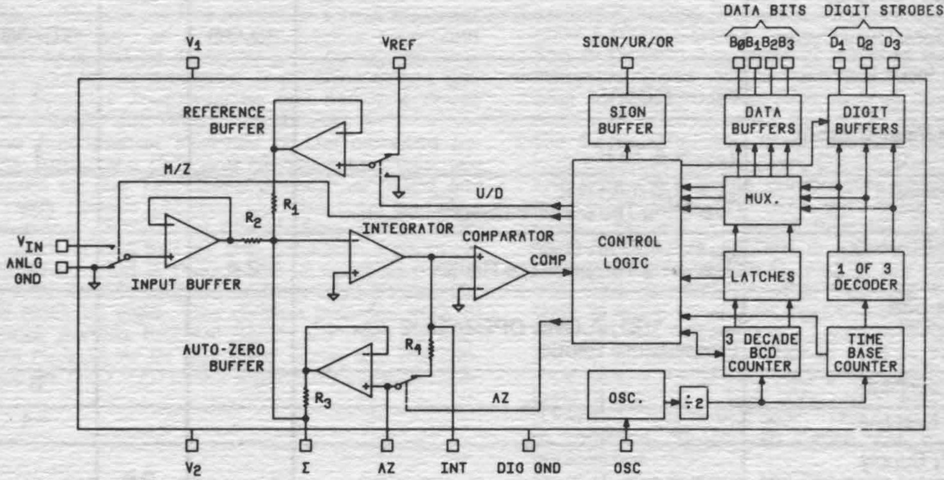
ABSOLUTES MAXIMUM RATINGS

V_{IN}	$V_1 + 0.3$ V, $V_2 - 0.3$ V
V_1V_2	16 V
V_1	8 V
Current at V_{IN}	1 mA
Voltage on any pin	$V_1 + 0.3$ V, $V_2 - 0.3$ V
V_{REF}	V_1
Operating Temperature (B)	0 to 70° C
Operating temperature (CD)	−20 to +85° C
Storage Temperature	−65 to 125° C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

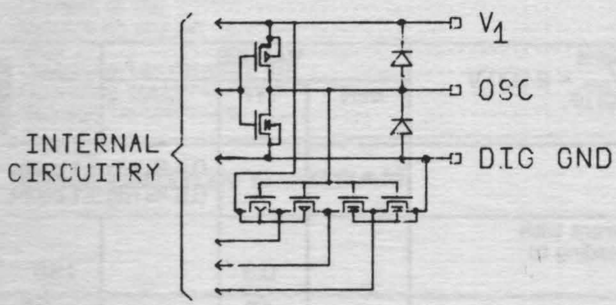
All DC parameters are 100% tested at 25° C. Lots are sample tested for AC parameters and High Temperature Limits to assure conformance with specifications.

PARAMETER	Test conditions $V_1 = +5$ V, $V_2 = -0$V, $V_{REF} = 2.000$ V $T_A = 25°$ C, $C_{INT} = 0.033$ µF, $C_{strg} = 0.1$ µF	VALUES MIN	TYP	MAX	UNIT
Nonlinearity	MMC 130.1 MMC 130			0.1 % rdg ±1 count 0.5 % rdg ±1 count	
Noise	Peak-to-Peak noise apparent with going from one steady reading to another		0.3		LSB
Gain T.C.	$0 < T_A < 70°$		10		µV/°C
Zero T.C.	$0 < T_A < 70°$ C		15		ppM/°C
NMR Normal Mode Rejection	$f_{series} = 60$ Hz, $f_{osc} = 24$ kHz	36			dB
I_{IN} V_{IN} Input Bias Current	$T_A = 25°$ C		7		pA
	$T_A = 70°$C		90		pA
	$T_A = 85°$ C(CD Only)			1	nA
I_{REF} V_{REF} input Bias Current	$T_A = 25°$ C		7		pA
	$T_A = 70°$ C		90		pA
	$T_A = 85°$ C (CD Only)			1	nA
I_{AZ} AZ Input Bias Current	$T_A = 85°$ C (CD Only) $V_{AZ} = -1$V			1	nA

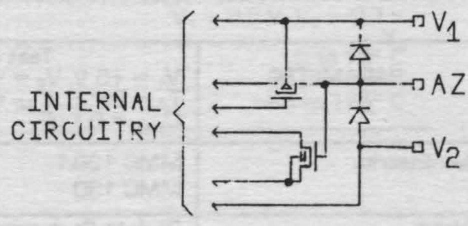
PARAMETER	Test conditions $V_1 = +5$ V, $V_2 = -0$V, $V_{REF} = 2.000$ V $T_A = 25°$ C, $C_{INT} = 0.033$ μF, $C_{strg} = 0.1$ μF	VALUES MIN	TYP	MAX	UNIT
f_{CLK} Clock Frequency			30		kHz
$D.C._{CLK}$ Clock Duty Cycle		30/70		70/30	%
I_{INL} Clock Input Current Low	$V_{INL} = 0.25$ V			1	mA
I_{INH} Clock Input Current High	$V_{INH} = 4.75$ V			1	mA
V_{OL} All Outputs	$I_{OL} = 1.6$ mA Over Operating Temperture Range			0.5	V
V_{OH} Digit Strobes	$I_{OH} = -400$ μA Over Operating Temperature Range	2.4			V
V_{OH} Data-Bits Sign/UR/OR	$I_{OH} = -100$ μA Over OPERATING Temperature Range	2.4			V
I_1 Supply current				6	mA
I_2 Supply Current				−4	mA
$PSRR_1$ V_1 Supply Rejection			0.6		mV/V
$PSRR_2$ V_2 Supply Rejection			1.4		mV/V

Typical Values are for Design Aid Only, and not subject to production testing

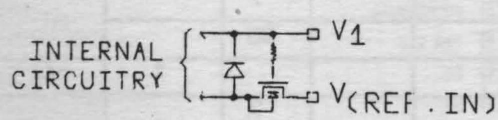
INPUT/OUTPUT SCHEMATICS

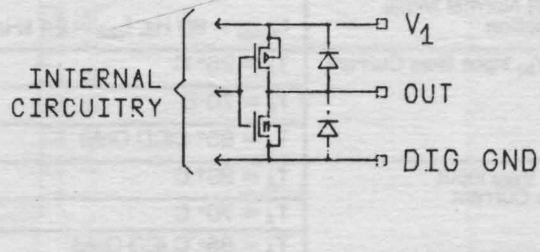


OSCILLATOR INPUT



AZ INPUT





V_{IN} OR V_{REF} INPUT

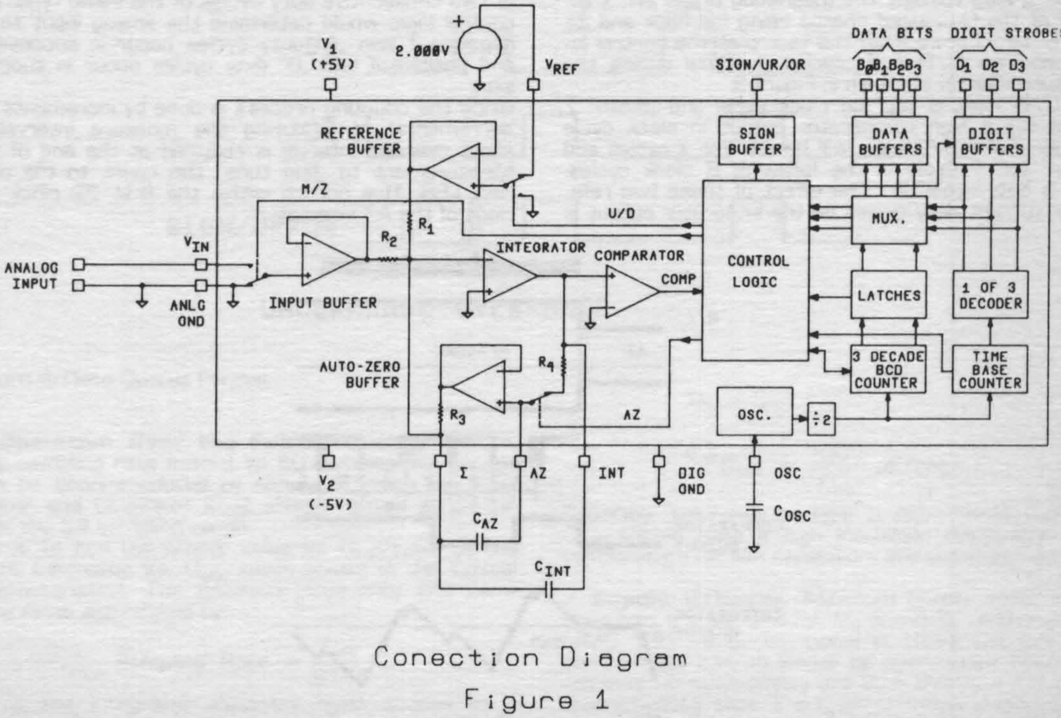
OUTPUT BUFFERS (Digits, Bits, SIGN/UR/OR)

FUNCTIONAL OPERATION

The Connection Diagram of Figure 1 should be referred to along with the timing diagrams of Figures 2,3 and 4 in this discussion of functional operation.
Time Base Counter — The oscillator circuit becomes fully functional with an external capacitor to ground. The OSC input can be driven by an external oscillator (0 to V_1 logic levels) if desired. A squaring circuit divides the oscillator frequency by two before it drives the BCD counter and Time-Base counter.
The two fundamental intervals of the sampling period, the Auto-Zero (AZ) and Measure intervals, are established by the Time-Base counter as 1024 and 2048 clock periods respectively. The total sampling interval is then 3072 clock periods long. Since the internal clock is one-half of the oscillator frequency., the sampling period is then 6144 (2 x 3072) oscillator periods. The Time-Base counter also divides the internal clock by eight. This division provides sets of eight clock periods (octets) which are used by both the data multiplexer as digit „ON" times and the control logic as U/D (Up/Down logic) duty cycle periods.

AUTO-ZERO INTERVAL

The Auto-Zero interval provides a means to null out the offset voltages of the amplifiers used in the MMC 130. In addition, it automatically establishes a second tracking reference voltage necessary for bipolar A/D conversion.
The Auto-Zero sequence is initiated when the M/Z (Measure/Zero) signal switches the input buffer amp to analog ground. After a brief count-correcting override period, the AZ switch is closed connecting the AZ amplifier and integrator together in a closed-loop second-order system. During this time the control logic ignores the comparator output and pulses the U/D switch at a 50% duty cycle of 4 clock periods „Up" and 4 „Down" (see fig. 2) Equilibrium of this closed-loops system is attained when the average currents through R_1 and R_3 are equal and opposite. This is achieved when V_{AZ}, the Auto-Zero voltage, is equal to $-1/2\ V_{REF}$ since $R_1 = R_3$. Establishing V_{AZ} and storing it on C_{AZ} gives V/D logic the capability of switching either a + or — reference current to the integrator during conversion. Thus when U/D is „Up", $I_1 + I_3 = -V_{REF}/2R_1$ and when U/D is „Down", $I_1 + I_3 = V_{ref}\ 32R_1$. The Auto-Zero interval is of sufficient duration to insure that V_{AZ} will be well established.
Prior to the start of the Measure interval, the integrator output (which had been cycling around — 1V) is brought back to analog ground, the comparator threshold. The system is now ready for a conversion.



Conection Diagram

Figure 1

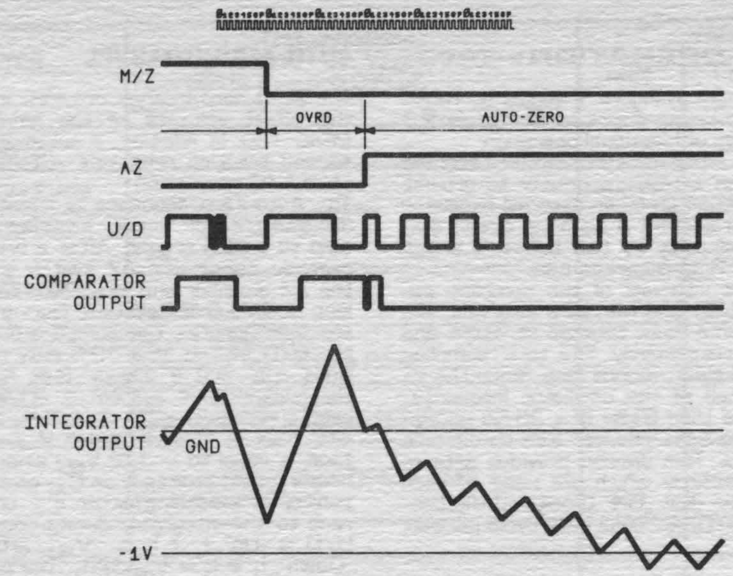


Figure 2 Auto-Zero Timing

MEASUREMENT INTERVAL

The „Quantized Feedback" conversion syzstem is characterized by a single phase Digitization interval is which a digital control system feeds back quantized units of charge in response to the sampled state of an analog comparator. These quanta of charge balance the charge being supplied to the integrator by the analog voltage. The magnitude ($V_{REF}/2R_1 \times 6/f_{clock}$) of the Quantized charge being fed back and its sign (+ or −) arise from the fact that the control logic has two U/D duty cycles available during the Measure interval al shown in Figure 3.

The U/D logic is „up" on clock cycle and „down" 7 cycles for a high comparator output in clock cycle number 7 the U/D logic will be „up" for 7 cycles and „down" for 1 cycle in the following 8 clock cycles. This is duty cycle „B". The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the „up" state of the U/D logic drives the integrator output voltage up. The up/down BCD counter increments by each clock pulse when the U/D logic is „down". Consequently the net count goes up 6 counts for a „B" duty cycle and down 6 for an „A" duty cycle.

Input polarity is determined by the first appearance of two consecutive duty cycles of the same type. The control logic would determine the analog input to be negative if two „A" duty cycles occur in succession and positive if two „B" duty cycles occur in succession.

Since the counting process is done by increments (or decrements) of 6 during the measure interval, a short override interval is required at the end of the Measurement to „fine tune" the count to the nearest LSB. This occurs within the first 32 clock periods of the AZ interval

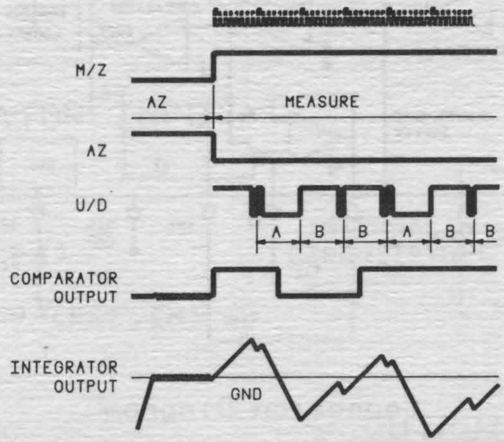


Figure 3 Measure Interval Timing

Following the count correcting override sequence; the contents of the BCD counters an sign flip-flop are loaded into the internal latches. Counter states of less than 80 or greater than 999 are decoded as underrange or overrange conditions respectively. The presence of an out-of-range signal gates a single pulse (one clock period) to the SIGN/UR/OR output during either D_1 or D_2 digit time (D_2 identifies overrange, D_1 identifies underrange). The overrange condition also provides a visual signal by holding the digit strobe outputs low during the Measure interval. This holds the display off for 2/3 of the sampling interval giving a blinking effect.

The BCD data stored in the latches is continuously scanned, every 24 clock periods (8 clock times per digit). Sign information appears at the SIGN/UR/OR pin coincident with the D_3 strobe. Interdigit blanking of the Digit Strobes is achieved by taking on full clock period from both the leading and trailing edges of the strobes. Thus the digit is on 6 clock periods while the BCD data for that digit appears for the full eight clock periods. Figure 4 shows the Data Output Timing.

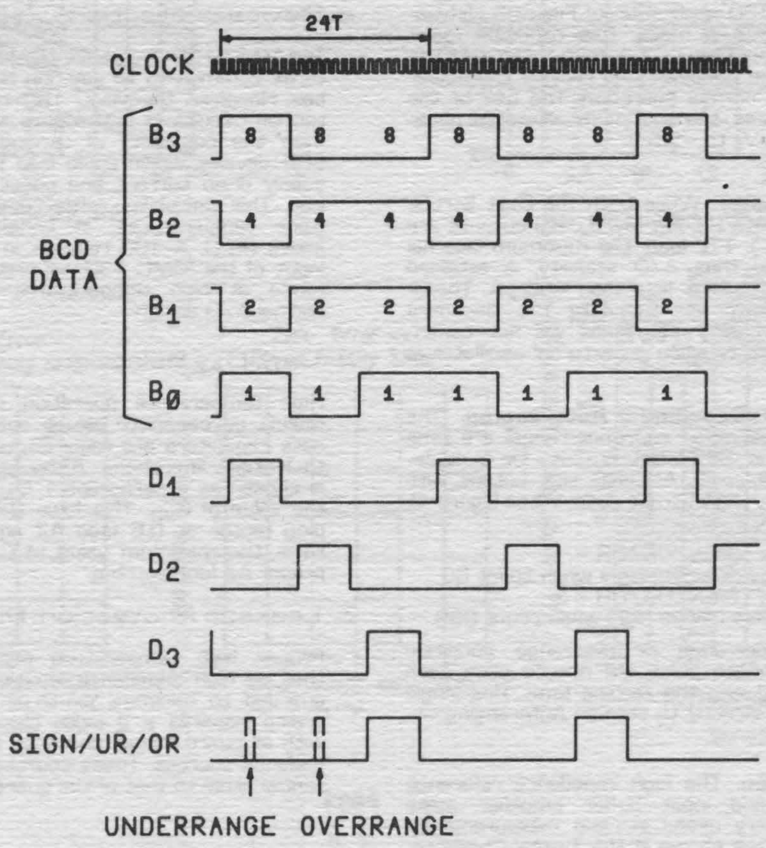


Figure 4. Data Output Format

1. **Operation Over the Full Frequency Range.** Any sampling rate from 1 to 60 samples per second can be accommodated by simply changing the integrator and Oscillator (C_{AZ}) should remain at o.1 µF over the full sampling range.

a. To find the proper value for C_{osc} refer to the clock frequency Vs. C_{osc} curve shown in the Typical Characteristics. The oscillator frequency and sampling rates are related by:

$$\text{Sampling Rate} = \frac{f_{osc}}{6144}$$

b. The integrator capacitor must change as a function of frequency by means of the following relationship:

$$C_{INT} = \frac{1000}{f_{osc}} \ \mu F/sec$$

Capacitor tolerance or type is not critical. C_{AZ} and C_{INT} should have a high insulation resistance over temperature (all film capacitors are suitable).

2. **Supply Voltages.** Minimum supply voltages for operation are $V_1 = 4.3V$, $V_2 = -4.3V$. Although the MMC 130 will be functional at these voltages, TTL compatibility can no longer be guaranteed. Maximum voltages for functionality are $V_1 = 8V$, $V_2 = -8V$. It is recommended that a o.1 µF or larger capacitor be used to bypass V_1 to ground at the MMC 130 when LED display are used.

3. **Input Prorection.** The MMC 130 has protection circuitry at all inputs and outputs which prevent static damage by clamping the voltage at these pins. In many applications, such as a DMM/DVM, the V_{IN} or V_{REF} input may have a high voltage source connected which is capable of supplying destructive currents into the MMC 130. To prevent such an occurence, a current limiting resistor should be placed in series with the apropriate input pin. The 1 mA maximum current rating should be observed. A 1M resistor in series with pin 17 of the MMC 130 would offer input protection up to a 1000V overvoltage.

4. **Lock-Up Protection.** The E204 JFET shown in the typical MMC 130 application of Figure 5 eliminates a power-on lock-up mode. This condition manifests itself by a constant 007 output. If the J-FET is not udes, it may be necessary to recycle the power supplies to attain normal operation. The use of the E204 J-FET reduces the maximum allowable negative supply voltage, V_2 to -5.5 V.

5. **TTL Compatibility.** While both the Digit Strobe (D_1, D_2, D_3) and Data Bit (B_0, B_1, B_2, B_3) outputs are capable of driving 1 TTL load, the maximum internal clock stability, and thus A/D stability, is attained when the bit outputs sink less than 400 µA. Therefore, CMOS or lowpower Schottky TTL decoders are preferred. Standard TTL loads will not contribute to A/D instability when an external oscillator is used.

6. **Range Signal Decoding Autoranging.** The ranging signals (overrange and underrange) are time multiplexed on the SIGN/OR output. De multiplexing consists of logically ANDING this output with either the D_1 or D_2 Digit Strobe output (see Figure 4). Thus:

$D_1 \cdot$ SIGN/UR/OR =
= Uderrange Pulse (active high) when count 80
$D_2 \cdot$ SIGN/UR/OR =
= Overrange Pulse (active high) when count 999

If either an underrange or overrange condition exists, the appropriate pulse will occure once each sampling interval during the zeroing time. This single pulse can be used directly to step on Autoranging circuit into the next range.

7. **Ratio operation.** The high impedance reference buffer amplifier and input buffer amplifier make the MMC 130 very useful in ratio measurements. The ratio error curve shown in the Typical Characteristics section illustrates the A/D transfer function.

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \; \frac{R_1}{R_2} \; 4096$$

Assuming the ideal design values for R_1 and R_2 (10 K and 20.48 K) the A/D transfer equation is:

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \times 2000$$

Actual R_1 and R_2 matching tolerance can deviate by 3%.

8. **Inter-Digit Blanking.**

a. The interdigit blanking period allows the MMC 130 to interface With gas discharge displays when oscillator frequencies of 16 kHz or less are used.

b. Since the BCD data for each digit appears before and does not change until after the digit strobe (except when new data is loaded), interface problems such as latching of improper codes are minimized.

c. The net digit duty cycle is reduced to 25% by the inter-digit blanking period. Average LED currents must be calculated with this consideration.

d. Since the total inter-digit blanking time is equal to a digit ON time, it may be used as a fourth digit strobe for special applications.

9. **High Temperature Operation of the MMC 130**

a. Device protection.

The MMC 130 does have the parasitic SCR structures common to all junction isolated CMOS devices. However, the MMC 130 includes special protection circuits at both inputs and outputs to minimize the possibility of turning on one of these SCR devices which could lead to excessive power supply drain current and possible device destruction. This possibility, while remote at normal ambient temperatures, in enhanced by operation above 85°C. A 100 resistor in series with the V_I Input of the MMC 130 will prevent such an occurence at high temperatures while allowing for normal A/D action.

b. C_{INT}, C_{AZ} Selection

High temperature operation makes special demands on capacitor values and types. Polycarbonate capacitors are required for C_{INT} and C_{AZ} due to leakage limitations. Although the value of C_{INT} is chosen as in paragraph 1, C_{AZ} must be 10 times the value of C_{INT}. This fixes the AZ system damping factor at 0.6 (see AZ equations) and maintains the maximum value of C_{AZ} consistent with proper AZ loop settling.

c. Leakage Protection Pin Guarding

Proper high temperature performance requires that all high impedance inputs (V_{IN}, V_{REF}, AZ) be guarded to minimize pin-to pin leakage. Good guarding requires a 2 sides glass-epoxy P.C. board with all guard traces and rings driven from low impedance sources. These sources should have a potential close to that of the guarded pin.

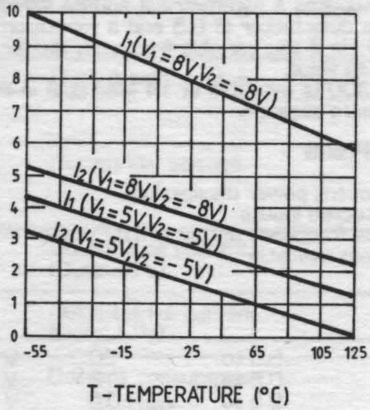
MMC 130 AZ EQUATIONS

$$\omega_n = \sqrt{\frac{1.25 \times 10^{-9}}{C_{INT}C_{AZ}}}$$

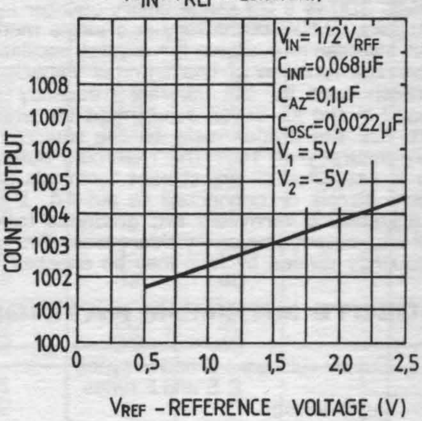
$$\xi = \sqrt{\frac{1}{32}\left(1 + \frac{C_{INT}}{C_{AZ}} + \frac{C_{AZ}}{C_{INT}}\right)}$$

TYPICAL CHARACTERISTICS

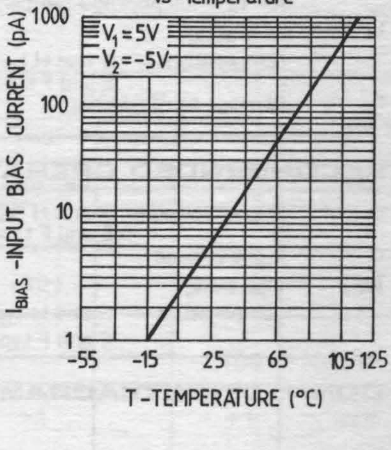
Supply Currents
vs Temperature



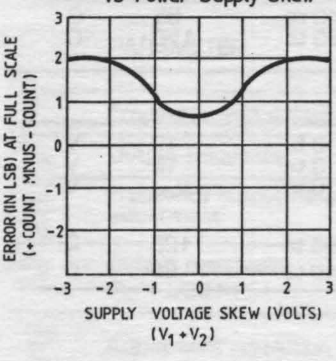
Ratio Operation
(V_{IN}/V_{REF} = Constant)



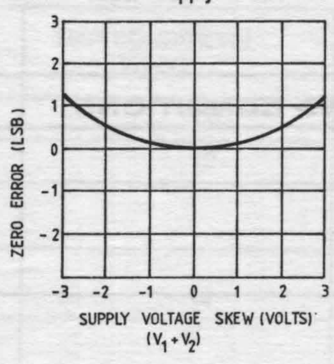
Input Bias Current
vs Temperature



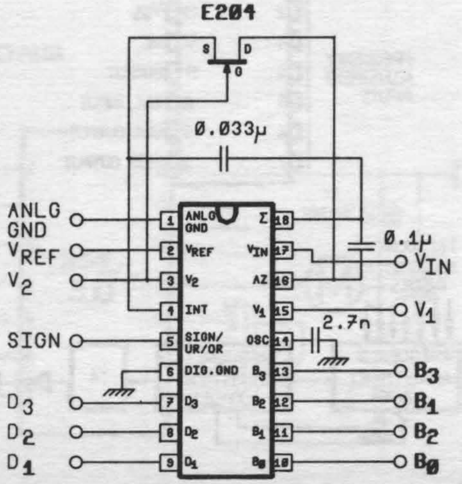
Rollover Error
vs Power Supply Skew



Zero Error vs
Power Supply Skew



APPLICATION



STEP-BY-STEP MOTOR DRIVE CLOCK CIRCUIT

GENERAL DESCRIPTION

The MMC 300 is a 23 stage binary counter in standard Al-gate CMOS technology in a single monolithic chip. An inverter is available for crystal oscillator application. The function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC. Seven adjustment terminals are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The maximum output frequency is set when all adjustment terminals are either open- circuit or connected to pin 14.. If one or more adjustment terminals are grounded (taken to pin 13) the output frequency decreases. The oscillator frequency divided by four may be checked at the test output (pin 8). With an oscillator frequency of 4.194812 MHz the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 0.5 Hz if the variable frequency divider is set to its medium value.

The MMC 300 is available in 14 lead dual in-line and ceramic plastic package.

FEATURES

- Low quiescent power dissipation
- Fully protected inputs
- Adjustable frequency divider in 127 steps
- Test output available

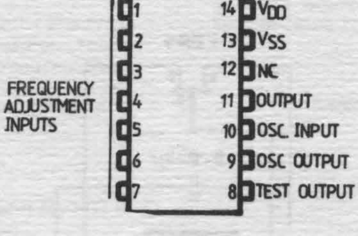
ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

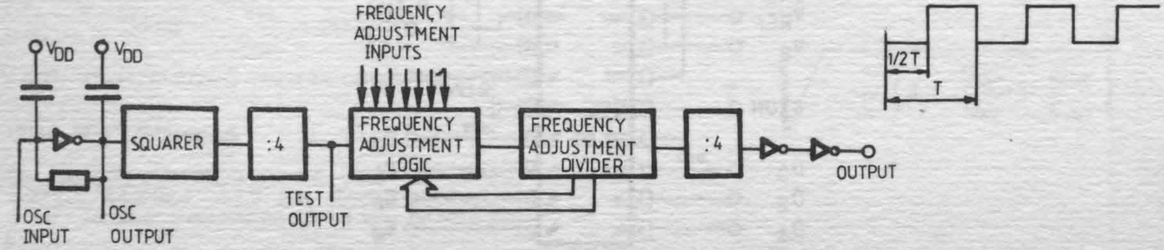
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	VALUES 25° C min.	typ.	max.	UNITS
V_{OH}	Output high voltage	$I_{OH} = 0$	6 9 12	5.99 8.99 11.99	6 9 12		V V V
V_{OL}	Output low voltage	$I_{OL} = 0$	6 9 12		0 0 0	0.01 0.01 0.01	V V V
I_{DN}	Output sink current (Output P_{in})	2 2	6 12	20 33	25 40		mA mA
I_{DP}	Output drive current (Output P_{in})	4 10	6 12	20 33	25 40		mA mA
I_{ON}	Current consumption		6 12		3 3		mA mA

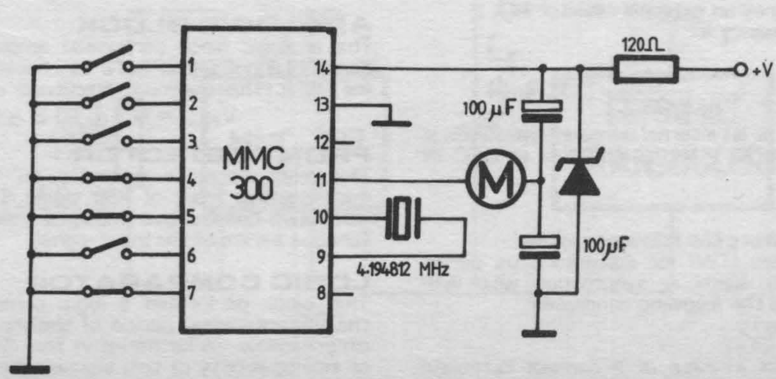
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°$ C, quartz frequency = 4, 194 812 MHz)

	PARAMETER	TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNITS
f_T	Frequency test output	12	1.048,693		1,048,713	Hz
f_{o}✲	Output frequency	12		0.5		Hz
$\frac{\Delta f}{f_O}$	Frequency output range adjustment		−121		+121	ppm
R_O	Output resistance (R_L = 300 K)	12			100	ohm
$\frac{df_O}{f_O}$	Adjustment resolution		−1		+1	ppm

✲ At the center position of the variable divider.

TYPICAL APPLICATIONS



KEY CALLER SYSTEM

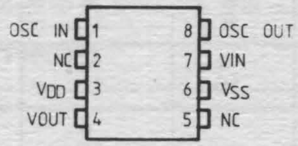
GENERAL DESCRIPTION

The MMC 333 is a low voltage, metal gate CMOS integrated circuit that implemented a KEY CALLER system. A KEY CALLER system detect aleatory signals with relative constancy of frequency and signalize that detection. Achievement of acoustic-to-electric and electric-to-acoustic conversions requires a single ceramic transducer. The device operates from a single 1.5V to 5V supply and is designated to minimize external components. The MMC 333 is available in 8 lead dual-in-line pakage.

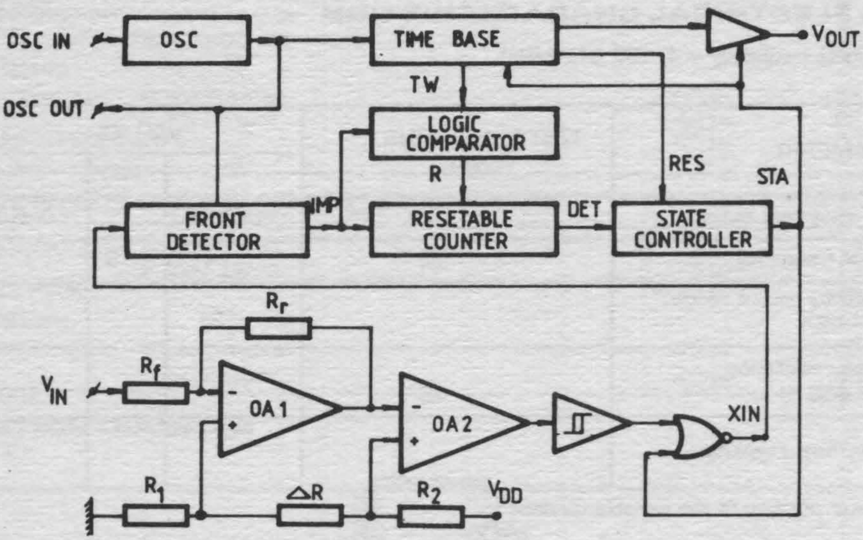
FEATURES

- Low voltage CMOS technology
- Low power consumtion
- On-chip oscillator
- A single input/output ceramic transducer

CONNECTION DIAGRAM



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Oscilator (OSC IN - OSC OUT)

The oscillator requires an external resistor R().
The oscillation frequency is:

$$f_0 = \frac{1}{2.2R_0C_0}\ ;\ T_0 = \frac{1}{f_0}\ ;$$

where C^0 = 50 pF is an internal achieved capacitor. It is posible to attach an external oscillator at OSC IN or OSC OUT.

TIME BASE

The time base generate the following signals:

- the time windows (TW) for instantaneous period measurement. This signal is syncronous with IMP signal and satisfyed the following conditions:
  - $TW_L = 8 \ast T_0$
  - $TW_H < 4 \ast T_0$
- the output signal in case of a correct detection performed.
- tte reset signal (RES) to return at reception state; this signal determinate the emision time to $T_E = 2^{15} \ast T_0$.

ANALOGIC BLOCK

The analogic block performed amplification and limitation of input signal (VIN) to convert it in digital signal (XIN). The minimum amplitude of input signal is:

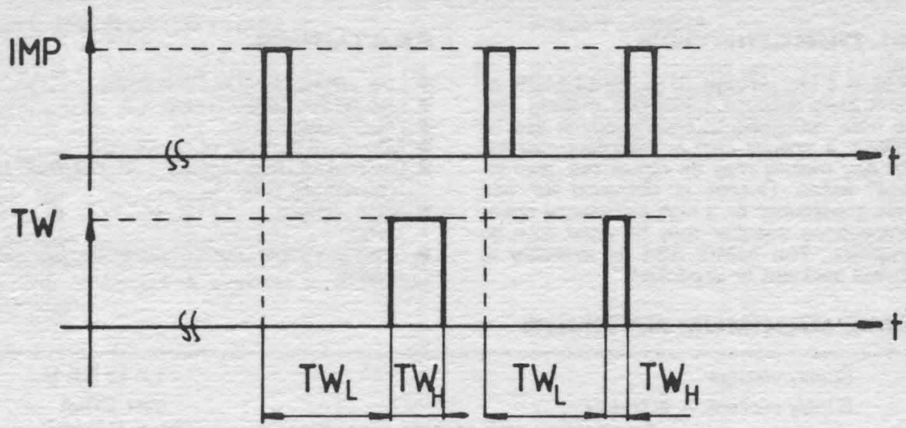
$$V_{IN_{min}} = 0.3 \ast 10\text{-}3 \ast V_{DD}$$

FRONT DETECTOR

The front detector generate an impuls (IMP) for each positive front of XIN signal. The distance between two consecutive impulses measure the instantaneous period of the input signal.

LOGIC COMPARATOR

This block performed a logic comparation between the instantaneous period of the input signal and the time window performated in the time base. In case of incompatibility of this signals, the counter is initialized.



RESETABLE COUNTER

This block counts the consecutive goods instantaneous period of the input signal. If the number of this periods is largest to N_{min} and smaller to N_{max}, then the system detected a correct input signal. This number (N_{min}, N_{max}) determinate the quality of detection, estimated with the ratio of the probability of signaL detection to the probability of noise detection:

$$S = 20 * \lg \frac{P_{signal}(N)}{P_{noise}(N)} = S(N)$$

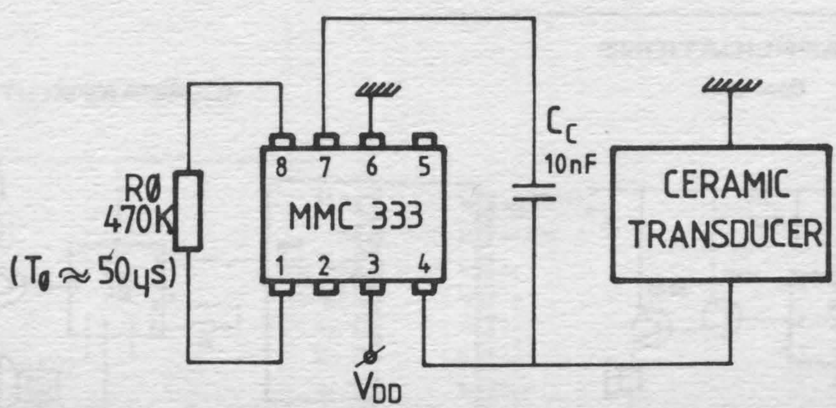
For this implementation Nmin = 128, N_{max} = 256 and optimized the quality factor (S = + 30dB) in following input conditions:

- the bandwing of the noise:
  400Hz — 3400Hz
- the bandwidth of the input stimulus:
  1750Hz — 2250Hz
- the minimum signal/noise ratio at system input
  — 17 dB

STATE CONTROLLER

The state controller allow the function of the system with a single input/output traductor.

TYPICAL APLICATION



MELODY GENERATOR

GENERAL DESCRIPTION

The MMC 334 is a low voltage, Al — gate CMOS integrated circuit that outputs a 64-note melody. Because all the data refferring to the melody is stored in on-chip ROMs, a special chip is manufactured for every melody. Any melody may be requested, also including „pause" notes. Output is designed for use with a ceramic transducer or a high impedance speaker. A low impedance speaker may be used with an additional amplifier. The MMC 334 is available in 8 lead dual-in-line package, or unpacked.

FEATURES

- Low voltage CMOS technology
- Low power consumption
- On-chip oscillator
- Maximum number of notes : 64
- Generated frequencies : 2 octaves (16 distinct frequencies only)
- Note length : 1/16 to 1/1 at programmable tempo
- Programmable note's envelope (32 steps & 16 levels)

ABSOLUTE MAXIMUM RATINGS

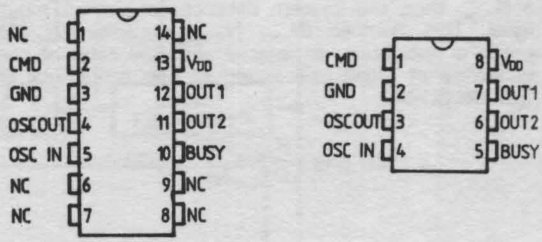
V_{DD}	Supply voltage	1.5 to 5.5 V
I_{DD}	Supply current — stand-by	max. 20μA
	— functionning with ceramic transducer	typ. 0.8mA✻
R	External resistor	30 to 500 kΩ✻

✻ Depending on the programmed melody

PIN DESIGNATION

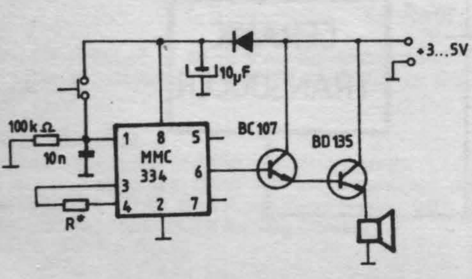
NAME	NUMBER	DESCRIPTION
CMD	1	Input command pin active high. A pulse on this pin starts the melody. It is internally pulled-up resulting in continous playing.
GND	2	Ground
OSCOUT	3	Output pin for internal oscilator use. Connecting a resistor between OSCOUT and OSCIN pins activates the on-chip oscillator.
OSCIN	4	Input pin for internal oscillator use. It may be driven by an external clock generator.
BUSY	5	Output pin, active low, indicating that the melody is in progress.
OUT1, OUT2	6,7	Opposite analog outputs
V_{DD}	8	Supply voltage

CONNECTION DIAGRAM

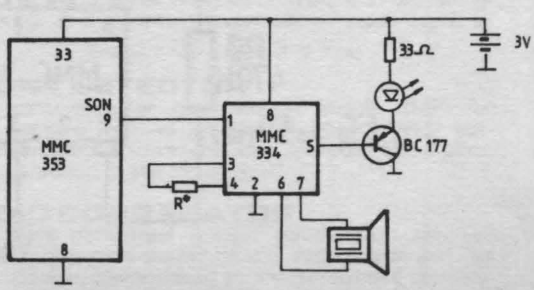


TYPICAL APPLICATIONS

Door bell



Clock alarm



AUTO CLOCK

GENERAL DESCRIPTION

The MMC 351 is a metal gate CMOS integrated circuit that provides or controls all signals needed for a $3^1/_2$-digit LED watch. The display format is 12 hours, with an AM/PM indicator. The circuit time base is a 32768 Hz crystal controlled oscillator. The time base frequency is successively divided to provide drive signals for a multiplexed 7-segment display. In order to drive the display, the watch requires a BCD-to-7 segment decoder (the MMC4511, for example). The device operates from a single 3V to 18V supply. The MMC351 is available in a 16-lead dual-in-line package.

FEATURES

- 32768 Hz crystal controlled oscillator
- wide supply voltage range: 3 to 18V
- low current consumption (3mA)
- 12 hours display format
- on-chip oscillator

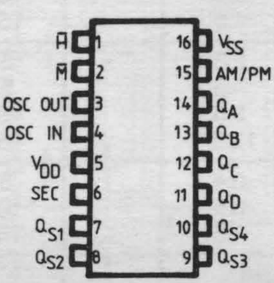
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	–0.5	...	18	V
V_I	Input voltage	–0.5	...	V_{DD} + 0.5	V
P_D	Total power dissipation	200 mW			
T_A	Operating temperature	–40	...	+ 85	°C
T_S	Storage temperature range	–65	...	+ 155	°C

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3	...	15	V
V_I	Input voltage	0	...	V_{DD}	
T_A	Operating temperature	–40	...	+ 85	°C

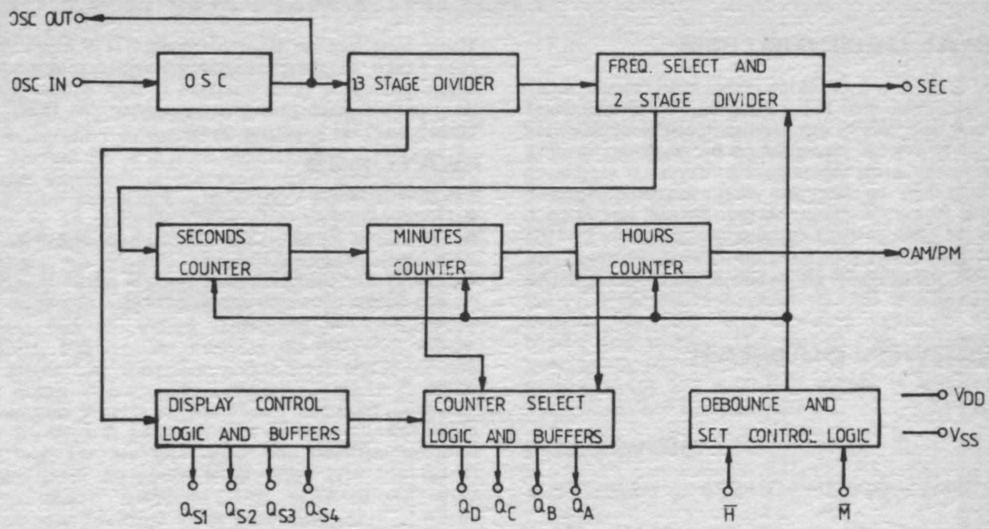
CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C, fosc = 32 768 Hz)

PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES 25°C min.	max.	UNIT
I_L	Quiescent current	0/ 5 0/10 0/15			5 10 15		1400 1600 1800	μA
V_{OH}	Output low voltage	0/ 5 0/10 0/15		< 1 < 1 < 1	5 10 15	4.95 9.95 14.95		V
V_{OL}	Output low voltage	5 /0 10/0 15/0		< 1 < 1 < 1	5 10 15		0.05 0.05 0.05	V
V_{IH}	Input high voltage		0.5/4.5 1/9 1.5/13.5	< 1 < 1 < 1	5 10 15	3.5 7 11		V
V_{IL}	Input low voltage		4.5/0.5 9/1 13.5/1.5	< 1 < 1 < 1	5 10 15		1.5 3.0 4.0	V
I_{IH}, I_{IL}	Input leakage current	0/15			15		±0.3	μA
I_{OH}	Drive current on BCD outputs	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15		0.5 0.5 1.5 3.0	mA
I_{OL}	Sink current on BCD outputs	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15		0.5 1.5 3.0	mA
I_{OH}	Drive current on digit outputs	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15		0.5 0.5 1.5 3.0	mA
I_{OL}	Sink current on digit outputs	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15		0.14 0.5 0.9	mA
I_{OH}	Drive current on AM/PM, SEC outputs	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15		0.1 0.1 0.2 0.4	mA
I_{OL}	Sink current on AM/PM, SEC outputs	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15		0.1 0.2 0.4	mA
I_{OH}	Drive current on OSC OUT outputs	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15		0.5 0.5 1.5 3.0	mA
I_{OL}	Sink current on OSC OUT outputs	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15		0.5 1.5 3.0	mA
C_I	Input capacitance	Any input					7.5	pF

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

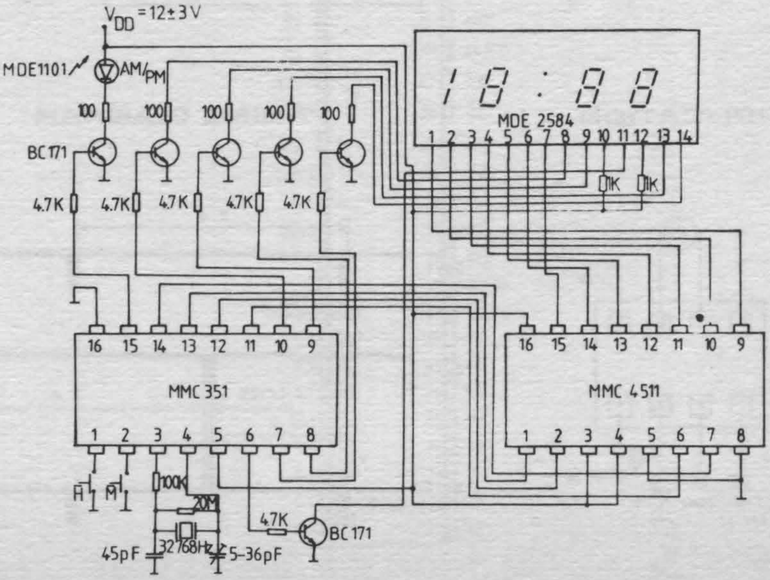
Time base:
The time base of the watch is provided by connecting a crystal controlled RC network to the on-chip CMOS inverter/amplifier.

Display multiplexing:
Outputs from each counter are time-division multiplexed to provide digit-sequential acces to the time data. The $3^1/_2$ digits of the display are multiplexed with a 22% duty cycle, 1024 Hz signal.

Time display:
The hour information is displayed in digit positions 1 and 2, while minute information in digit positions 3 and 4. There are an AM/PM indicator and a seconds serially output.

Time setting:
Closure of the 'M' switch will advance minutes at a 2 Hz rate, with no advance of the hours counter and with seconds counter in 00. Closure of the 'H' switch will advance hours counter at a 1 Hz rate. When POWER ON, minutes counter must be set first.

TYPICAL APPLICATIONS



WRIST WATCH STEP MOTOR DRIVER

GENERAL DESCRIPTION

The MMC 352 is a monolithic integrated circuit, available as unpacked die. The circuit is manufacturated in a low voltage CMOS technology (typical supply voltage 1.5V) and it is intended to be used for driving step motors for wrist watches.

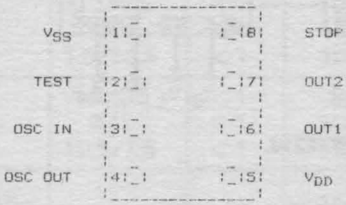
It contains an oscillator with external quartz (f_o=32768 Hz), 16 stage binary divider, an output stage which delivers two oposite signals with 1/128 ratio and two output buffers for motor driving. The oscillator requires only an external trimmer and the quartz cristall.

The circuit has an asynchronous STOP input which, in high state, stops the oscillator, resets the binary divider and turns both outputs in high state. This input has an internal pull-down resistor. A TEST output with f_o=16 Hz is also provided.

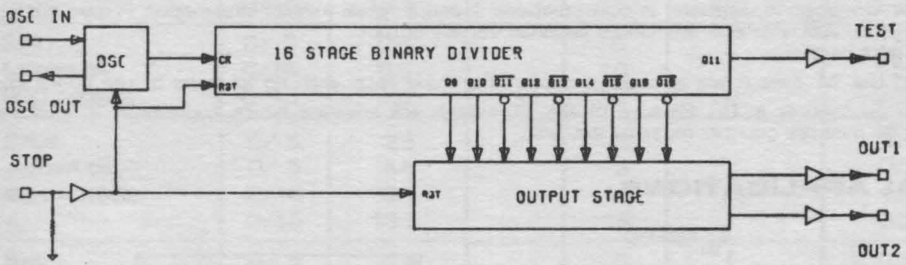
FEATURES

- Supply Voltage V_{DD} = 1.2 ... 1.7 V
- Quartz Frequency f_o = 32768 Hz
- Very Low Power Consumption in Stand-by (STOP in High State) $I_{DD} < 1\ \mu A$
- Low Power Consumption $I_{DD} < 3\ \mu A$ at V_{DD} = 1.5 V and Motor Resistance of 3.5 kΩ.

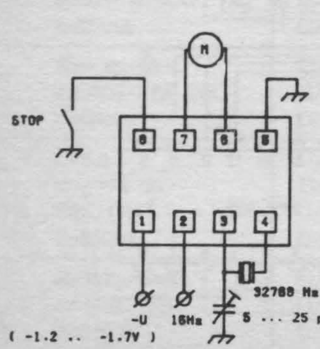
CONNECTION DIAGRAM



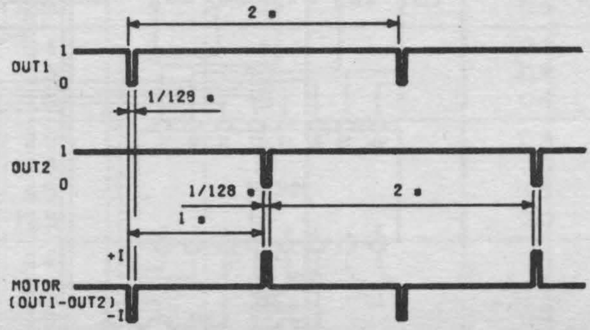
FUNCTIONAL DIAGRAM



TYPICAL APPLICATION



TIMING DIAGRAM



LCD/LED WATCH CIRCUIT

GENERAL DESCRIPTION

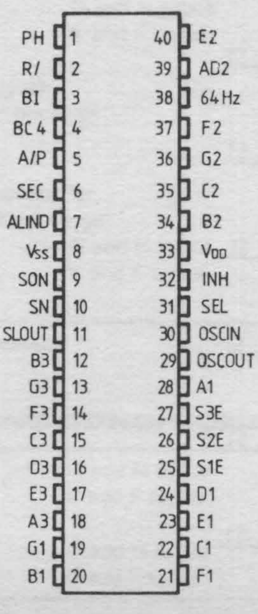
The MMC353 is a low threshold voltage metal gate CMOS integrated circuit that provides or controls all signals needed for a 3 1/2 digit LCD or LED watch. The circuit timebase is a crystal controlled oscillator. The selection input SEL is set to 1 for a 32768 Hz oscillator or to 0 for a 4194304 Hz oscillator. This time base frequency is counted down to provide proper signals to display Hours-Minutes information continuously, with Seconds and Month-Date information available upon demand. Time is displayed in 12 hours format. When displaying Hours-Minutes information, the circuit provides an AM/PM indicator, an alarm "on" indicator and a 1 Hz signal for the blinking colon. The circuit contains an alarm counter that provides Alarm Hours-Alarm Minutes information on demand. A serial output of this counter SON is kept high for an hour after the coincidence between the time counters (real time) and the alarm counters (alarm settings). The SON output may be temporarly inhibited for a time interval of 7 minutes using the snooze input SN or cancelled using the programming buttons S2E, S3E. In order to turn off a radio after a desired time interval of up to 59 minutes, the circuit contains a sleep downcounter with the serial output SLOUT. The reset input R/ allows resetting all the counters. The Seconds, Minutes and Alarm Minutes counters are reset to 00, the Hours, Alarm Hours, Month and Date counters are reset to 01 and the Sleep counter is reset to 59. The programming inputs S1E...S3E allow the watch to change displaying information (Hours-Minutes) and to set counters (Hours, Minutes, Seconds, Month, Date, Alarm Hours, Alarm Minutes, Sleep Minutes).

The programming inputs S1E...S3E, the snooze input SN and the reset input R/ are internally connected to 1; for making them active push butons are used that establish a temporarly connection to 0. 24 phase-controlled outputs are available for direct drive of a 3 1/2 digit liquid crystal output display. A 64 Hz output serves as the backplane drive for the LCD and as phase input PH for the circuit when used with LCD display. When used with LED display, the PH input is set to 1 for common cathode LED and to 0 for common anode LED. The blanking input BI set to 1 blanks the display. The watch may be inhibeted by connecting the INH input to 0. The circuit operatês from a single 2.5 V to 5 V supply. It is available in a 40-lead dual-in-line package.

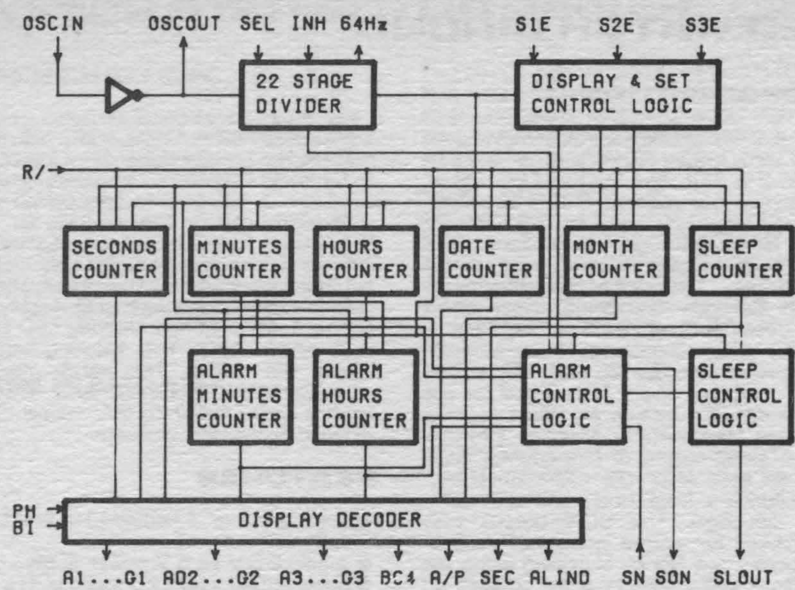
FEATURES

- 32768 Hz or 4194304 Hz crystal controlled operation
- single 2.5 V to 5 V power suplly
- drive outputs for LED's and LCD's
- 12 hours display
- AM/PM output
- alarm "on" indicator
- colon display
- 24 hours alarm setting
- 7 minutes snooze alarm
- presettable 59 minutes sleep downcounter
- all counters resettable
- 3 butons sequential setting

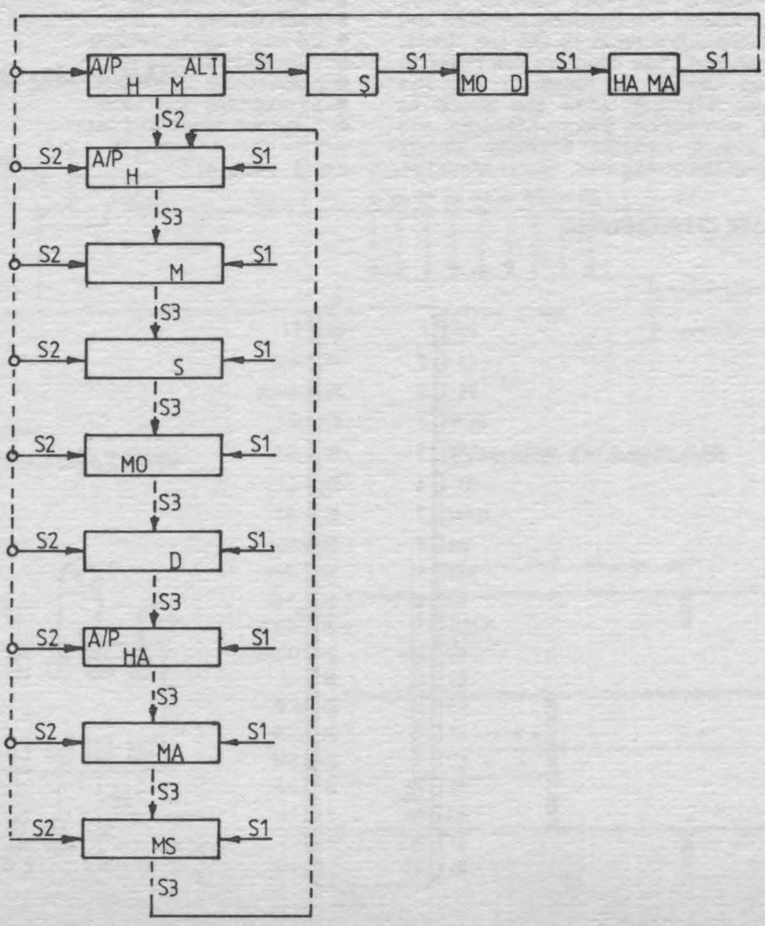
CONNECTION DIAGRAM



BLOCK DIAGRAM



WATCH PROGRAMMING DIAGRAM



CMOS CROSSPOINT SWITCH WITH CONTROL MEMORY
MMC 355 — SERIAL SWITCH ADDRESSING
MMC 356 — PARALLEL SWITCH ADDRESSING

GENERAL DESCRIPTION

The MMC 355 and MMC 356 are CMOS integrated circuits containing a 8x8 array of digitally controlled analog switches together with control memory, address decoders and level translators. The array is organized as 8 multiplexers with common inputs. The multiplexers can be individually inhibited. Any of the 8 multiplexers can be addressed by selecting the appropriate 7 bits (address and inhibit) of the programming word.
For the MMC 355 the address and inhibit bits are loaded serially into an internal shift register on the leading edge of clock signal. For the MMC 356 the programming word is loaded parallely. This operation is performed when the select inputs ($\overline{S}_1$, $\overline{S}_2$, S_3 for the MMC 355; S_1, S_2 for the MMC 356) are properly set.
The presence of multiple select inputs facilitates the array connection of such circuits. When the required operating power is applied, the states of the 64 switches must be turned off by inhibiting all the multiplexers in succession.
The MMC 355 and MMC 356 are housed in a 24-pin and a 28-pin dual-in-line package, respectively.

FEATURES

- Low "on" resistance: 125 Ω (typ.) over 15 Vp.p. signal-input range for $V_{DD}—V_{EE}$=15V
- High "off" resistance: channel leakage: ±500 p. nA (max) for $V_{DD}—V_{EE}$=15V
- Internal memory
- Large analog signal capability
- High cross-talk off-state insolation
- Pull-up or pull-down resistors on all digital inputs
- Low power, high noise immunity CMOS technology
- Serial switch addressing, 3 select inputs (MMC 355)
- Parallel switch addressing, 2 select inputs (MMC 356)

TYPICAL APPLICATIONS

- Telephone switching systems
- Analog or digital multiplexers
- Data acquisition systems
- Test equipments

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	−0.5	to	20	V
		E and F types	−0.5	to	18	V
V_I	Input voltage		−0.5	to	V_{DD}+0.5	V
I_I	DC input current (anyone input)				±10	mA
Ptot	Total power dissipation (per package)					
	MMC 355				400	mW
	MMC 356				400	
	Dissipation per output transistor for					
	T_{op} = full package-temperature range				100	mW
T_A	Operating temperature:	G and H types	−55	to	125	°C
		E and F types	−40	to	85	°C
T_{stg}	Storage temperature		−65	to	150	°C

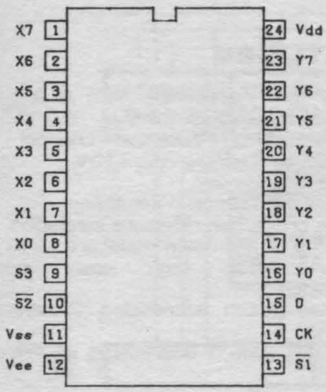
* All voltages are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

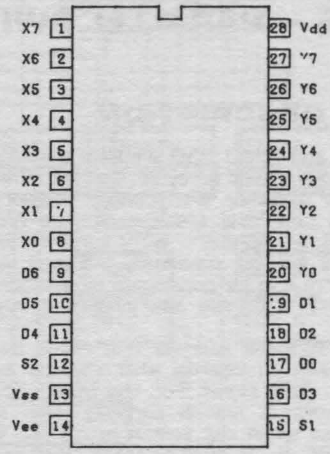
V_{DD}*	Supply voltage:	G and H types	3	to	18	V
		E and F types	3	to	15	V
V_I	Input voltage		0	to	V_{DD}	V
T_A	Operating temperature:	G and H types	−55	to	125	°C
		E and F types	−40	to	85	°C

CONNECTION DIAGRAMS

MMC 355

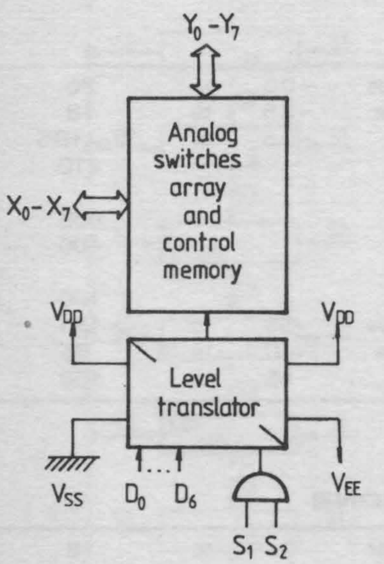


MMC 356

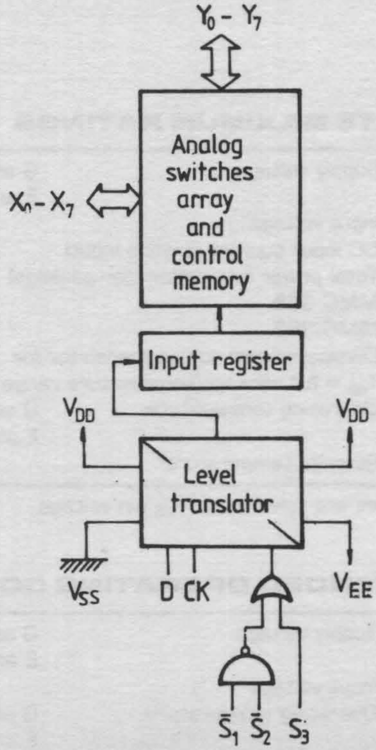


BLOCK DIAGRAMS

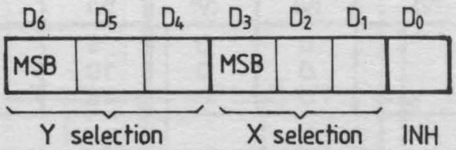
MMC 355



MMC 356



PROGRAMMING WORD



TRUTH TABLE

ADDRESS							CONNECTION
DY_2	DY_1	DY_0	DX_2	DX_1	DX_0	INH	
0	0	0	X	X	X	0	MUX 0 inhibited
0	0	1	X	X	X	0	MUX 1 inhibited
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	X	X	X	0	MUX 7 inhibited
0	0	0	0	0	0	1	X0—Y0
0	0	0	0	0	1	1	X1—Y0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
0	0	0	1	1	1	1	X7—Y0
0	0	1	0	0	0	1	X0—Y1
0	0	1	0	0	1	1	X1—Y1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
0	0	1	1	1	1	1	X7—Y1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	0	0	0	1	X0—Y7
1	1	1	0	0	1	1	X1—Y7
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	X7—Y7

X — Don't care

STATIC ELECTRICAL CHARACTERISTICS
(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES			UNIT
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	Min.	Typ.	Max.	
I_{DD}	Quiescent device current		0 0 0	0 0 0	5 10 15			60 150 2500	µA
SWITCH									
R_{ON}	ON resistance	$0 \leq V_I \leq V_{DD}$	0	0	5 10 15		470 180 125	1050 400 280	Ω
ΔR_{ON}	(between any 2 channels)		0	0	5 10 15		15 15 10		Ω
OFF channel leakage current(●)	All switch OFF		0	0	15			500	nA
C capacitance	Input output feedthrough		−5	−5	5		35		pF
CONTROL									
V_{IL}	Input low voltage	$=V_{DD}$ through 1 kΩ	$V_{EE}=V_{SS}$ $R_L=1$ kΩ to V_{SS}		5 10 15			1,5 3 4	V
V_{IH}	Input high voltage		$I_{IS} < 2$ µA on all OFF channels		5 10 15	3,5 7 11			V
I_I(●●)	Input current (Any control input)		$V_I=0/15$ V		15			60	µA
C_I	Input capacitance (Any data or select input)						5	7,5	pF

(●) Determined by minimum feasible leakage measurement for automatic testing

(●●)

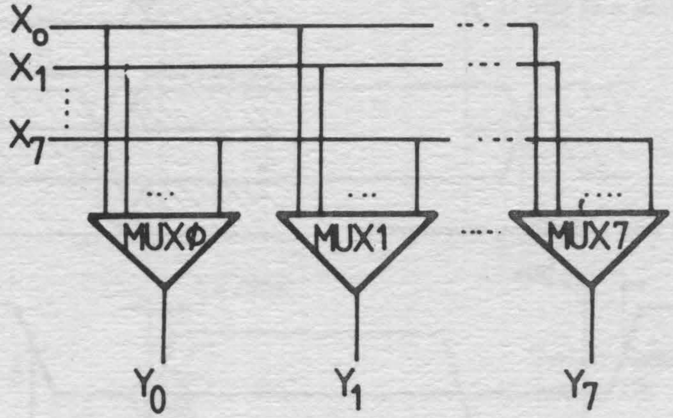
MMC 355: The D, $\overline{S}_1$, $\overline{S}_2$ inputs are tied to V_{DD} through a pull-up resistor.
The CK and S_3 inputs are tied to V_{SS} through a pull-down resistor.

MMC 356: The D_0—D_6, S_1, S_2 inputs are tied to V_{DD} through a pull-up resistors.

CIRCUITS DESCRIPTION

The MMC 355 and MMC 356 are CMOS integrated circuits containing 64 digitally controlled analog switches, control memory, decoders, level translators and addressing logic.

The switches array and the input logic are powered between V_{DD} and V_{EE}, and between V_{DD} and V_{SS}, respectively.
The analog switches array is organized as eight 8:1 common inputs (X_0, X_1,...,X_7) multiplexers, the outputs being Y_0, Y_1,...,Y_7.



Crospoint array

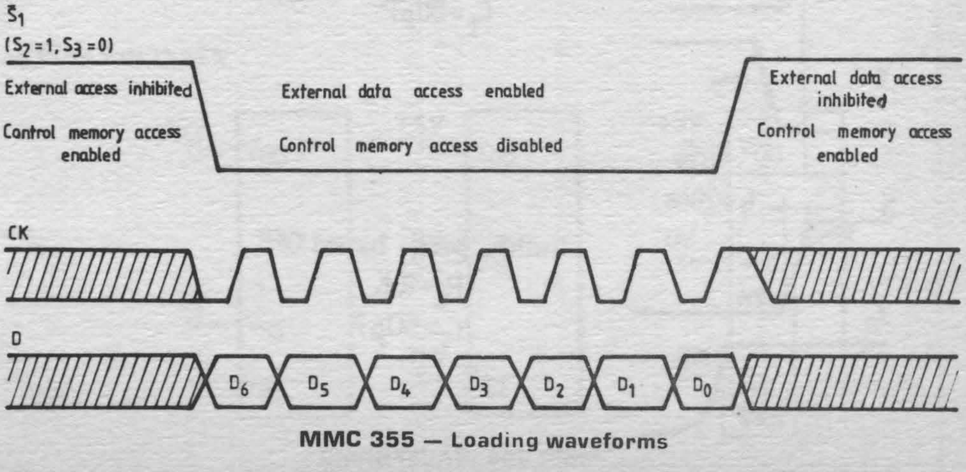
Each multiplexer can be inhibited (all its switches are off).
Each multiplexer must be separately programmed.
The programming word is 7 bits long (D_6, D_5,...,D_0).
The bit allocation follows:

D_6	D_5	D_4	D_3	D_2	D_1	D_0
DY2	DY1	DY0	DX2	DX1	DX0	INH

$Y_{selection}$ (MUX selection) $X_{selection}$ (Switch selection) Inhibit

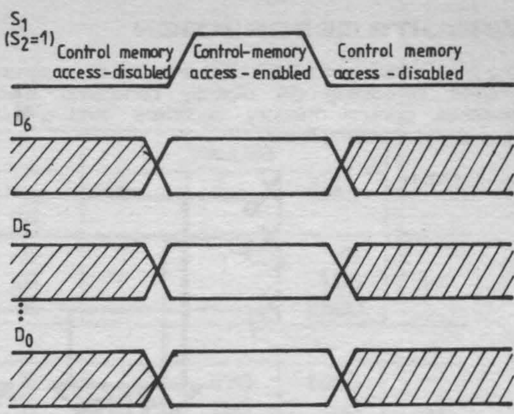
At a time, no more than one channel can be ON in every multiplexer. Thus, in the whole array, a maximum of 8 switches are ON simultaneously.

The D_6, D_5, D_4 bits select the multiplexer, the D_3, D_2, D_1 bits select the channel. If $D_0 = 0$, the multiplexer is inhibited (all channels OFF).
If $D_0 = 1$, the channel selected by the D_3, D_2, D_1 will be ON.
The control memory retains the state of every switch.
When the operating power supply is applied, the states of the analog switches are indeterminate. Therefore, all the multiplexer must be turned off, or properly programmed (8 steps).
The programming word can be serially (MMC 355) or parallely (MMC 356) loaded.
The MMC 355 contains a serial input (D) shift register. The loading is performed on the leading edge of the CK signal, and begins with the D_6 bit.
The operation is accomplished only if the select inputs combination ($\overline{S}_1 \cdot \overline{S}_2 + S_3$) is at logic 1. (See fig. below).

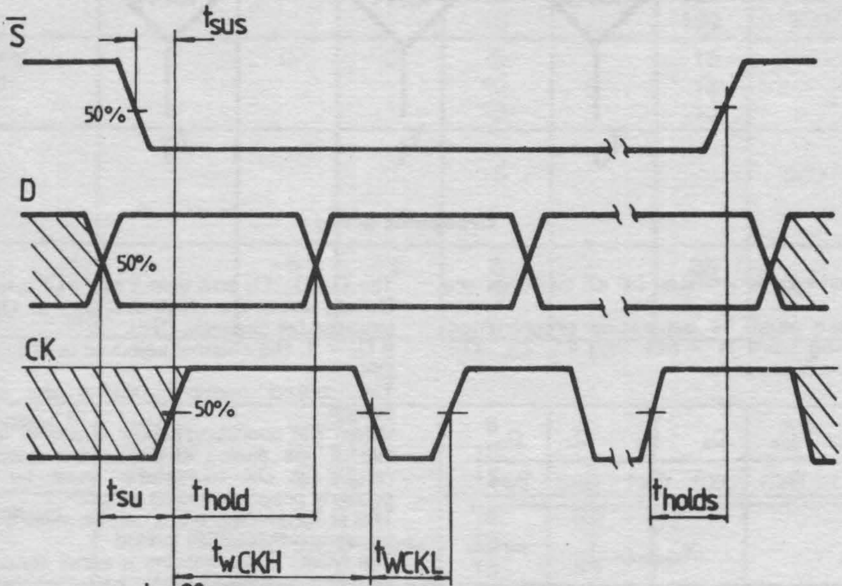


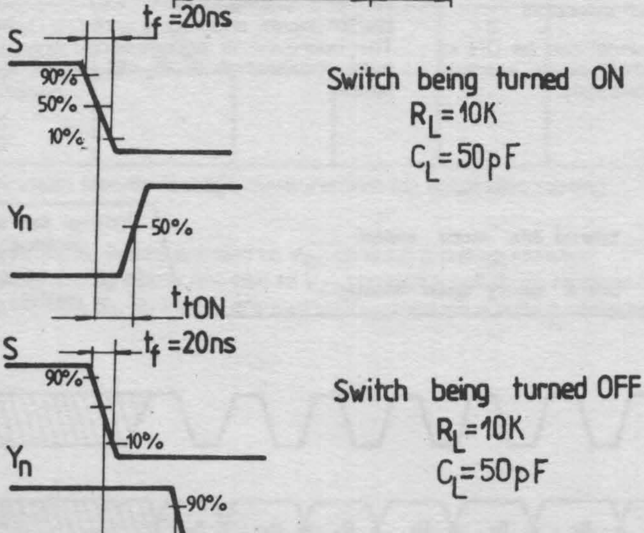
MMC 355 — Loading waveforms

As long as the selection signals are active, the data are shifted through the register without affecting the memory status. When the selection signals are disabled, the information passes from the shift register into the control memory.
For the MMC 356 version, the programming word is loaded directly in the control memory, as long as the select signal is active ($S_1 \cdot S_2$ is at logic 1).



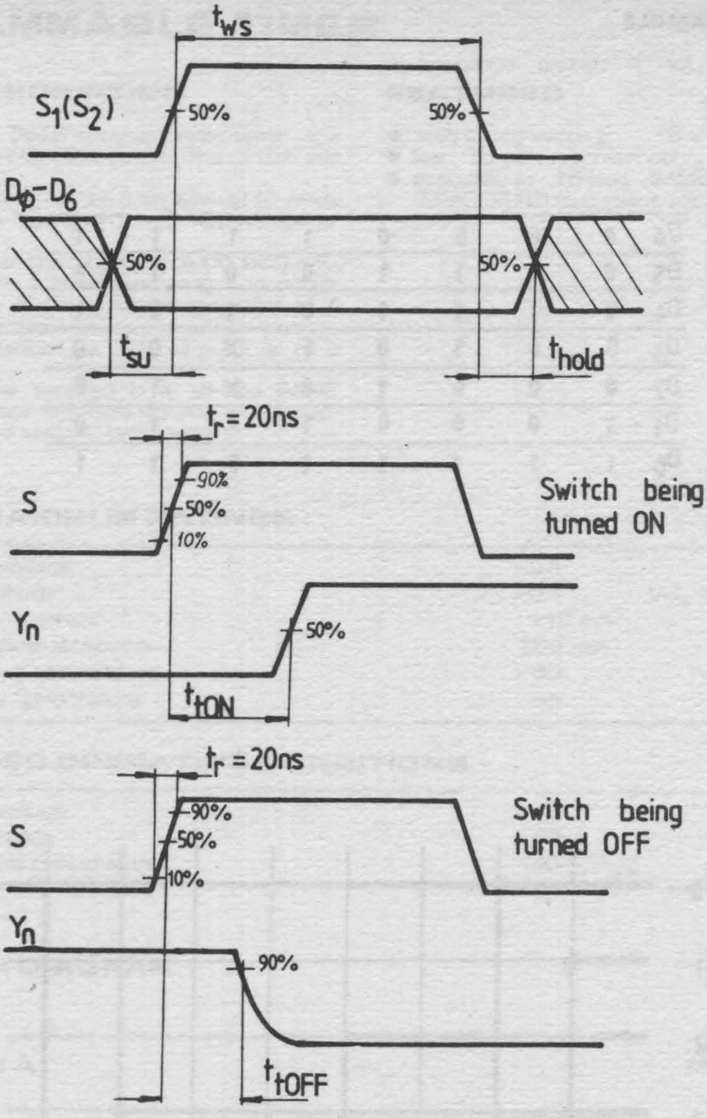
MMC 356 — Loading waveforms



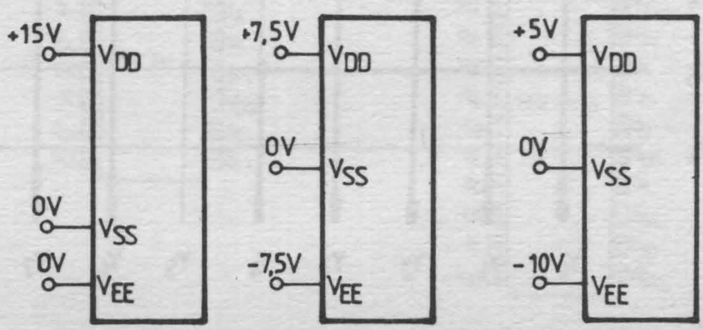


MMC 355 WAVEFORMS

MMC 356 WAVEFORMS



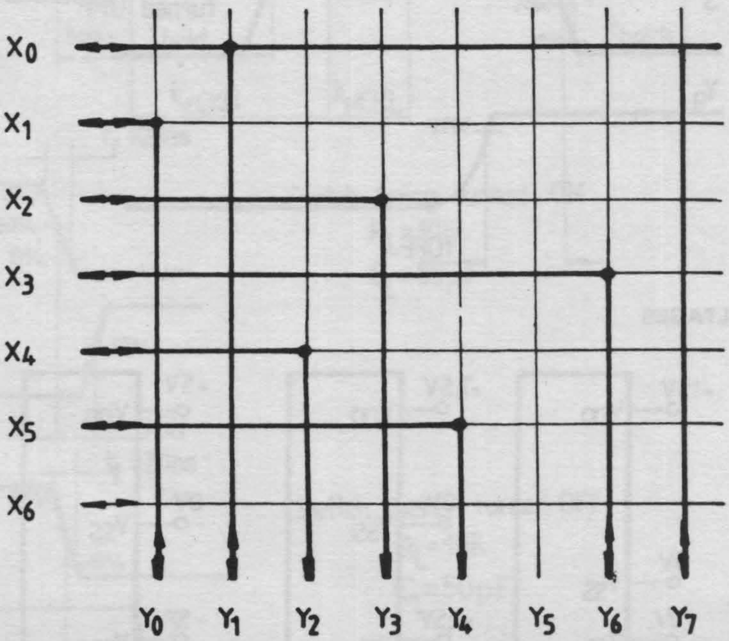
TYPICAL BIAS VOLTAGES



PROGRAMMING EXAMPLE

Programming words for a certain configuration
(MUX5 inhibited!)

D_6	0	0	0	0	1	1	1	1
D_5	0	0	1	1	0	0	1	1
D_4	0	1	0	1	0	1	0	1
D_3	0	0	1	0	1	X	0	0
D_2	0	0	0	1	0	X	1	0
D_1	1	0	0	0	1	X	1	0
D_0	1	1	1	1	1	0	1	1



PROGRAMMABLE TIMER

GENERAL DESCRIPTION

MMC 361A, MMC 361B programmable timer is a metal gate CMOS integrated circuit. The circuit can drive a 4-digit display.
The 4 internal counters can be programmed to divide by: 10✻10✻10✻10, 10✻6✻10✻10, 10✻10✻24 or 10✻6✻24.
The counters transfer their content to the BCD outputs of the circuit in a multiplexed way. The circuit compares the state of the counters with that of 4 external „tumble-switches".
The coincidence is sensed as a 0-1-0 pulse or as a 0-1 step.
The circuit can be supplied in a 16-lead (MMC 361A) or in a 24-lead (MMC361B) dual-in-line package, according to the specific application.

FEATURES

- wide supply range 3 . . . 18 V
- low current consumption: less than 1 mA
- available in 16-lead (MMC 361A) or 24-lea (MMC 361B) dual-in-line package

ABSOLUTE MAXIMUM RATINGS

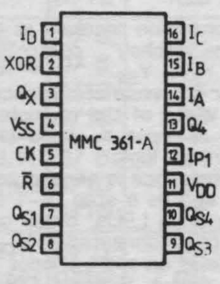
V_{DD}	Supply voltage	–0.5	...	18	V
V_I	Input voltage	–0.5	...	V_{DD} + 0.5	V
I_I	DC input current	+10 mA			
P_D	Total power dissipation	200 mW			
T_A	Operating temperature	–40	...	+ 85	°C
T_S	Storage temperature	–65	...	+150	°C

RECOMMENDED OPERATING CONDITIONS

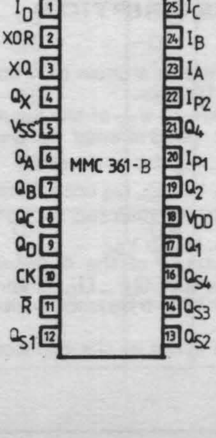
V_{DD}	Supply voltage	3	...	15	V
V_I	Input voltage	0	...	V_{DD}	
T_A	Operating temperature	–40	...	+85	°C

CONNECTION DIAGRAM

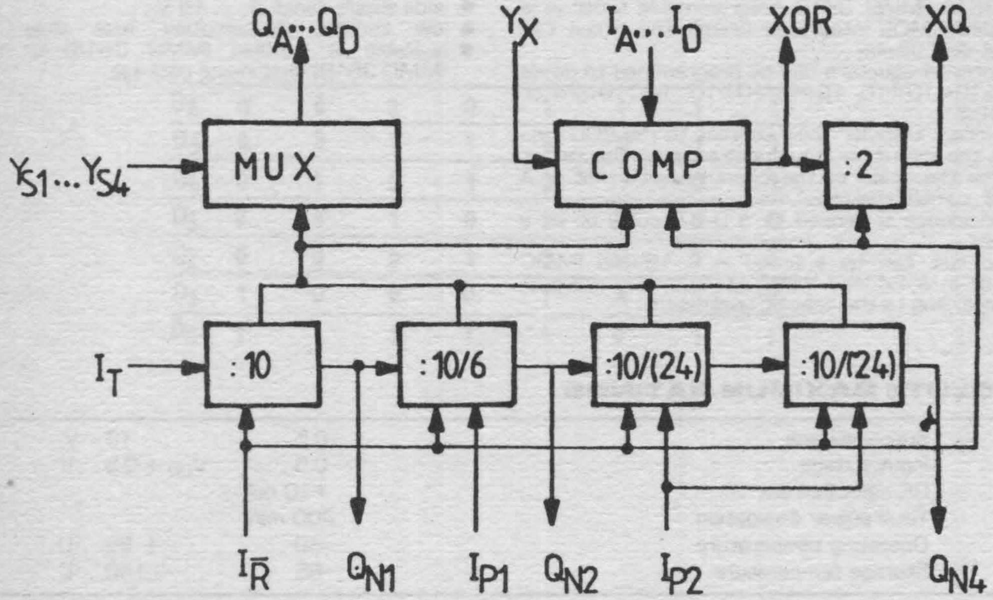
MMC 361A



MMC 361B



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The clock input, I_T, is applied to a chain of 4 counters at rates in the range 0 ... 100 Hz.
According to the connection to V_{SS} of the inputs I_{P1}, I_{P2}, the counters can be programmed to divide by:

10⁎10⁎10⁎10	— I_{P1}, I_{P2} not connected
10⁎6⁎10⁎10	— I_{P1} to V_{SS}, I_{P2} not connected
10⁎10⁎24	— I_{P2} not conected, I_{P2} to V_{SS}
10⁎6⁎24	— I_{P1}, I_{P2} to V_{SS}

The transfer from the outputs of the 4 counters to the BCD outputs of the circuit, Q_A ... Q_D, is controlled by the 25% duty cycle, 1 KHz frequency multiplexing signals Y_{S1} ... Y_{S4}.
The circuit compares the state of the counters with the information received at the I_A ... I_D inputs from 4 „tumbles-witches", controlled by the multiplexing signals Y_{S1} ... Y_{S4}.
In order to sense coincidence, a signal of period equal to the width of the multiplexing signals Y_{S1} ... Y_{S4} is applied at input Y_X to a chain of 2 flip-flops inside the compare logic.
The coincidence is sensed as a pulse 0—1—0 at XOR output and as a step 0—1 at XQ output; in order to directly drive LEDs, these outputs have NPN bipolar transistors connected to V_{DD}.
A low level on the $I_{R/}$ input resets to 0 the flip-flops of the circuit; Schmitt Trigger action on this input permits unlimited clock rise and fall times.
For the option in 16-lead package (MMC 3621A), the programming input I_{P2}, the BCD outputs Q_A ... Q_D and the serial outputs Q_{N1} ... Q_{N4} are not connected.

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (µA)	V_{DD} (V)	VALUES T_{LOW} min.	T_{LOW} max.	25°C min.	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5 0/10 0/15 0/20			5 10 15 20		20 40 80 400		20 40 80 400		600 1200 2400 12000	µA
		E, F types	0/ 5 0/10 0/15			5 10 15		80 160 320		80 160 320		600 1200 2400	µA
V_{OH}	Output high voltage		0/ 5 0/10 0/15		< 1 < 1 < 1	5 10 15	4 9 14		4 9 14		4 9 14		V
V_{OL}	Output low voltage		5 /0 10/0 15/0		< 1 < 1 < 1	5 10 15		0.05 0.05 0.05		0.05 0.05 0.05		0.05 0.05 0.05	V
V_{IH}	Input high voltage			0.5/4.5 1/9 1.5/13.5	< 1 < 1 < 1	5 10 15	4.95 9 12		4.95 9 12		4.95 9 12		V
V_{IL}	Input low voltage			4.5/0.5 9/1 13.5/1.5	< 1 < 1 < 1	5 10 15		1.35 1.9 2.7		1.35 1.9 2.7		1.35 1.0 2.7	V
I_{IH}	Input leakage curent	G, H types	0/18			18		.1		.1		1.0	µA
		E, F types	0/15			15		.3		.3		1.0	µA
I_{IL}	Input leakage curent	G, H types	0/18			18		.25		.25		2.5	mA
		E, F types	0/15			15		.75		.75		2.5	mA
I_{OH}	Output drive current	G, H types	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15	–2.0 –0.6 –1.6 –4.2		–1.6 –0.5 –1.3 –3.4		–1.1 –0.3 –0.9 –2.4		mA
		E, F types	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15	–1.5 –0.5 –1.3 –3.6		–1.3 –0.4 –1.1 –3.0		–1.1 –0.3 –0,9 –2.4		mA
I_{OL}	Output sink current	G, H types	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15	0.6 1.6 4.2		0.5 1.3 3.4		0.3 0.9 2.4		mA
		E, F types	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15	0.5 1.3 3.6		0.4 1.1 3.0		0.3 0.9 2.4		mA
C_I	Input capacitance		Any input							7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES max.	UNIT
t_{PLH} YQ, t_{PHL} YQ	Propagation delay time $Y_{S1}...Y_{S4}—Q_A...Q_D$	15		750	ns
t_{PLH} IQ, t_{PHL} IQ	Propagation delay time $I_T—Q_A...Q_D$	15		3	μs
t_{TLH}, t_{THL}	Transition time $Q_A...Q_D$	15		150	ns
f_{CK}	Clock frecuency I_T	5 15		400 800	KHz

FREQUENCY DIVIDER

GENERAL DESCRIPTION

MMC 362 frequency divider is a metal gate CMOS integrated circuit. The time base of the circuit is provided by connecting a 4 MHz quartz and a RC network to the on-chip CMOS inverter/amplifier. The circuit provides multiplexing signals at a 1 KHz rate, with a 25% duty cycle, and clock signals of period .01 s, .1 s, 1 s and 1 min. The circuit is supplied in a 16-lead dual-in-line package.

FEATURES

- wide supply range: 3 . . . 18 V
- 4 MHz crystal-controlled operation
- available in 16-lead dual-in-line package

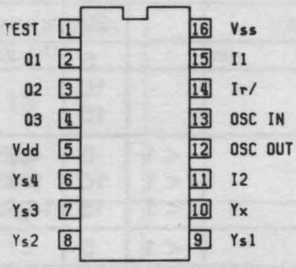
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	−0.5	...	18	V
V_I	Input voltage	−0.5	...	V_{DD} + 0.5	V
I_I	DC input current	+10 mA			
P_D	Total power dissipation	200 mW			
T_A	Operating temperature	−40	...	+ 85	°C
T_S	Storage temperature	−65	...	+150	°C

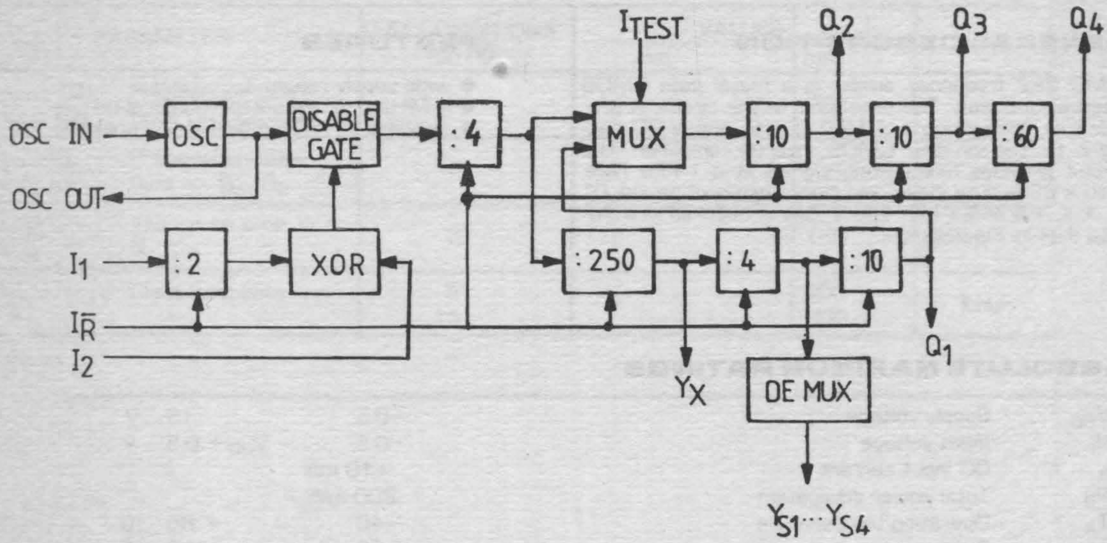
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3	...	15	V
V_I	Input voltage	0	...	V_{DD}	
T_A	Operating temperature	−40	...	+85	°C

CONNECTION DIAGRAM



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The precision tine base of the circuit is provided by connecting a 4 MHz quartz crystal and a RC network together with the on-chip CMOS inverter/amplifier. The inputs I_1, I_2 disable the access of the signal generated by the internal oscillator to the dividing chain, by a pulse applied on I_1 or by a step applied on I_2. The state after reset make access possible if I_2 is connected to V_{SS}. A low level on the $I_{\bar{R}}$ input resets to 0 the flip-flops of the circuit; Schmitt Trigger action on this input permits unlimited clock rise and fall times.

For testing purposes, I_{TEST} input connected to V_{SS} allows a 1 MHz signal to be applied to the second section of the dividing chain instead of the 100 Hz signal in normal operation.
The circuit provides 25% duty cycle, 1 KHz frequency multiplexing signals, Y_{S1} ... Y_{S4}, and a 4 KHz signal, Y_X, for timing purposes.
It also provides signals of period equal to .01 s, .1 s, 1 s, 1 min, that can be used as clock input for a timer. The circuit being mounted in 16-lead dual-in-line package, the .01 s output is not connected.

STATIC ELECTRICAL CHARACTERISTICS

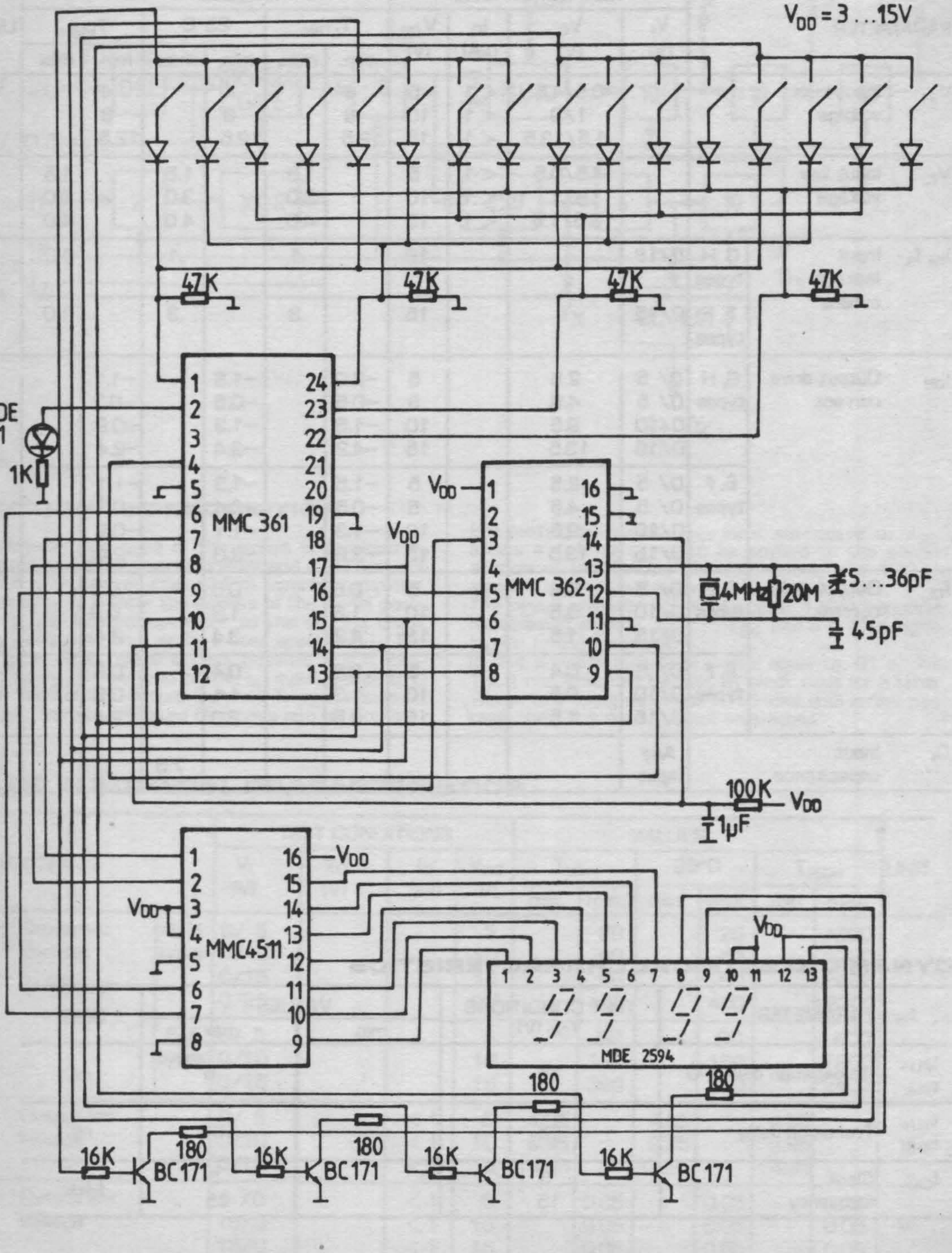
PARAMETER			V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T_{LOW} min.	T_{LOW} max.	25°C min.	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		20		20		600	μA
			0/10			10		40		40		1200	
			0/15			15		80		80		2400	
			0/20			20		400		400		12000	
		E, F types	0/ 5			5		80		80		600	
			0/10			10		160		160		1200	
			0/15			15		320		320		2400	
V_{OH}	Output low voltage		0/ 5		< 1	5	4.95		4.95		4.95		V
			0/10		< 1	10	9.95		9.95		9.95		
			0/15		< 1	15	14.95		14.95		14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05		0.05		0.05	V
			10/0		< 1	10		0.05		0.05		0.05	
			15/0		< 1	15		0.05		0.05		0.05	

STATIC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T_{LOW} min.	T_{LOW} max.	25°C min.	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
V_{IH}	Input high voltage			0.5/4.5	< 1	5	4		4		4		V
				1/9	< 1	10	8		8		8		
				1.5/13.5	< 1	15	12.5		12.5		12.5		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5		1.5		1.5	V
				9/1	< 1	10		3.0		3.0		3.0	
				13.5/1.5	< 1	15		4.0		4.0		4.0	
I_{IH}, I_{IL}	Input leakage curent	G, H types	0/18			18		.1		.1		1.0	μA
		E, F types	0/15			15		.3		.3		1.0	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2.0		−1.6		−1.1		mA
			0/ 5	4.6		5	−0.6		−0.5		−0.3		
			0/10	9.5		10	−1.6		−1.3		−0.9		
			0/15	13.5		15	−4.2		−3.4		−2.4		
		E, F types	0/ 5	2.5		5	−1.5		−1.3		−1.1		
			0/ 5	4.6		5	−0.5		−0.4		−0.3		
			0/10	9.5		10	−1.3		−1.1		−0,9		
			0/15	13.5		15	−3.6		−3.0		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.6		0.5		0.3		mA
			0/10	0.5		10	1.6		1.3		0.9		
			0/15	1.5		15	4.2		3.4		2.4		
		E, F types	0/ 5	0.4		5	0.5		0.4		0.3		
			0/10	0.5		10	1.3		1.1		0.9		
			0/15	1.5		15	3.6		3.0		2.4		
C_I	Input capacitance		Any input							7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay I-O	15		5	μs
t_{TLH}, t_{THL}	Transition delay	15		150	ns
f_{CK}	Clock frequency	5		5	MHz
		15		15	


V_DD = 3 ... 15V
47K
47K
47K
47K
MDE 1101
1K
MMC 361
V_DD
MMC 362
4MHz
20M
5...36pF
45pF
100K
V_DD
1μF
MMC4511
V_DD
MDE 2594
180
180
180
180
16K
BC171
16K
BC171
16K
BC171
16K
BC171

TV CAMERA SYNC GENERATOR

GENERAL DESCRIPTION

The MMC 371 camera sync generator is a metal-gate CMOS integrated circuit designed to supply the basic output functions for the monochrome 625 line/50 Hz and 525 line/60 Hz interlaced camera for closed TV system. The output signals are supplied for both OIRT and CCIR standards.
The MMC 371 can operate from any of two frequency sources: an internal oscillator with an external crystal or an externally applied clock signal (4 MHz for the 625 line/50 Hz camera and 4.032 MHz for the 525 line/60 Hz camera).

FEATURES

- Output functions for the monochrome 625 line/50 Hz and 525 line/60 Hz interlaced cameras.
- Output signals to control multiple camera installations
- Internal oscillator or external frequency source.

ABSOLUTE MAXIMUM RATINGS

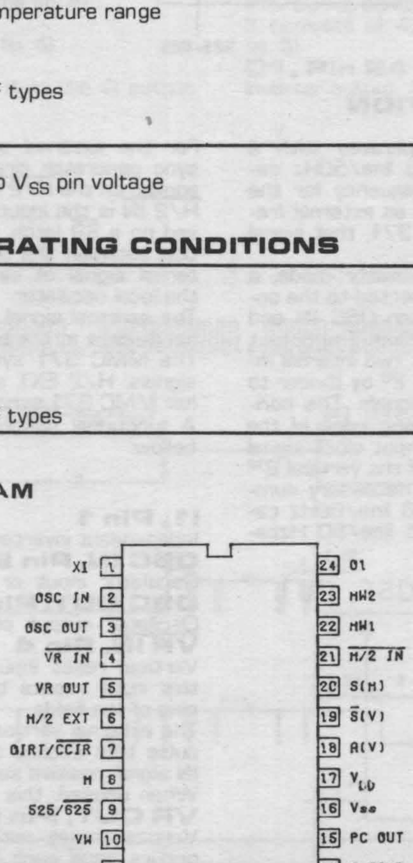
V_{DD}*	Supply voltage:	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

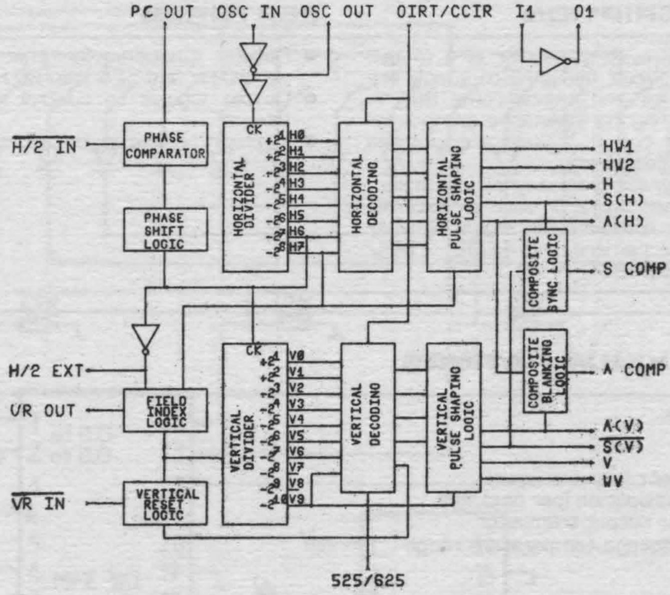
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	5 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature :	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



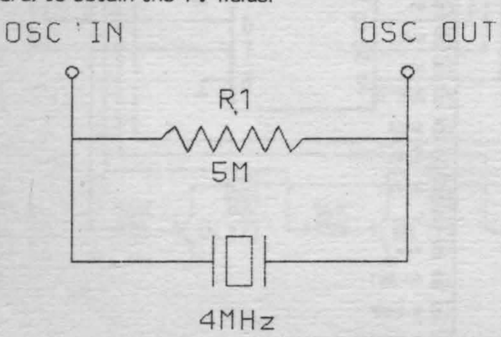
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MMC 371 sync generator operates with a 4 MHz clock frequency for the 625 line/50Hz camera, and with 4.032 MHz clock frequency for the 525 line/60 Hz camera. When using an external frequency source to operate the MMC 371, that signal should be applied at OSC IN pin.

For the operation in the crystal oscillator mode, a crystal and a resistor R must be connected to the onchip CMOS inverter/amplifier between OSC IN and OSC OUT pins, as shown in figure bellow. The output of the oscillator is cleaned up by next two internal inverters and applied on the input of a 2^8 by divider to obtain the frequency of horizontal signals. The horizontal divider is operated on the falling edge of the signal from the OSC OUT pin. The input clock signal divided by 2^7 is applied on the input of the vertical 2^{10} by divider that is reseted after the necessary number of lines 262,5 lines for the 525 line/60Hz camera and 312, 5 lines for the 625 line/50 Hzcamera) to obtain the TV fields.



For the external synchronization of the MMC 371 sync generator circuit two external signals must be applied on the H/2 IN and VR IN simultaneonly.

H/2 IN is the input of a digital phase comparator based on a $\overline{SR}$ latch. The result of the phase comparation between the external $\overline{H/2\ IN}$ signal and the internal signal of same frequency is used to control the local oscillator.

The external signal applied on $\overline{VR\ IN}$ resets the vertical dividers at the beginning of the fields.

The MMC 371 sync generator provides the output signals: H/2 EXT and VR OUT for synchronizing other MMC 371 sync generators.

A functional description of the circuit pins is given bellow:

I1, Pin 1
Independent inverter input. (See block diagram)

OSC IN, Pin 2
Osculator input or external frequency source input

OSC OUT, Pin 3
Oscilator output or inverted OSC IN signal output

$\overline{\text{VR IN}}$, Pin 4
Vertical reset input. A low level voltage applied on this input resets the vertical dividers at the beginning of the fields.

The external vertical reset signal must be a negative pulse that occurs once at two fields within the H/2 IN signal positive semiperiod.

When unused, this input must be connected to V_{DD}.

VR OUT, Pin 5
Vertical reset output. This signal is a pulse that occurs once each even field, at the leading edge of A(V) in that field (see fig. 6).

It can be used for external synchronization of other MMC 371 circuits.

H/2 EXT, Pin 6

Horizontal external sunchronization output signal (fig. 6). The frequency of this signal is twice the frequency of the horizontal signals.

OIRT/$\overline{CCIR}$, Pin 7

A logic „1" level on OIRT/$\overline{CCIR}$ selects the OIRT output functions.
A logic „0" level on OIRT/$\overline{CCIR}$ selects the CCIR output functions.

H, Pin 8

Horizontal drive output signal (see fig. 5)

525/$\overline{625}$, Pin 9

A logic „1" level on 525/625 selects the internal vertical reset for the 525 line/60 Hz camera.
A logic „0" level on 525/625 selects the internal vertical reset for the 625 line/50 Hz camera.

VW, Pin 10

Vertical write output signal, for the 625 line/50 Hz, camera.
It is a pulse that begins after 26 lines from the leading edge of A(V) and ends after 240 lines (see fig. 6).

V, Pin 11

Vertical drive output signal (see fig. 6)

A(H), Pin 12

Horizontal blanking output signal (see fig. 5)

A COMP, Pin 13

Composite blanking output signal (see fig. 4)

S COMP, Pin 14

Composite sync output signal (see fig. 4)

PC OUT, Pin 15

Digital phase comparator output. It is the Q output of a $\overline{SR}$ latch.
The signal from this output is the results of the comparation between the external $\overline{H/2}$ IN signal and the internal signal of same frequency and can be used to command the local oscillator.

V_{SS}, Pin 16

Ground

V_{DD}, Pin 17

Positive supply voltage

A(V), Pin 18

Vertical blanking output signal (see fig. 6)

$\overline{S(V)}$, Pin 19

Vertical sync output signal (see fig. 6)

S(H), Pin 20

Horizontal sync output signal (see fig. 5)

H/2 IN, Pin 21

Horizontal external synchronization input signal. This signal is applied on the $\overline{S}$ input of a $\overline{SR}$ latch for digital phase comparation (see also PC out, Pin 15). The frequency of the external H/2 IN signal is twice the frequency of horizontal signals.
When unused, H/2 IN will be connected to V_{SS}.

HW1, Pin 22

„Horizontal Write 1" output signal, for the 625 line/50 Hz camera.
It consists of 80 pulses of 0,5 μs each on a line, (see fig. 5).

HW2, Pin 23

„Horizontal Write 2" output signal, for the 625 line/50 Hz camera.
It consists of 40 pulses of 1 μs each on a line, (see fig. 5).

O1, Pin 24

Inverter output. (See block diagram)

TIMING DIAGRAMS

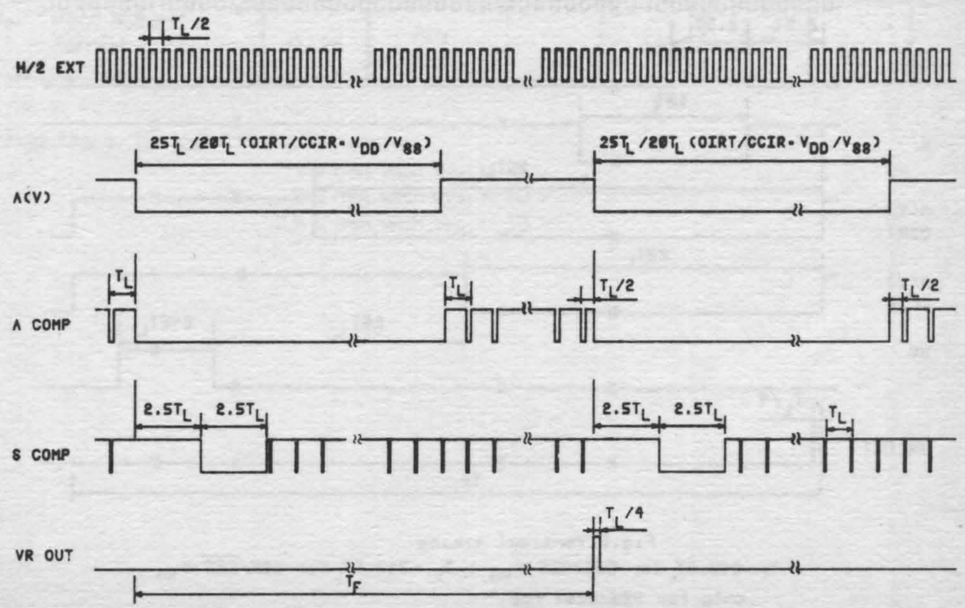


Figure 4

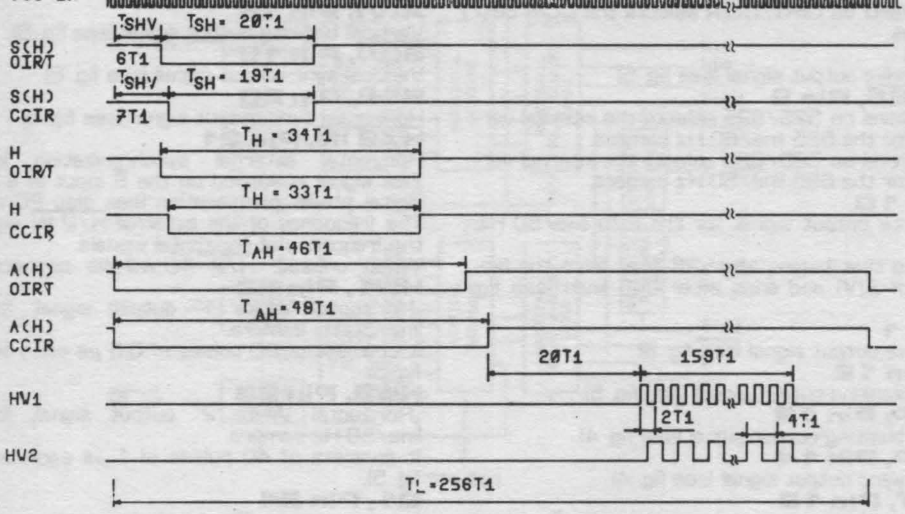


Fig. 5 Horizontal timing fo is the clock frequency

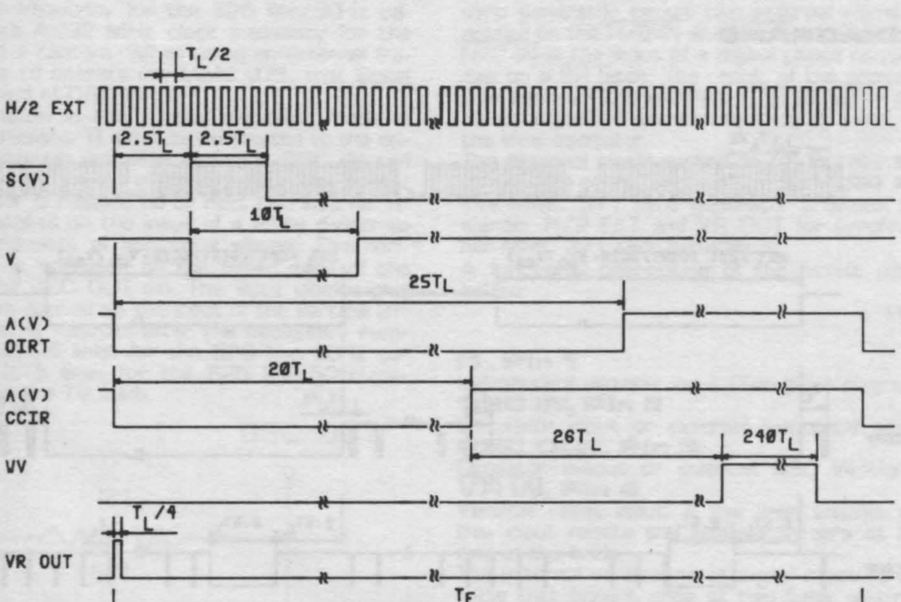


Fig.6 Vertical timing

$T_F = 262.5T_L$ for $525/625 = V_{DD}$; $T_F = 312.5T_L$ for $525/\overline{625} = V_{SS}$.

only for $525/625 = V_{SS}$.

STATIC ELECTRICAL CHARACTERISTICS

(T_A = 25 C)

PARAMETER		TEST CONDITIONS				VALUES		UNIT
		V_I (V)	V_O (V)	I_O (uA)	V_{DD} (V)	Min.	Max.	
I_L	Quiescent current	0/5			5		200	μA
		0/10			10		400	
		0/15			15		800	
V_{IH}	Input high voltage		0.5/4.5	<1	5	3.5		V
			1/9	<1	10	7		
			1.5/13.5	<1	15	11		
V_{IL}	Input low voltage		4.5/0.5	<1	5		1.5	V
			9/1	<1	10		3	
			13.5/1.5	<1	15		4	
V_{OH}	Output high voltage	0/5		<1	5	4.9		V
		0/10		<1	10	9.9		
		0/15		<1	15	14.9		
V_{OL}	Output low voltage	5/0		<1	5		0.1	V
		10/0		<1	10		0.1	
		15/0		<1	15		0.1	
I_{OH}	Output drive current	0/5	2.5		5	0.8		mA
		0/5	4.6		5	0.3		
		0/10	9.5		10	0.6		
		0/15	13.5		15	1.5		
I_{OL}	Output sink current	5/0	0.4		5	0.3		mA
		10/0	0.5		10	0.6		
		15/0	1.5		15	1.5		
I_{IL}, I_{IH}	Input leakage current	0/15	Any input		15		±0.3	μA

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 15 pF, R_L = 200 k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_W	Clock pulse width (external frequency source)	5 10 15	115		135	ns
t_{TLH}, t_{THL}	Transition time	5 10 15			200 100 80	ns
t_{PLH}	Propagation delay from OSC IN to A(H)	5 10 15		450 200 130	650 300 200	ns
t_{PHL}	Propagation delay from OSC IN to A(H)	5 10 15		650 300 180	850 500 350	ns
t_{PLH}, t_{PHL}	Propagation delay from OSC IN to H, S(H), H/2 EXT, HW1, HW2	5 10 15		450 200 130	650 300 200	ns

FREQUENCY SYNTHESISER CONTROLLER

GENERAL DESCRIPTION

The MMC 381 is one of a pair of CMOS integrated circuits, primarly intended for use in frequency synthesiser. The complementary device is the special D/B divider for frequency synthesiser MMC 382/383.
The MMC 381 E/F/G/H tipes are supplied in the 16 lead dual-in-line ceramic or plastic packages

FEATURES

- Wide choice of reference frequency using a single crystal
- maximal reference frequency ≥ 5 MHz
- flexible programming:
  — direct interface to ROM or PROMS
  — microprocesor compatible
- wide programme range for the reference counter $6 \div 4098$
- on-chip crystal controlled oscillator
- cut-down of the power supply of ROM or PROM capabilities
- synchronisation output for switching power supply
- wide range of power supply $3V \div 18V$
- high noise immunity and low power consumption

APPLICATIONS

- Professional frequency synthetisers

ABSOLUTE MAXIMUM RATINGS

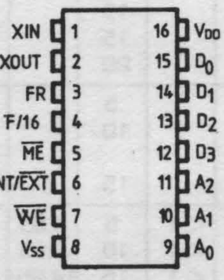
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	8	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



PIN DESIGNATION

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	XIN XOUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal generated reference signal may alternatively be applied to OSC IN. This may be a low signal AC coupled into OSC IN or it may be DC coupled if a full logic swing is available. The programme range of the reference counter is 6-4096 in steps of 2.
3	FR	Reference divider output. The output is logic high, except one period of the crystal oscillator.
4	F/16	Output of the crystal oscillator signal divided by 16 is mainly intended for use switching power supply synchronisation.
5	$\overline{ME}$	An open-drain output for use in controlling the power supply to an external ROM or PROM. The output is low during the data read period and in high impedance at other times.
6	INT/$\overline{EXT}$	This pin allows selection between internal and external programming modes. — external mode — this pin is grounded. ME output is not active, WE is a write enable input for D0—D3. — internal mode — a positive pulse on this pin initiates a programming cycle. The settle time of the external memory is controlled by the high level slot of this pulse. Its width depends on the power-up time of the external memory.
7	WE	Bidirectional write enable pin. In the internal mode the WE signal is internally generated by MMC 381 and is applied to MMC 382/383 (pin 11). In the external mode, WE is a write enable input (whitch triggers the internal data latches). When WE is going high, the input data (D0—D3) will be latched.
8	V_{SS}	Negative supply (normally ground)
9, 10, 11	A0—A2	Bidirectional data select pins — internal mode — tri-state data select outputs intended to address external memory and the MMC 382/383 — external mode — select inputs for the data latches
12—15	D0—D3	Information on these inputs is transfered in the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
16	V_{DD}	Positive supply

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		15		0.12	15		450	μA
			0/10			10		30		0.12	30		900	
			0/15			15		60		0.12	60		1800	
			0/20			20		300		0.24	300		9000	
		E, F types	0/ 5			5		50		0.12	50		450	
			0/10			10		100		0.12	100		900	
			0/15											
						15		200		0.12	200		1800	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A=25°C; C_L=50pF; R_L=200K; typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns).

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			Min.	Typ.	Max.	
t_{THL} t_{TLH}	Transition time	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V			200 100 80	ns ns ns
t_{PHL} t_{PLH}	Propagation delay time (INT/EXT to ME)	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V R_L = 200K			400 200 160	ns ns ns
f_{CL}	Maximum clock frequency	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		5 10 15		MHz MHz MHz
t_W(I)	INT/EXT command	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		200 140 100		ns ns ns
t_W(WE)	Write enable pulse width (WE)	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		120 60 50		ns ns ns
t_{SU}	Date setup time	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		80 40 30		ns ns ns
t_{P1-H} t_{P0-H}	3-state propagation delay times: output high or low to high	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V R_L = 1 K			300 150 120	ns ns ns
t_{PH-1} t_{PH-1}	Output high impedance to high or low	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V R_L = 1 K			300 150 120	ns ns ns

FUNCTIONAL DESCRIPTION

Reference oscillator

The reference oscillator normally operates with an external crystal. The internal circuitry can be used as a buffer amplifier in case an external reference should be required.

Reference divider

The reference divider is a 12 stages ripple-carry binary counter. The last 11 stages are presettable. The programme range of the reference counter is 6—4098 in steps of 2, the division ratie being the programmed number (see date map).
The programme number is loaded from the internal latches at the end os each dividing cycle. The output is logic high, except each period of the crystal oscillator.

Programming in internal mode

When in internal mode, programming information is supplied by an external ROM or PROM under the control of the MMC 381. Thirty-two data bits are required for frequency synthesiser channel organised as eight 4-bit words. (see date map).
Reading of this data is normally done in a single shot mode with the data read cycle started by a positive pulse, on the program enable pin (int/ext). A memory enable signal is supplied to allow power-down of the memory when not in use. The power-up time of the memory is provided during the positive logic slot of the memory enable pulse. This delay does not depend on the crystal oscillator frequency and is easily correlated with the type of memory in use.

DATA MAP

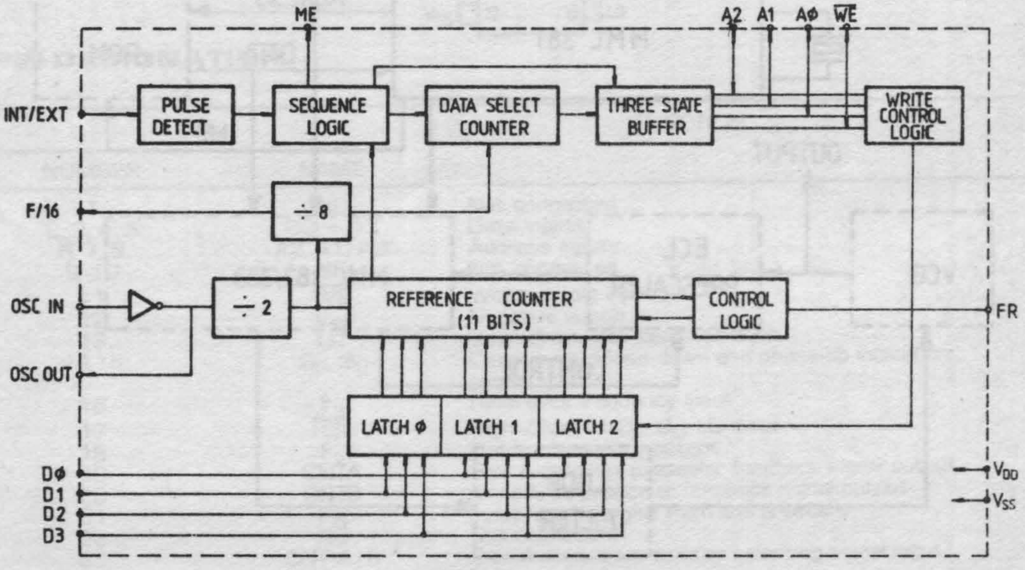
WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	A3	A2	A1	A0
2	0	0	1	B3	B2	B1	B0
3	0	1	0	C03	C02	C01	C00
4	0	1	1	C13	C12	C11	C10
5	1	0	0	C23	C22	C21	C20
6	1	0	1	D3	D2	D1	C30
7	1	1	0	D7	D6	D5	D4
8	1	1	1	D11	D10	D9	D8

The data read cycle is generated from a program clock at 1/16 th of the reference oscillator frequency.
During programming, the division rate will be neither the old one nor the new one. In order to minimize the time of out-of-lock operation, the read cycle is triggered by the output signal.
Data select outputs and WE output remain in a high impedance state when the read cycle is completed to release the data select bus (to allow the address bus to be used for other functions if desired).

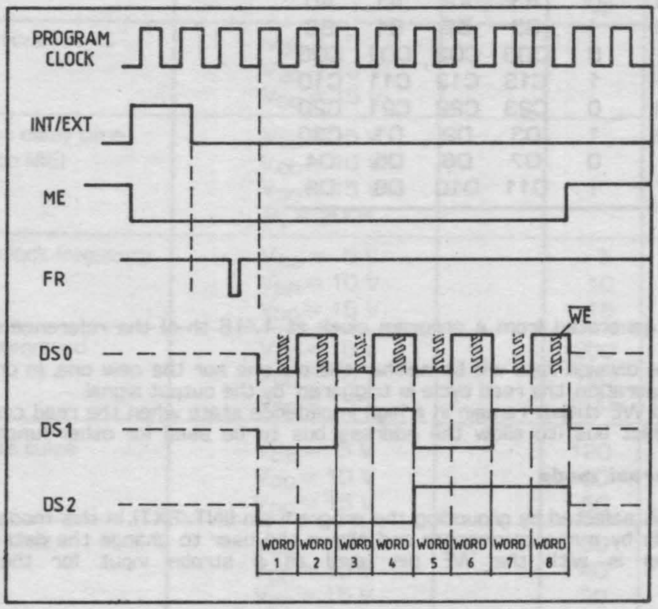
Programming in external mode

This mode of operation is selected by grounding the program pin (INT/EXT). In this mode timing is generated externally, normally by a microprocessor and allows the user to change the data in appropriated latches. The data map is with the WE pin used as a strobe input for the data latches.

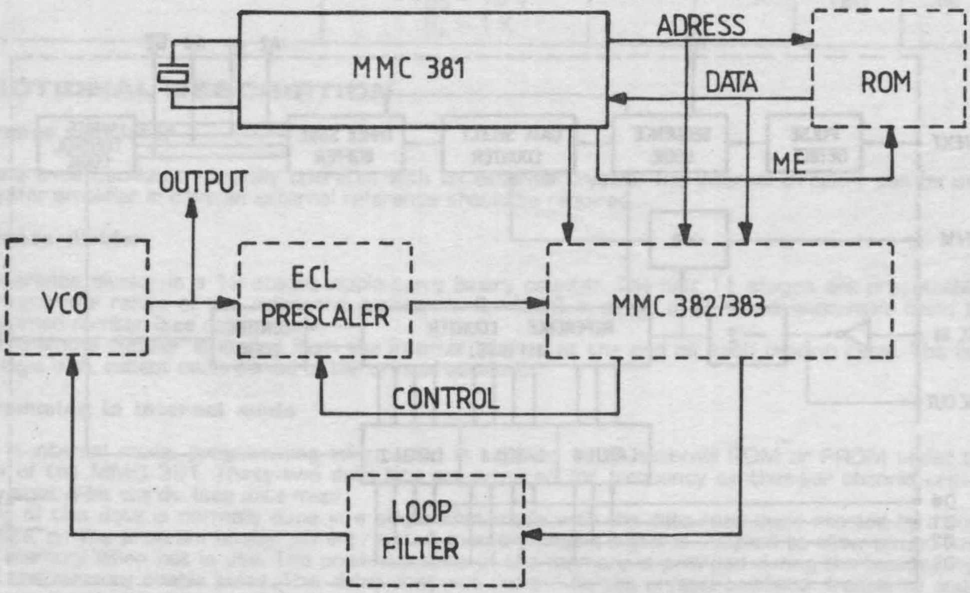
BLOCK DIAGRAM



DATA SELECTION



TYPICAL APPLICATION



BINARY/DECIMAL SPECIAL DIVIDER FOR FROQUENCY SYNTHESIS

GENERAL DESCRIPTION

The integrated circuits MMC 382 and MMC 383 are designed in order to form (either of them) with the IC MMC 381 the central unit of a phase locked loop (PLL) frequency synthesis system. If necessary the system may be microprocessor controlled.
The integrated circuit MMC 382/383, together with a prescater form a fully programmable divider. For that it generates feedback signales for a 2 or 4 modulus prescaler. The integrated circuit MMC382/383 contains a phase and freqvency comparator.
In this the divided frequency is compared with the reference frequence (likely generated by MMC 381), resulting an error signal which properly processed and filtered, controls the VCO.

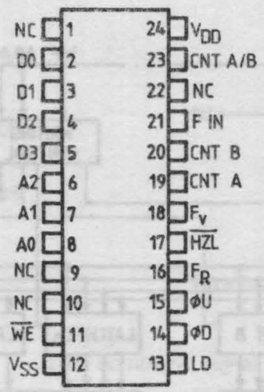
FEATURES

- Maximum input signal frequency: ≥9 MHz (V_{DD} =15 V)
- Control signals for a 2 modulus prescaler (up to 128/129) or for a 4-modules prescaler (typically 100/101/110/111), selectable by user.
- Binary (MMC 383) or decimal (382) programming of the dividing rates.
- In decimal configuration (MMC 382) the circuit can be manually programmed with 10 position multiplexed switches (BCD coded).
- It is included a phase and frequency comparator wich can be disabled by user with outputs in high Z state.
- High noise imunity
- Low supply current (<2.5 mA/V_{DD}=5 V for any dividing rates with t_{FIN}=3 MHz)
- Wide power supply voltage range: 3÷18 V

APPLICATIONS

- Telecommunication systems: radio stations, radiotelephones, radiotelegraphy, professional radioreceivers.
- Programmable dividing in control systems
- Equal frequency and different filling factors signals generation.

CONNECTION DIAGRAM



PIN DESIGNATION

PIN NUMBER	PIN NAME	FUNCTION
1	NC	Not connected
2, 3, 4, 5	DØ ÷ D3	Data inputs
6, 7, 8	A2, A1, AØ	Address inputs
9, 10	NC	Not connected
11	$\overline{WE}$	Write enable input
12	V_{SS}	Negative supply
13	LD	Open-drain, lock detected output
14,15	$Ø_D$, $Ø_U$	Open-drain, phase-down and phase-up indication outputs
16	F_R	Reference frequency input
17	$\overline{HZL}$	High-Z lock of $Ø_U$, $Ø_D$, LD input
18	F_V	Divided frequency output
19	CNTA	2 or 4-modulus prescaler feedback signal output
20	CNTB	4-modulus prescaler feedback signal output
21	F_{IN}	Input for the signal from the prescaler
22	NC	Not connected
23	CNT A/B	2 or 4-modules prescaler selecting signal input
24	V_{DD}	Positive supply

ABSOLUTE MAXIMUM RATINGS

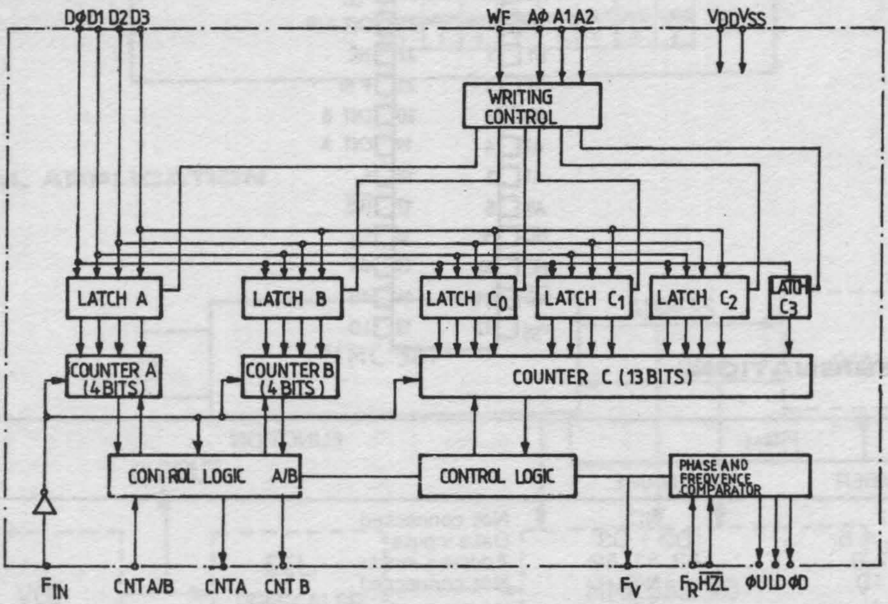
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

BLOCK DIAGRAM



DATA MAP

WORD	A2	A1	A0	D3	D2	D1	D0	LATCH
1.	0	0	0	A3	A2	A1	A0	A
2.	0	0	1	B3	B2	B1	B0	B
3.	0	1	0	C03	C02	C01	C00	C0
4.	0	1	1	C13	C12	C11	C10	C1
5.	1	0	0	C23	C22	C21	C20	C2
6.	1	0	1	X	X	X	C30	C3
7.	1	1	0	X	X	X	X	—
8.	1	1	1	X	X	X	X	—

X = DON'T CARE

FUNCTIONAL DESCRIPTION

The programmable dividing block of the VCO's frequency

This stage consists of two 4 bit programmable counters (A and B), a 13 bit programmable counter (C) and control logic. Each counter has a latch-typ memory for the inserted programmed numbers (see data map).
The address inputs A0—A2 select only one internal latch wich stores the dates at inputs D0—D3 during the "low" level of the write enable signal WE.
The C counter of MMC 382 is $3^1/_2$ digit decimal counter with a dividing ratio between 2 and 2001.
The C counter of MMC 383 is a 13 bit binary counter with a dividing ratio between 2 and 8193.
When CNT A/B is "low" the A and B counters operate separately with a clock signal from the F_{IN} input, generating two output signals (CNT A and CNT B) for a 4 modulus prescaler.
At the beginning of a dividing cycle the outputs CNT A and CNT B are "low" and remain in this state for a number of clock periods equal to the programmed then the outputs pass to "high" until the end of the dividing cycle of the C counter.
The F_V output is "high" excepting a single period of the signal applied to the input F_{IN}, when it passes to "low" pointing out the end of a cycle of the C counter and loading of the programmed numbers of the internal memories in the A, B, C counters.
In order to have a correct dividing, the numbers programmed for each counter should satisfy the following conditions:

$$C \geq A+1 \quad \text{and} \quad C \geq B+1$$

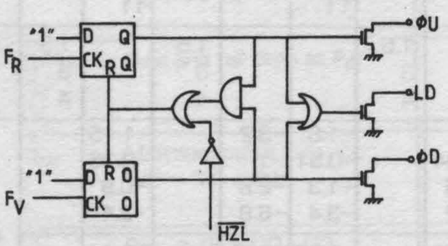
By means of a 100/101/110/111 prescaler the dividing ratio is obtained:

$$N = A + 10B + 100C$$

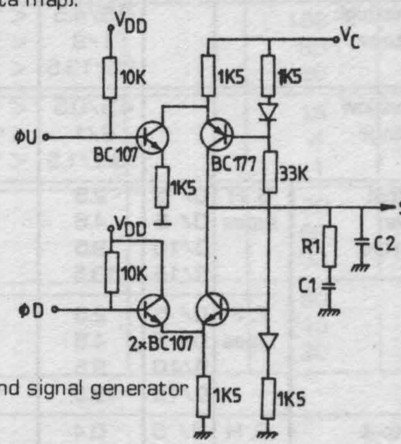
With $C \geq 10$ it is posible to obtain any dividing state in the range of:

$$1000 \div 200{,}199 \quad \text{for} \quad \text{MMC 382}$$
$$1000 \div 819{,}399 \quad \text{for} \quad \text{MMC 383}$$

When the CNT A/B input is "high" the A and B counters are together forming a 7 bit (E) programmable counter. In this case the first cell of the B counter is not used. In the E counter the most significant bit (MSB) is B_3 and the last significant bit (LSB) is A_0 (see data map).



Phase and frequency comparator



VCO command signal generator

The E counter delivers a control signal al the CNT A output for a prescaler with 2 dividing ratioes P/P+1, where $P \leq 128$.
In order to have a correct dividing the numbers programmed for each counter should satisfy the condition $C \geq E+1$.
By means of a P/P+1 prescaler it is possible to obtain a dividing ratio $N = E + C \times P$.
By means of a 128/129 prescaler and $C \geq 128$ it is possible to obtain any dividing ratio in the range of:

$2^7 = 128 \div 256{,}255$ for MMC 382
$2^7 = 128 \div 2^{20} + 2^8 - 1 = 1{,}048{,}831$ for MMC 383

Phase and frequency comparator

An internal output of the C counter (which externally goes to the pin F_V) and the F_R input (connected to the reference signal divider of the circuit MMC 381) are connected to a phase and frequency comparator. This generates signals at 3 open drain outputs: U, D and LD.
When the input signals are in phase the outputs ϕ_U, ϕ_D and LD are in a high-Z state, excepting very narrow pulses ($<$100ns) at V_{SS}.
When the input signals are not in phase, and the outputs ϕ_U, ϕ_D and LD are connected through resistances at V_{DD}, the mean voltage at the outputs ϕ_U, ϕ_D provides information about the phase and frequency error.
When $f_{FV} > f_{FR}$, the mean voltage at ϕ_U is higher than the one at ϕ_D, and viceversa. By external processing of the information it is possible to obtain a command signal for the voltage controlled oscillator (VCO); an example is shown in fig. below. As the phase and frequency error decreases in any way ($f_{FV} > f_{FR}$ or $f_{FV} < f_{FR}$) the mean voltage at the LD output increases.
A "low" signal at the HZL input inhibits the comparator, driving the outputs ϕ_U, ϕ_D and LD in high-Z state

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		15		0.12	15		450	μA
			0/10			10		30		0.12	30		900	
			0/15			15		60		0.12	60		1800	
			0/20			20		300		0.24	300		9000	
		E, F types	0/ 5			5		50		0.12	50		450	
			0/10			10		100		0.12	100		900	
			0/15			15		200		0.12	200		1800	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

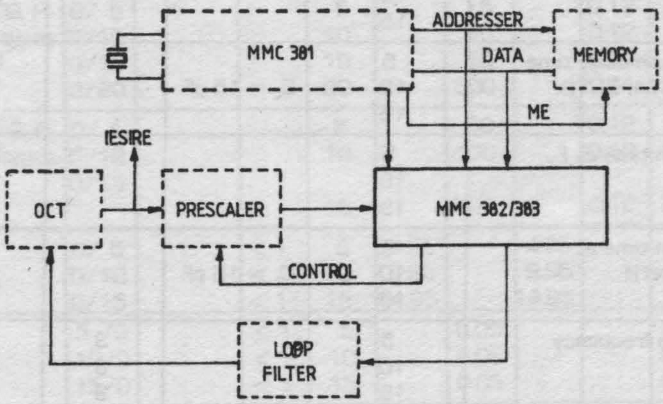
2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Values min.	Values max.	Unit
t_{PLH}, t_{PHL}	Propagation delay time F_{IN} to F_V	5			300	ns
		10			200	ns
		15			120	ns
t_{PLH}, t_{PHL}	Propagation delay time F_{IN} to CNTA, CNTB	5	$C_L = 15$ pF		240	ns
		10	$C_L = 15$ pF		120	ns
		15	$C_L = 15$ pF		90	ns
t_{THL}, t_{TLH}	Transition time at F_V	5			200	ns
		10			100	ns
		15			80	ns
t_{THL}, t_{TLH}	Transition time at CNTA, CNTB	5	$C_L = 15$ pF		80	ns
		10	$C_L = 15$ pF		40	ns
		15	$C_L = 15$ pF		25	ns
f_{CL}	Maximum frequency clock	5		3		MHz
		10		6		MHz
		15		9		MHz
t_W	Minimum clock pulse width at F_{IN}	5			160	ns
		10			80	ns
		15			60	ns
t_r, t_f	Rise and fall time at F_{IN}	5			15	μs
		10			4	μs
		15			1	μs
t_W	Minimum pulse WE = "0" width	5			120	ns
		10			60	ns
		15			50	ns
t_{SU}	Set-up time D0—D3, A0—A2 to WE	5			80	ns
		10			40	ns
		15			30	ns

TYPICAL APPLICATIONS



SAMPLE AND HOLD PHASE COMPARATOR

GENERAL DESCRIPTION

The integrated circuit MMC 384 compares the phase of a V signal to the phase of a reference R signal into two comparators: one sample and hold, high gain, digital-analogue, and the other digital. The circuit also contains a phase modulator for V signal which generates a V' signal whose phase is compared to the phase of the R signal into the two comparators.

FEATURES

- Externally adjustable high gain ($\sim$3000 V/cycle at V_{DD} = 10 V)
- Built-in phase modulator
- Operation possible with an active loop filter
- High noise immunity
- Low consumption (static supply current <3 mA/V_{DD} = 10 V)
- Wide power supply range (5 ÷ 18 V)

APPLICATIONS

The circuit can be used in any phase loked loop system.
The main utility field is the telecommunication systems which use frequency synthesis: radio stations, radiotelegraphy, radiotelephony, professional radioreceivers.

ABSOLUTE MAXIMUM RATINGS

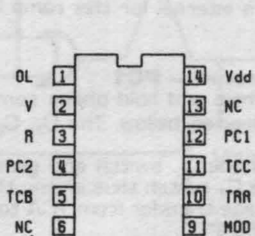
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_i	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

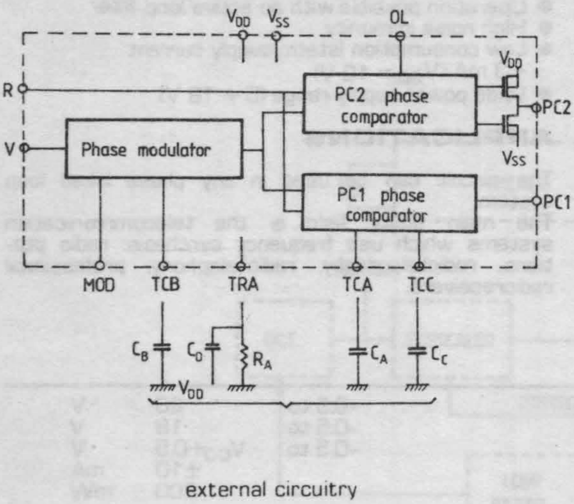
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3	to	18	V
		E and F types	3	to	15	V
V_I	Input voltage		0	to	V_{DD}	V
T_A	Operating temperature:	G and H types	−55	to	125	°C
		E and F types	−40	to	85	°C
R_A	External biasing resistor		V_{DD}= 5V		≥ 350	kΩ
			V_{DD}= 8V		≥ 85	kΩ
			V_{DD}=10V		≥ 45	kΩ
			V_{DD}=12V		≥ 35	kΩ
			V_{DD}=15V		≥ 22	kΩ

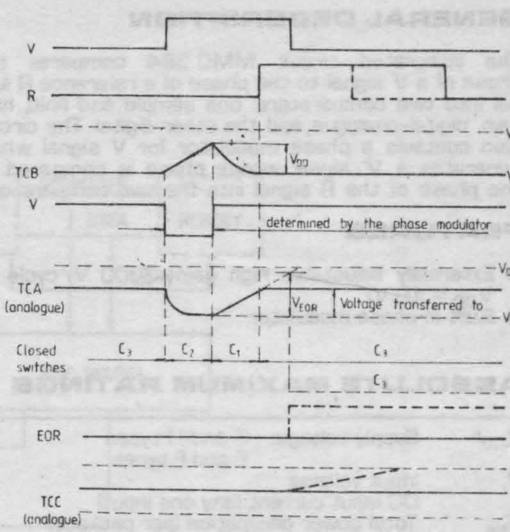
CONNECTION DIAGRAM



BLOCK DIAGRAM



TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

The block diagram of the circuit MMC 384 consists of PC1 digital-analogue comparator a PC2 digital comparator, and a phase modulator.
The modulator and sample and hold phase comparator (PC1) contain analogue circuitry.
The supply of these stages is made by means of current mirrors which multiply or divide at the required values the I current which flows through a R_A resistance connected between the TRA pin and ground.
The I current value is given by the formula:

$$I = \frac{V_{DD} - V_{SS}^{-3}}{R_A} \quad \text{(see Note 1)}$$

Phase modulator
The phase modulator is a digital-analogue circuitry which uses a C_B external capacitor connected to the TCB. The rising edge of the V signal determines a falling-edge (inactive) of V′ signal and a voltage ramp at the TCB pin.
When the voltage at the TCB pin equals the one applied to the MOD pin an internal comparator determines a rising edge (active) of the V′ signal. This implies the end of the ramp at the TCB pin and the discharge of the C_B capacitor.
So a controlled delay of the V signal is obtained.
charge of the C_B capacitor. So a controlled delay of the V signal is obtained.
When applying a modulating signal to MOD, a liniar phase modulation is generated. The modulator gain is determined by the C_B capacitor value (see Note 1):

$$K_{mod} = \frac{C_B \cdot R_A \cdot f_V}{18(V_{DD} - V_{SS} \cdot 3)} \qquad \text{cycles/V}$$

where f_V is the frequency of the signal applied at the V input.
On the TCB prin voltage ramp the C_A capacitor should discharge.
Thus in a given configuration a minimum internal for this ramp is required, namely a minimum level for the MOD voltage.

The sample and hold phase comparator — PC1
The block diagram of the analogue sample and hold phase comparator and the phase characteristics of the PC1 comparator are shown in figures bellow. The C_1, C_2, C_3 analogue switches are closed just one in a while.
The rising edge of the V′ signal closes the C_1 switch and generates a voltage ramp at the TCA pin.
The rising edge of the R signal opens the C_1 switch thus ending the slope. At the same time C_3 switch closes, which enables the voltage transfer from TCA to TCC pin. If the ramp ends before the rising edge of the R signal, when:

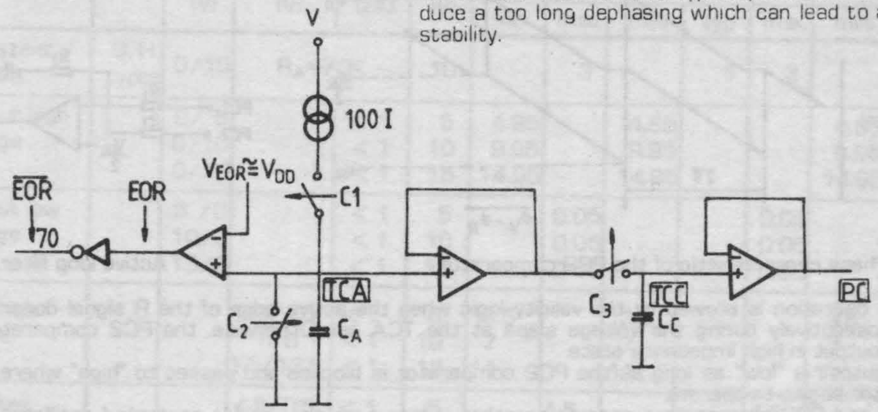
$$V_{TCA} = V_{EOR} < V_{DD}$$

Note 1: The formula is correct only in the recommended operating conditions.

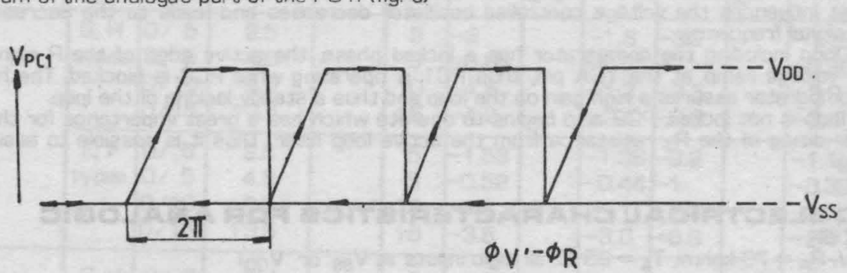
an end of ramp (EOR), signal is internally generated, which closes the C_3 switch and starts the PC2 digital phase comparator.
The phase comparator gain is given by the C_A capacitor value (see Note 1):

$$K_\phi = \frac{105(V_{DD}-V_{SS}-3)}{C_A . R_A . f_V} \quad \text{V/cycle}$$

The C_C hold capacitor value should be chosen as, in connection with the output impedance of the MMC 384 TCC terminal (typically 700 Ω), not to introduce a too long dephasing which can lead to a loop instability.

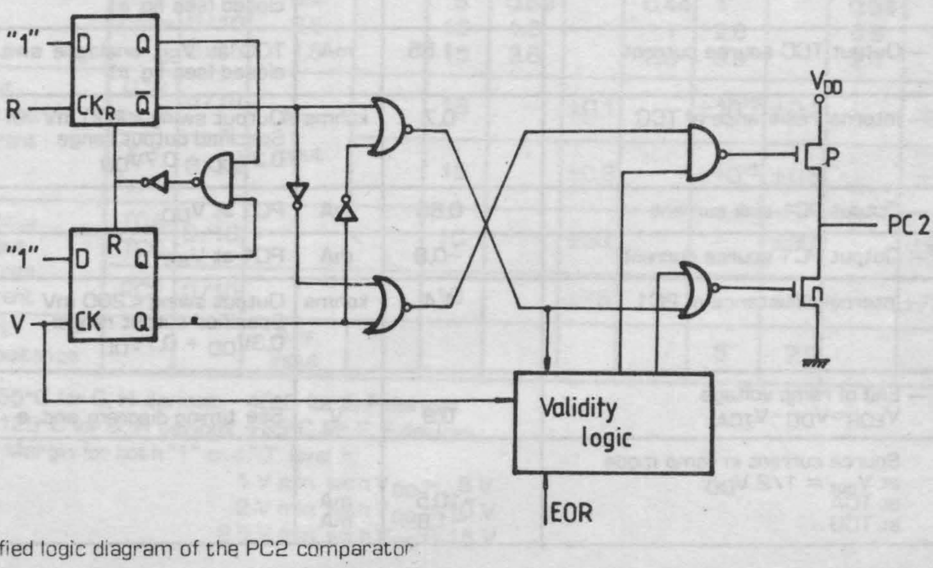


Block diagram of the analogue part of the PC1. (fig. a)



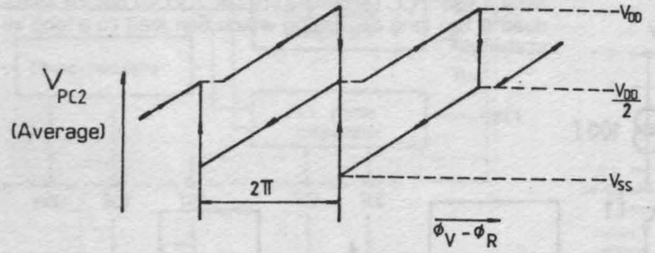
Phase caracteristics of the PC1 comparator.

PC2 — Digital phase comparator

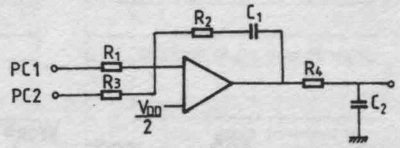


Simplified logic diagram of the PC2 comparator.

The N and P channel MOS transistors from the PC2 output are connected as analogue switches. Thus at this output it is possible to obtain positive and negative voltage pulses which depend on the sign and size of the dephasing between the R and V′ signals. During the voltage ramp at the TCA pin, namely within the area where the PC1 comparator operates, the PC2 comparator output is blocked in the high impedance state. The mean voltage obtained by through integration at the PC2 output linearly depends on the dephasing between the R and V′ signals.



Phase characteristic of the PC2 comparator.



Active loop filter.

The PC2 operation is allowed by the validity logic when the active edge of the R signal doesn't appear twice consecutively during the voltage slape at the TCA pin. Otherwise, the PC2 comparator blocks with the output in high impedance state.
The OL output is "low" as long as the PC2 comparator is blocked and passes to "high" where the PC2 comparator begins to operate.
The PC1 and PC2 comparators operate together in loop upon the voltage controlled oscillator (OCT) by means of an active loop filter. This filter reverses the phase of the signals from PC1 and PC2 and assures the proper operation of the signal. For example, if the phase difference $\phi_V - \phi_R$ increases, the voltage that influences the voltage controlled oscillator decreases and leads to the decreasing of the generated signal frequency.
When the loop including the comparator has a locked phase, the active edge of the R signal appears during the voltage ramp at the TCA pin, thus PC1 is operating while PC2 is blocked. The high gain of the PC1 comparator assures a high gain on the loop and thus a steady locking of the loop.
When the loop is not locked, PC2 also begins to operate which has a great importance for the loop gain by a proper sizing of the R_3 resistance from the active loop filter. Thus it is possible to assure a quick loop locking.

STATIC ELECTRICAL CHARACTERISTICS FOR ANALOGIC BLOCKS

(V_{DD} = 10V, R_A = 70 kohmi, T_A = 25°C, all logic inputs at V_{SS} or V_{DD})

PARAMETER		VALUE	UNIT	CONDITIONS
I_{OH}	— Output TCC sink current	1,8	mA	TCC at V_{DD}, analogue switch C_3 closed (see fig. a)
I_{OL}	— Output TCC source current	−1,65	mA	TCC at V_{SS}, analogue switch C_3 closed (see fig. a)
R_i	— Internal resistance of TCC	0,7	kohms	Output swing <200 mV Specified output range $0{,}3V_{DD} \div 0{,}7V_{DD}$
I_O	— Output PC1 sink current	0,85	mA	PC1 at V_{DD}
I_O	— Output PC1 source current	−0,8	mA	PC1 at V_{SS}
R_i	— Internal resistance of PC1	1,4	kohms	Output swing <200 mV Specified output range: $0{,}3V_{DD} \div 0{,}7V_{DD}$
V_{EOR}	— End of ramp voltage $V_{EOR}=V_{DD}-V_{TCA}$	0,9	V	See timing diagram and a
I_O	Source current in ramp mode at V_{out} = 1/2 V_{DD}: at TCA at TCB	 −10,5 −1,8	 mA mA	

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

	PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/10	R_A=70K		10		3		1	3		5	mA
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
I_{OH}	3-state output leakage current	TCA TCC	0/10			10		±30			±30		±90	nA
		PC2	0/10			10		±75			±75		±750	nA
C_I	Input capacitance			Any input						5	7.5			pF

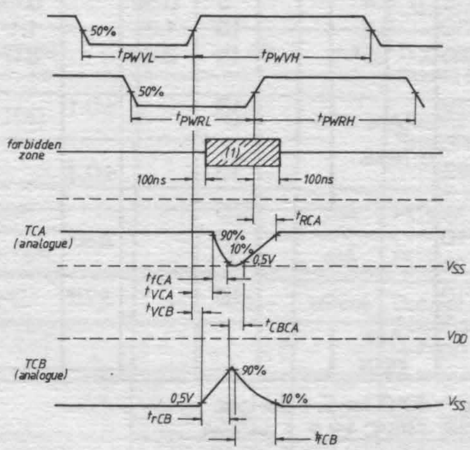
* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

Dinamic electrical characteristics are given for the integrated current connected as shown in fig. 2, with the following for the external components: R_A=70 kΩ±30%, C_A=270 pF, C_B=150pF, C_C=1nF, C_D=10nF, în conditions: V_{DD}=10V, T_A=25°C, t_r,t_f at inputs 20ns.

PARAMETER		CONDITIONS		TYPICAL VALUE	UNIT
S_{TCA}	Slew rate at TCA	V_{out}=0.3V_{DD}...0.7V_{DD}	R_A=70kΩ−30% R_A=70kΩ R_A=70kΩ+30%	43 33 21	V/μs
S_{TCB}	Slew rate at TCB	V_{out}=0.3V_{DD}...0.7V_{DD}	R_A=70kΩ−30% R_A=70kΩ R_A=70kΩ+30%	16 11 9	V/μs
t_{CBCA}	Start of TCA ramp delay			160	ns
t_{RCA}	Delay of TCA — hold			40	ns
t_{VCA}	Delay of TCA descharge			120	ns
t_{VCB}	Start of TCB ramp delay			120	ns
t_{rCB}	TCB ramp duration		V_{MOD}=4V V_{MOD}=6V V_{MOD}=8V	400 550 700	ns ns ns
$t_{rmin.CB}$	Required TCB min. ramp duration			200	ns
t_{PWVL} T_{PWVH}	Min.V input pulse width			20 20	ns ns
t_{PWRL} t_{PWRH}	Min.R input pulse width			20 20	ns ns
t_{fCA}	TCA fall time			90-	ns
t_{fCB}	TCB fall time		V_{MOD}=5V	240	ns



(1) Forbidden one in the locked state for the positive edge of V and R and both edges of STB

EXPONENTIAL COUNTER

GENERAL DESCRIPTION

The MMC 391 is a CMOS aluminium gate, BCD up-exponential counter, design to be used in every application where it is necessary a threshold counting where the last bits are negligible. It is provided with a wide selection of ranges: 0÷999; 1000÷9999; 10000÷99999; 100000÷999999.
The counting capability is up to 10^7 and a warning is outpulsed when a threshold is reached (four thresholds available). The typical application is in portable individual particle detectors. The display drivers are not part of the circuit.

FEATURES

- capacity up to 10^7
- wide selection of range options: 10^3, 10^4, 10^5, 10^6
- low power consumption
- exponential displaying of the output
- wide supply range 3 V to 18 V

APPLICATIONS

- dosimetric
- data counting
- industrial aplications

ABSOLUTE MAXIMUM RATINGS

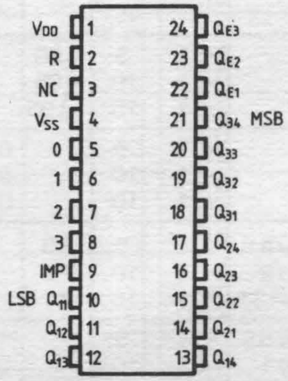
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

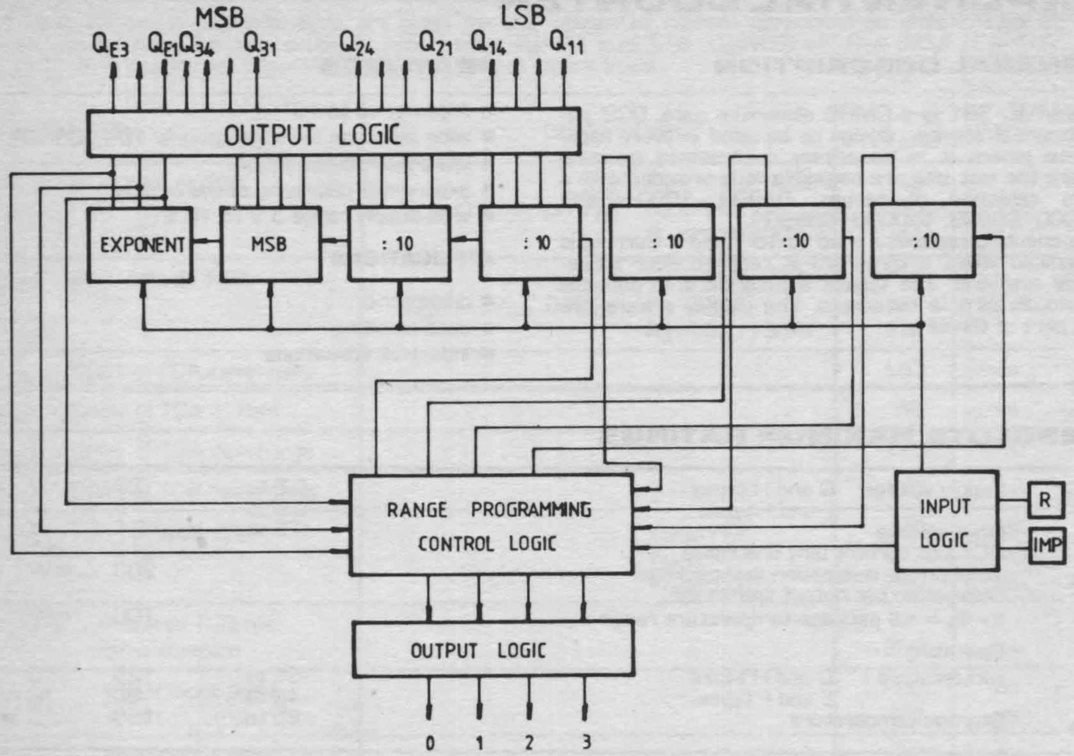
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	

	PARAMETER		TEST CONDITIONS V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

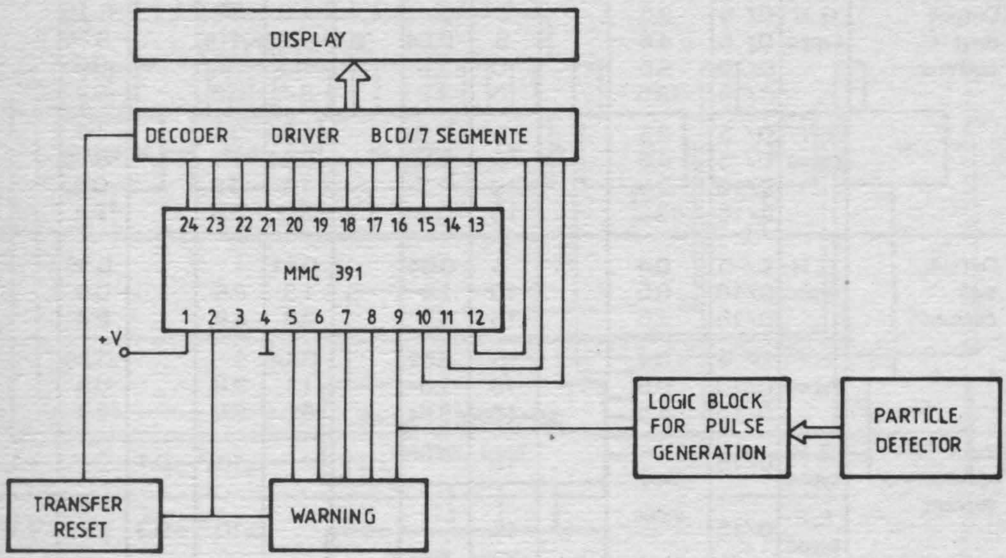
* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, R_L = 200 kΩ, all input rise and fall times = 20 ns, C_L = 50 pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C).

	PARAMETER	TEST CONDITIONS VI (V)	VALUES min.	typ.	max.	UNIT
f_{max}	Maximum opperating frequency	5		2		MHz
		15		6		
t_d	Propagation delay time (IMP to outputs)	5		270		ns
		10		150		
		15		75		
t_r	Output rise time	5		75		ns
		10		40		
		15		35		
t_f	Output fall time	5		125		ns
		10		70		
		15		50		
t_{DR}	RESET to outputs delay	5		350		ns
		10		150		
		15		100		
t_{WR}	RESET pulse width	5		300		ns
		10		100		
		15		70		

TYPICAL APPLICATION



LOOP DISCONNECT DIALLER

GENERAL DESCRIPTION

The MMC 760 Loop Disconnect Dialler provides the features to implement a pulse dialler with redial. It can be operated directly by the telephone line current and converts a single per key contact into the corresponding pulse signals to simulate the rotary dialler.
When in stand-by condition it requires only few microamperes to maintain the storage of the last call. Keyboard inputs are fully static; outputs are provided to pulse the telephone line and to mute the receiver during impulsing.
Other features are: pin selectable long distance call inhibition, 24 digit memory in wich can be introduced a maximum of 8 access pauses, pin selectable redial inhibition and out pulsing inhibition for operation with payment-card telephones.
Redial can be achieved with two pin selectable procedures.

The device requires an inexpensive 455 kHz ceramic resonator and is designed to minimize external components.
The unique design of the power-on reset circuit can avoid the need for a special dedicated spring in the hook switch.
The loop is disconnected for a time longer than 300 ms when fraudulent dialling is tried with the hook or any external device by sensing the line condition at the input LS.
The MMC 760 is realized in low voltage CMOS technology and can be easily mask programmed to meet all administration standards.

FEATURES

- Direct telephone line operation
- Low voltage CMOS technology
- Low power consumption in stand-by mode
- Pin selectable long distance call inhibition
- Pin selectable output pulsing inhibition
- 8 Selectable access pauses
- Wide selection of mask options for 1,5 — 1,6 — 1,66 — 2 B/W ratios

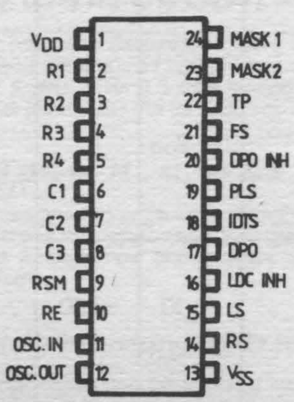
ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	5	V
V_i	Input voltage	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
P_{tot}	Total power dissipation	400	mW
T_A	Operating temperature range	−25 to +50	°C
T_{stg}	Storage temperature range	−65 to +85	°C

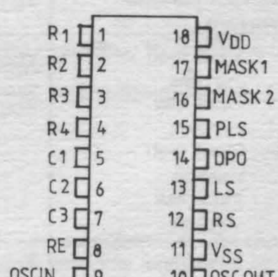
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
** All voltages are reffered to V_{SS} pin voltage.

CONNECTION DIAGRAM

MMC 760 - 1,2



MMC 760 - 3,4



STATIC ELECTRICAL CHARACTERISTICS

(T_A = −25°C to +50°C)

		PARAMETER	TEST CONDITIONS	min.	typ.	max.	UNIT
Supply	V_{DD}	Supply voltage		2.2	2.5	5	V
	I_{DD}	Operating supply current	V_{DD} = 2.5 V f_o = 455 kHz			0.5	mA
	I_{DD} stand-by	Stand-by supply current (oscillator, off, no external load connected)	V_{DD} = 2.5 V			25	μA
Keyboard inputs	Row inputs						
	In_H	Input high current	V_{DD} = 2.5 V		60	80	μA
	In_L	Input low current	V_{IH} = 2.5 V			−1	μA
	V_{IH}	Input threshold voltage	V_{IL} = 0 V	1			V
	Column inputs						
	I_{IH}	Input high current	V_{DD} = 2.5 V			1	μA
	I_{IL}	Input low current	V_{IH} = 2.5 V		−60	−80	μA
	V_{IL}	Input threshold voltage	V_{IL} = 0 V			V_{DD}−1 V	V
Oscillator	OSC IN						
	I_H	Input high current	V_{DD} = 2.5 V, V_{IH} = 2.5 V			1	μA
	I_L	Input low current	V_{IL} = 0 V			−1	μA
	OSC OUT						
	I_{OH}	Output drive current	V_{DD} = 2.5 V, V_{OH} = 2 V	−150			μA
	I_{OL}	Output sink current	V_{DD} = 2.5 V, V_{OL} = 0.5 V	150			μA
Mask output	I_{OH}	Output drive current	V_{DD} = 2.5 V, V_{OH} = 1.4 V	−1			mA
	I_{OL}	Output sink current	V_{DD} = 2.2 V, V_{OL} = 0.1 V		20		μA
DPO	I_{OL}	Output sink current	V_{DD} = 2.2 V, V_{OL} = 0.4 V	1			mA
	I_{OFF}	Output leakage current	V_{DD} = 2.5 V			+1	μA
LDC INH DPO INH PLS RSM RE	I_{IH}	Input high current	V_{DD} = 2.5 V, V_{IH} = 2.5 V			1	μA
	I_{IL}	Input low current	V_{DD} = 2.5 V, V_{IL} = 0 V			−1	μA
	V_{IH}	Input high voltage		0.7 V_{DD}			V
	V_{IL}	Input low voltage				0.3 V_{DD}	V
LS	I_{IH}	Input high current	V_{DD} = 2.5 V V_{IH} = 2.5 V			1	μA
	I_{IL}	Input low current	V_{DD} = 2.5 V V_{IL} = 0 V	−100	−160	−250	μA
	V_{IH}	Input high voltage		0.7 V_{DD}			V
	V_{IL}	Input low voltage				0.3 V_{DD}	V

		PARAMETER	TEST CONDITIONS	min.	typ.	max.	UNIT
RS	I_{OH}	Output drive current	$V_{DD} = 2.5\ V, V_{OH} = 1.8\ V$	−20			μA
	I_{OL}	Output leakage current				1	μA
	V_{IH}	Input high voltage		0.8 V_{DD}			V
	V_{IL}	Input low voltage				0.2 V_{DD}	V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = -25°C$ to $+50°C$)

	PARAMETER		TEST CONDITIONS	VALUES			UNIT
				min.	typ.	max.	
t_{ACC}	Key access time after last bounce		for all $f_0 = 455$ kHz $V_{DD} = 2.5$ V		5.5		ms
t_{OSC}	Oscillator start-up time					60	ms
t_{MASK}	Mask 1, Mask 2 pulse duration				20		ms
t_{DM}	Mask 1, Mask 2 delay time with respect to DPO				50		ms
t_{PD}	Pre-digital pause				400		ms
t_{DPO}	DPO period	FS = 0 FS = 1			50 100		ms ms
t_B/t_M	Break to make ratio				1.6		
t_{IDT}	Interdigit time	IDTS = 0 IDTS = 1			800 400		ms ms
t_{RES}	Minimum line break before reset				150		ms
t_{OTO}	Oscillator turn-off time after clear-down	LDC INH = 0 LDC INH = 1			150 300		ms ms
$t_{LDC\ INH}$	Line break time when LDC INH 1				300		ms

For the 18 pin circuit the RSM, DPOINH, FS and TP inputs are internally connected to "1" logic and the LDCINH and IDTS inputs are internally connected to "0" logic.

FUNCTIONAL DESCRIPTION

Oscillator (OS IN-OS OUT)

The oscillator has been designed to work with an inexpensive ceramic resonator ($f_0 = 455$ kHz); it requires two external load capacitors (100 pF) and the inverter feedback resistor.
The oscillator starts after LS (line sense) is taken low; it comes back to the stand-by mode after LS has gone high for at least 150 ms (or 300 ms if LDC-INH high).

Keyboard (R_1 to R_4, C_1 to C_3)

MMC 760 is designed to work with a single contact keyboard.
A valid key entry is recorded when a single row pin is connected to a single column pin. All the input combinations except a single row and a single column are not recognized. A valid key is entered after 5ms from the last key bounce.

Outpulsing inhibition (DPO INH)

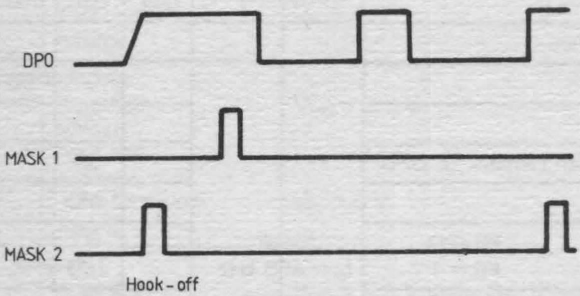
If this pin is low, digits can be entered into the memory but they are not sent on the line: when DPOINH goes high the stored digits are sent on the line. This function is realized to allow operations with payment-card telephones in which it is sometimes needed to assess the validity of the payment-card.

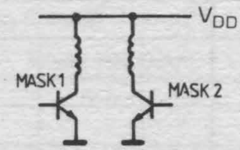
Dial pulse output (DPO)

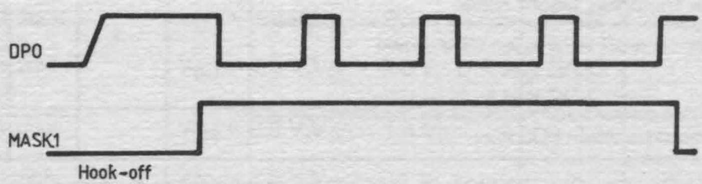
When a valid key is recognized the line must be opened and closed at a fixed rate and the total number of break pulses corresponds to the number of the selected key (10 line breaks are associated to the key „0"). DPO is an open drain output; line breaks occur when DPO is active to ground.

Mask Outputs (MASK 1, MASK 2)

The Mask outputs are used to mute the speech circuit during signalling. In telephones using conventional speech circuits muting is generally achieved by short-circuiting with a two-winding, bistable reed-relay. In this case MASK 1 and MASK 2 provide pulse outputs to drive the winding which close and open the contact respectively.
In telephones with electronic speech circuits muting is implemented electronically. In this case a metal option transforms MASK 1 into a signal which remains high throughout signalling.







Redial enable (RE)

Redial of the last call is possible according to the procedures described below only if RE is high. Redial is never allowed when RE is low.

Redial Selection Mode (RSM)

The last number redialling facility operates in two modes. In the first (RSM high) the key sequence** 0 will repeat the last number dialled. The last number memory can be cleared by the # key. In the second case (RSM low) the last number dialled is only stored if the key* is pressed before replacing the handset. As before, the sequence** 0 starts the last number repeat. In both cases the stored number is unaffected by incoming calls. The redial request can be simplified by a mask option to the single key*, instead of the sequence**0.

Pause length selection (PLS)

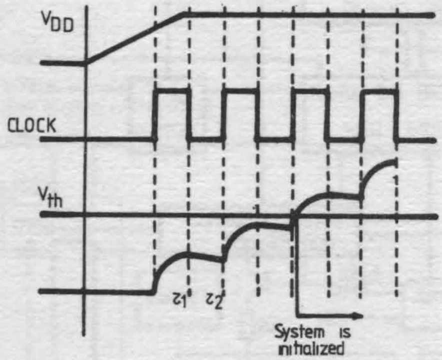
Interdigit pauses are available to interrupt outpulsing to give to the exchange the possibility of switching from a private to a public line. The device memorizes automatically a pause when the first digit is zero; a maximum of 7 pauses can be added during dialling by selecting key*. These pauses are active only during readialling and have a duration of 3 sec if PLS is low or 20 sec if PLS is high; in both cases pause duration can be shortened pushing key*.

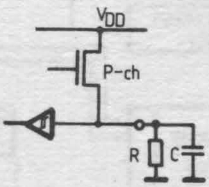
Line sense (LS)

This input senses if the line loop is closed or not
LS = high means loop open
LS = low means loop closed
When LS is kept high for more than 150 ms the circuit is reset (if LDCINH = 0). When LDCINH = 1 reset occurs after 300 ms.

Reset (RS)

This input/output pin is used to turn off the oscillator when line interrupts of more than 150 ms are sensed; it is also used as a power-on reset in applications where redial is not allowed. When the hand-set is picked-up and V_{DD} increases over its minimum value, the oscillator starts and an external capacitor is charged above a fixed threshold level by an opendrain P-ch. transistor driven by a 150 kHz clock. Reset occurs after a line interrupt of more than 150 ms; the pull-up transistor goes off and the capacitor discharges through a resistor to GND level.





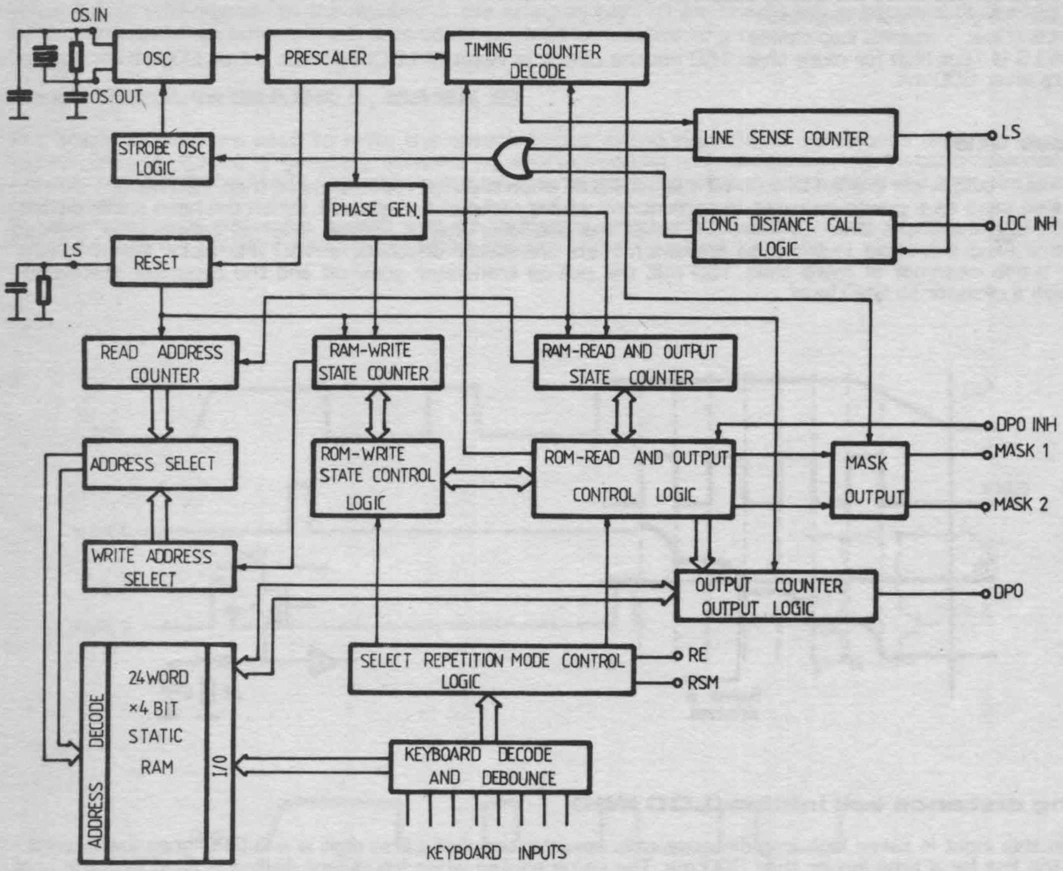
Long distance call inhibit (LDC INH)

When this input is taken high long distance calls are inhibited; if the first digit is a 0 DPO goes low interrupting the line for a time longer than 300 ms. The same applied when fraudulent dialling is tried with the hook or any external device by sensing the line condition at the input LS. When INH is low this facility is inoperative.

Test pin (TP)

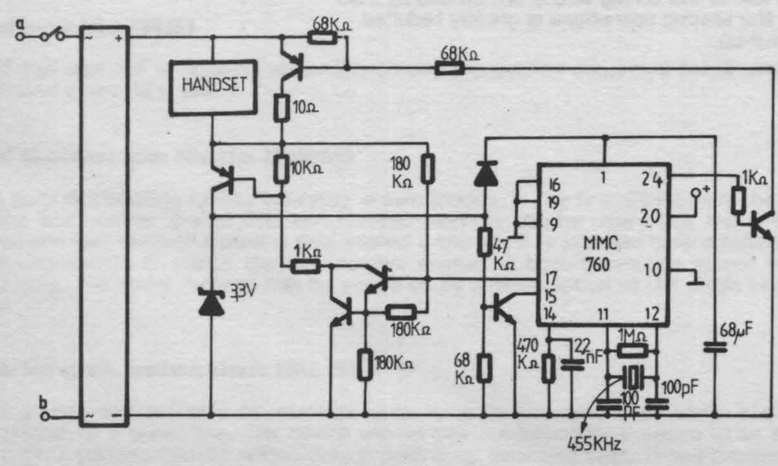
When this input is taken low all the timing values are divided by 100.
In this way the length of the testing operations is greatly reduced.
This pin has an internal pull-up.

BLOCK DIAGRAM

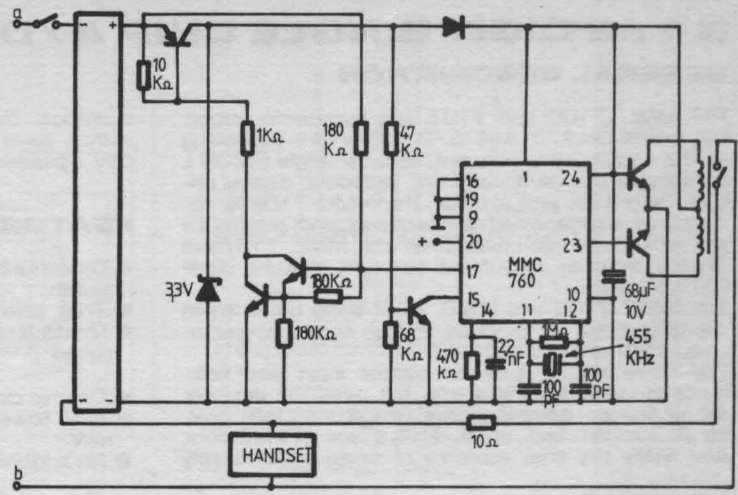


TYPICAL APPLICATIONS

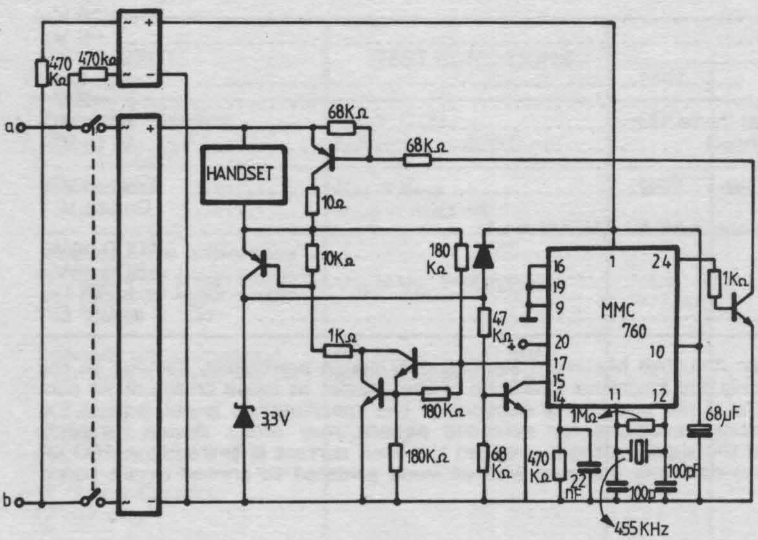
Typical serial applications



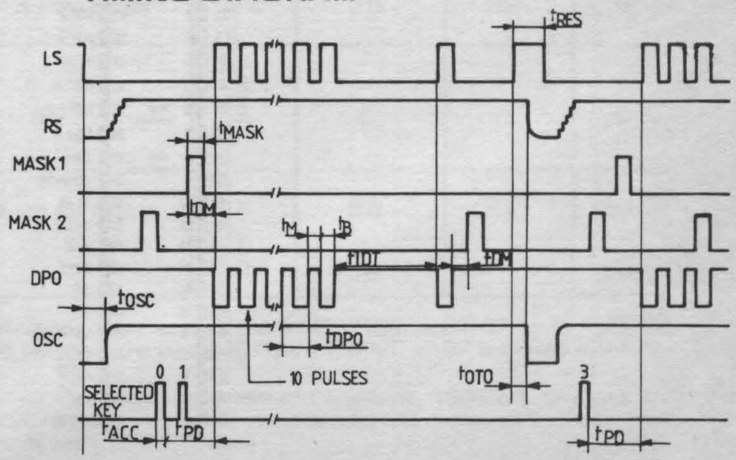
With bistable relay



Pulse dialler with redial



TIMING DIAGRAM



3 1/2 DIGIT SINGLE CHIP A/D CONVERTER

GENERAL DESCRIPTION

The MMC 7106 and 7107 are high performance, low power 3—1/2 digit A/D converters containing all the necessary active devices on a single CMOS I. C. Included are seven-segment decoders, display drivers, reference, and a clock. The MMC 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the MMC 7107 will directly drive an instrument-size light-emitting diode (LED) display.

The MMC 7106 and MMC 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy.

The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (MMC 7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and display.

FEATURES

- Guaranteed zero reading for 0 volts input on all scales.
- True polarity at zero for precise null detection.
- Direct display drive — no external components required
  — LCD MMC 7106
  — LED MMC 7107
- On chip clock and reference.
- Low power dissipation — typically less than 10 mW.
- No additional active circuits required.

ABSOLUTE MAXIMUM RATINGS

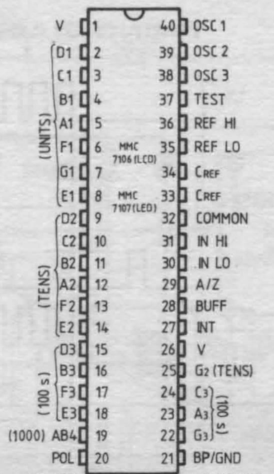
Supply Voltage (V^+)	
MMC 7106	15 V
MMC 7107	+6 V
Supply Voltage (V^-)	
MMC 7106	0V
MMC 7107	−9 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock input	
MMC 7106	Test to V^+
MMC 7107	Gnd to V^+
Power dissipation (MMC 7106 Note 2; MMC 7107 Note 1)	
Ceramic package	1000 mW
Plastic package	800 mW
Operating Temperature	0° C to + 70° C
Storage Temperature	−65° C to 85° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

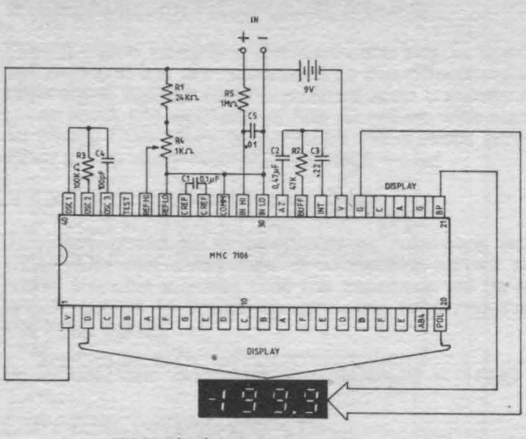
Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

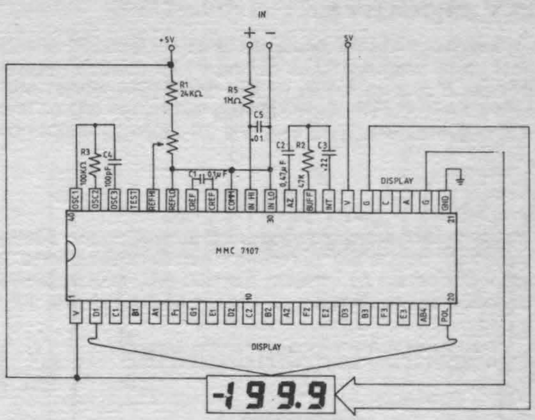
PIN CONFIGURATION



CONNECTION DIAGRAM



MMC 7106 with Liquid Crystal Display



MMC 7107 with LED Display

ELECTRICAL CHARACTERISTICS (note 3)

PARAMETER	TEST CONDITIONS	VALUES MIN	VALUES TYP	VALUES MAX	UNIT
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0 mV	−000.0	±000.0	+000.0	Digital Rading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$V_{IN} = V_{IN}$ = 200.0 mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200 mV or full scale = 2.000 V	−1	±.2	+1	Counts
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25 kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
7106 Only Pk—Pk Segment Drive Voltage Pk—Pk Backplane Drive Voltage (Note 4)	V^+ to V^- = 9 V	4	5	6	V
7107 Only Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment voltage = 3 V	5	8.0		mA
Pin 19 only		10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the MMC 7106 and 7107 at T_A = 25° C, f_{clock} = 48 kHz. MMC 7106 is tested in the circuit of Figure 1. MMC 7107 is tested in the circuit of Figure 2.

Note 4: Back plane drive is in phase with segment drive for „off" segment, 180° out of phase for „on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.

TEST CIRCUITS

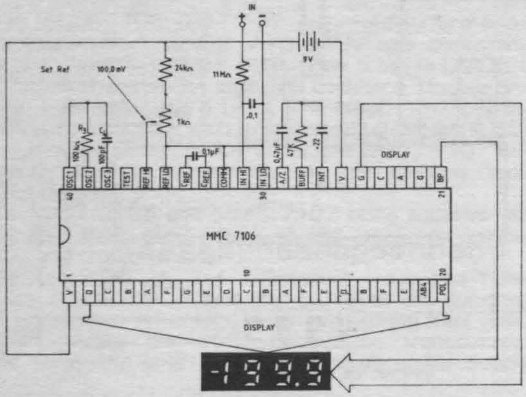


Figure 1: 7106

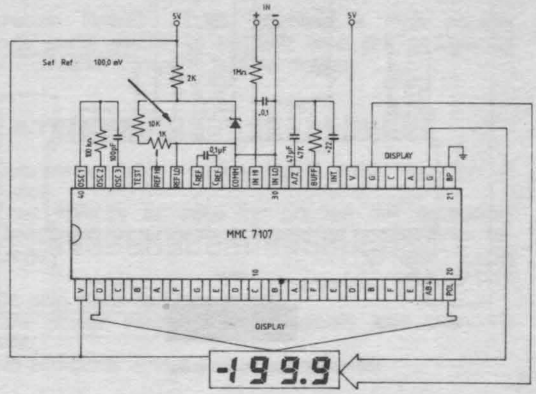


Figure 2: 7107

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the MMC 7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A—Z), (2) signal integrate (INT) and (3) deintegrate (DE).

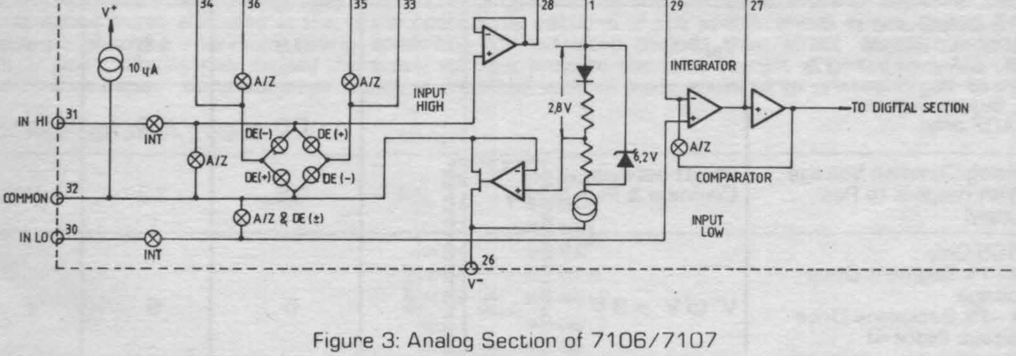


Figure 3: Analog Section of 7106/7107

1. AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the autozero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A—Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10 μV.

2. SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. DE-INTEGRATE PHASE

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal.

Specifically the digital reading displayed is $1000 \left(\frac{V_{IN}}{REF} \right)$.

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. However. since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

DIFFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a rollover error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Values Selection below).

ANALOG COMMON

This pin is included primarily to set the common mode voltage for battery operation (MMC 7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (> 7 V), the COMMON voltage will have a low voltage coefficient and low output impedance.
The limitations of the on-chip reference should also be recognized, however. With the MMC 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC) internal chip dissipation, and package thermal resistance can increase noise near full scale. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All the problems are of course eliminated if an external reference is used.

The MMC 7106, with its negligible dissipation, suffer from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog Common should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

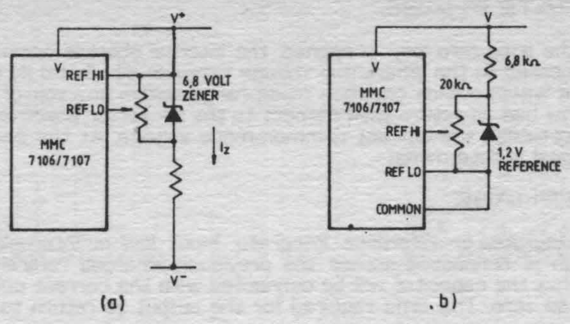


Fig. 4 : Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the MMC 7106 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.
The second function is a „lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10 mA under these conditions.

Caution: on the MMC 7106, in the lamp test mode, the segments have a constant d-c voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

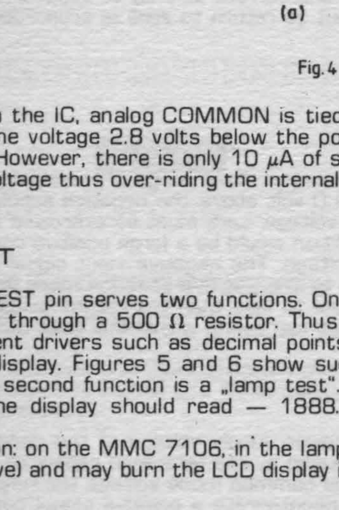


Figure 5: Simple Inverter for Fixed Decimal Point

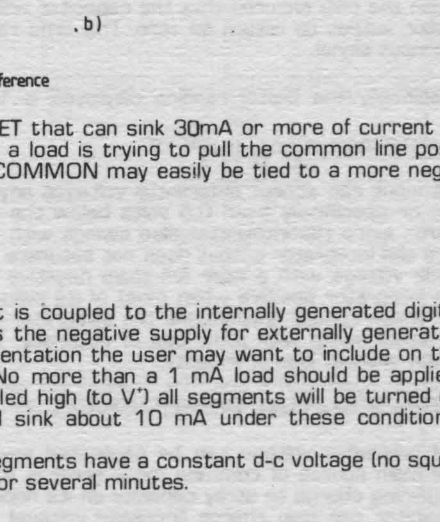


Figure 6: Exclusive 'OR'Gate for Decimal Point Drive

DIGITAL SECTION

Figures 7 and 8 show the digital section for the MMC 7106 and MMC 7107, respectively. In the MMC 7106, an internal digital ground ia generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible d-c voltage exists across the segments.

Figure 8 is the Digital Section of the MMC 7107. It is identical to the MMC 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA.

In both devices, the polarity indication is „on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

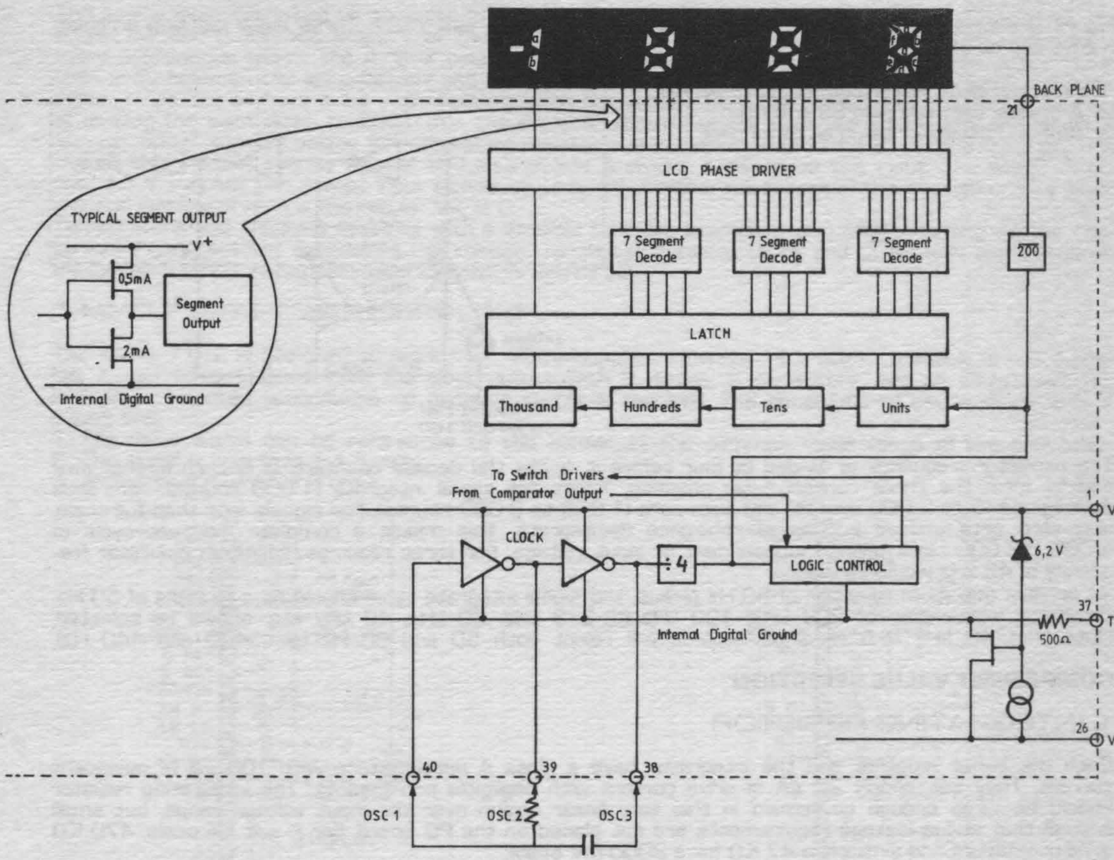


Figure 7: Digital Section 7106

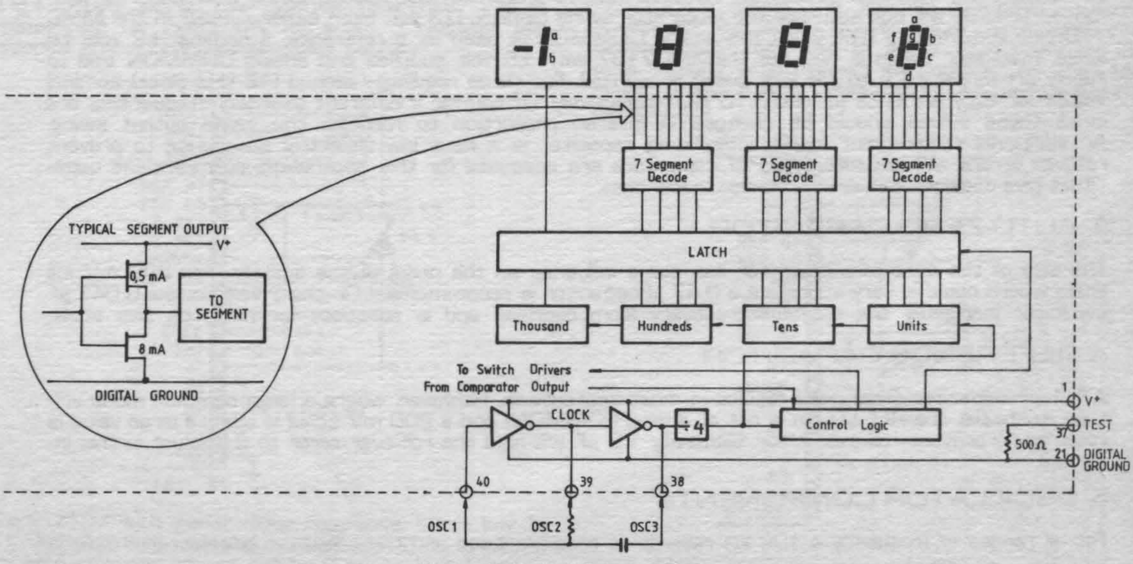
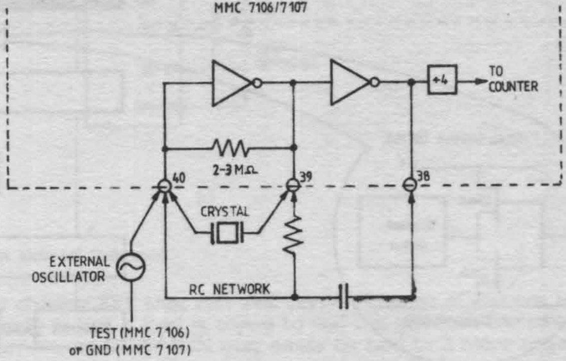


Figure 8: Digital Section 7107

SYSTEM TIMING

Figure 9 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R—C oscillator using all three pins.



The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phasess. These are signal integrate (1 000 counts), reference deintegrate (0 to 2 000 counts) and auto-zero (1 000 to 3 000 counts). For signals less than full scale, auto-zero gets unused portion of reference deintegrate. This makes a complete measure cycle of 4 000 (16 000 clock pulses) independent of input voltage. For three readings/secod an oscillator frequency of 48 kHz would be used.
To achieve maximum rejection of 50 Hz pickup, the signal integrate cycle should be a multiple of 50 Hz. Oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz etc. should be selected. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. INTEGRATING RESISTOR

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470 KΩ is near optimum and similarly a 47 KΩ for a 2000 mV scale.

2. INTEGRATING CAPACITOR

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the MMC 7106 or the MMC 7107, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the MMC7107 with ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μF and 0.10 μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to mentain the same output swing. An additional requirement of the integrating capacitor is it have low dielectric absorbtion to prevent rollover errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. AUTO-ZERO CAPACITOR

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale a 0.047 μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. REFERENCE CAPACITOR

A 0.1 μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200 mV scale is used, a large value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

5. OSCILLATOR COMPONENTS

For all ranges of frequency a 100 kΩ resistor is recommanded and the capacitor is selected from the equation $f = \frac{.45}{RC}$. For 48 kHz clock (3 readings/second), C = 100 pF.

6. REFERENCE VOLTAGE

The analog input reequired to generate full-scale output (2 000 counts) is: $V_{IN} = 2\ V_{REF}$. Thus, for the 2.000 mV and 2 000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682 V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = .341 V. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The MMC 7107 with ±5 V supplies can accept input signals up to ± 4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$.
Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. MMC 7107 POWER SUPPLIES

The MMC 7107 is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. In fact, in selected applications no negative supply is required. The conditions to use a single + 5 V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ± 1.5 volts.
3. An external reference is used.

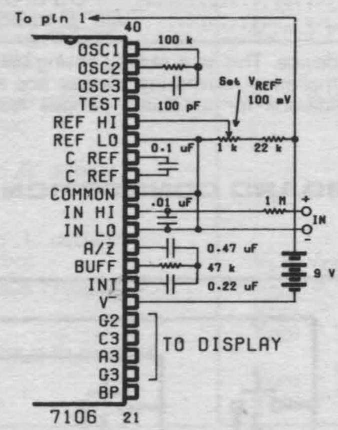


Fig.1 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage(9V battery)

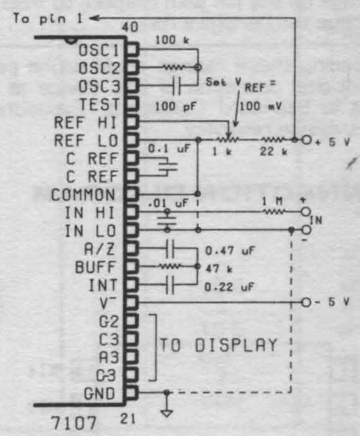


Fig.2 7107 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. INLO may tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

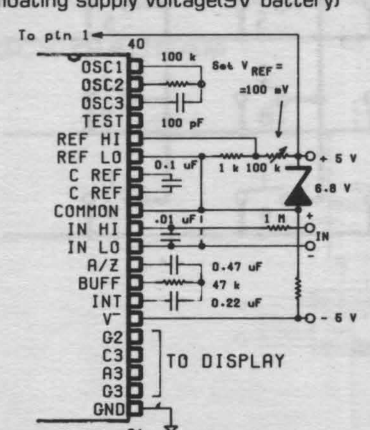


Fig.3 7107 with Zener diode reference. Since low T. C. Zeners have breakdown voltage 6.8 V, diode must be placeed across the total supply (10V). IN LO may be tied to either COMMON or GND

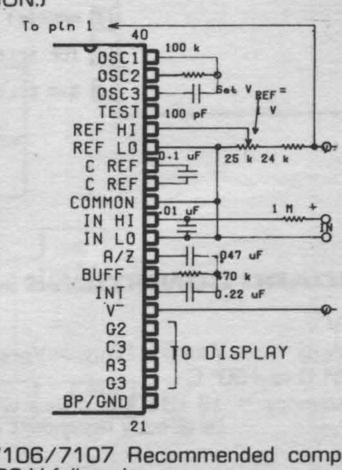


Fig.4 7106/7107 Recommended component values for 2.000 V full scale

PUSH BUTTON TELEPHON DIALLER

GENERAL DESCRIPTION

The MMC 9151 Pushbutton Dialler performs the function of converting input data from a keyboard into a series of pulses suitable for loop disconect dialing. It can be operated directly by the telephone line current and it has a redial capability. It has the facility of B:M and IDP pin selection. The use of CMOS technology results in low voltage and current requirements enabling easy interfacing with a variety of telephones.

FEATURES

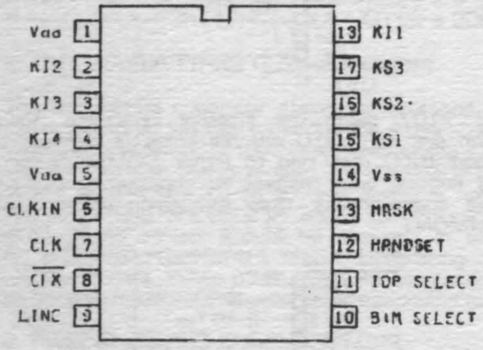
- 2.5 to 5 V and 200 mA plus standby mode
- frequency of on- chip clock set by external RC network
- selectable break: make ratio and interdigital pause
- uses 3 x 4 matrix keyboard with no keyboard ground or common contact
- keyboard inputs have antibounce protection
- input pull-up or pull-down resistor on-chip
- redial controlled from keyboard
- 22 digit capacity
- dialler reset for line power breaks > 200 ms

ABSOLUTE MAXIMUM RATINGS

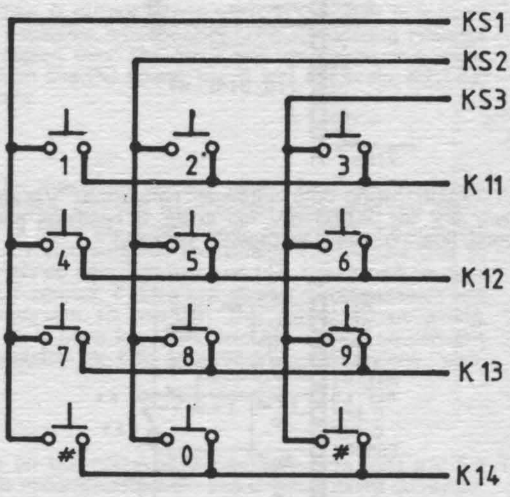
Voltage on any pin with respect to VSS	−0.3 to 5.5 V
Storage temperature range	−65° C to 85° C

- exceding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



KEYBOARD CONNECTION



STANDARD CONDITIONS (unless otherwise noted)

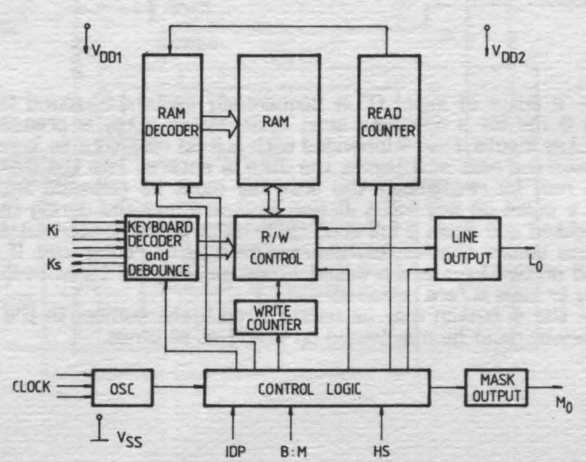
$V_{SS} = 0$ V
$V_{DD1} = V_{DD2} = 2.5$ V to 5 V ($V_{DD1} > V_{DD2}$)
$T_A = -25°$ C to $+50°$ C
Clock frequency = 18 kHz. The device will function correctly from 8 kHz to 50 kHz but all timings will be directly dependent on the clock period

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
INPUTS					
V_{IL} logic „0" level		−0.3	—	0.2	V
V_{IH} logic „1" level		V_{DD2}—0.2	—	V_{DD2}+0.3	V
current source to V_{DD2} (keyboard inputs)	note 1	2	—	60	/μA
current sink to V_{SS} (keyboard inputs, IDP, BIM)		3	—	90	/μA
clock in leakage current	$t_A = 25°$ C, $V_{in} = V_{SS}$ or V_{DD1}	—	—	20	nA
key depression period		10	—	—	ms
OUTPUTS					
LINE					
I_{OL} logic „0" output current	$V_o = 1$ V	2	—	—	mA
I_{OFF} leakage current	$V_o = 5$ V	—	—	1	/μA
MASK					
I_{OL} logic „0" output current	$V_o = 1$ V	2	—	—	mA
I_{OH} logic „1" output current	$V_o = V_{DD2}$—1 V	2	—	—	mA
CLOCK FREQUENCY	$V_{DD1} = V_{DD2} = 3.75$ V	17.2	—	18.6	kHz
	$V_{DD1} = V_{DD2} = 2.5$ V	14.3	—	—	kHz
	$V_{DD1} = V_{DD2} = 5$ V	—	—	19.5	kHz
SUPPLY CURRENT					
I_{DD1}	$V_{DD1} = 5$ V $V_{DD2} = 0$V	—	—	7	/uA
I_{DD2}	$V_{DD2} = 5$ V note 2	—	—	200	/μA

note 1: the device will function correctly with a maximum logic „0" of 1 V and a minimum logic „1" of V_{DD}—1 V. However use under these conditions may result in an increased supply current.
note 2: measured with B:M, IDP inputs at V_{SS} and with no keys depressed.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

V_{SS} — the negative supply of the device. All voltages are referenced to this pin.

V_{DD2} — the positive supply to the digit store and write counter. Power must be maintained on this pin if the redial function is used.

V_{DD1} — the positive supply to the clock generator and control logic. VDD2 should rise to 2.5 V within 20 ms of switch on.

CLOCK IN, CLOCK, $\overline{\text{CLOCK}}$ — these pins are conected to an external RC network whick controls the frequency of the clock generator and hence the timing of the line and mask outputs.

HANDSET INPUT — the state of the handset input is used to control this input, a logic „1" on the input indicating that the handset is on hook and a logic „0" indicating that the handset is off hook. This input is used to reset the control logic depending on the past history of the input. If the input is taken from logic „1" to logic „0" and the clock is not oscillating, a reset pulse is produced when clock pulses are detected. The device is then ready for operation. If the input is taken to logic „1" for less than 200 ms and the clock generator is operating throughout this period, a reset pulse is not produced when the input is taken back to logic „0". Thus short breaks in line power will not affect the operation of the circuit.
If the input is taken to logic „1" for more than 200 ms and clock pulses are present throughout this period a reset pulse will be generated at the end of the 200 ms period.

LINE OUTPUT — the loop disconect dial pulses appear at this output. It is an open drain output with the source of the output transistor being conected to V_{SS}. A break period corresponds to this transistor being switched on and a make period or $\overline{\text{IDP}}$ corresponds to the transistor being switched off.
The first digit of any outdialing sequence is preceded by a pre digit pause equal in length to an interdigital pause.

MASK OUTPUT — this is a push pull output and is used to mute the telephone speech circuit. A logic „1" indicates that the speech circuit is to be muted, this occurring immediately on recognition of an input from the keypad.

IDP INPUT — this pin is used to select the duration of the interdigital pause. With a clock frequency of 18 kHz interdigital pauses of 700, 800 ms may be selected.

IDP	Voltage on pin
700 ms	V_{DD2}
800 ms	V_{SS}
500 ms	clock

BREAK: MAKE RATIO — a choice of four break: make ratio is available as a pin programmable option 70 : 30, 66.6 : 33.3, 60 : 40 and 50 : 50.

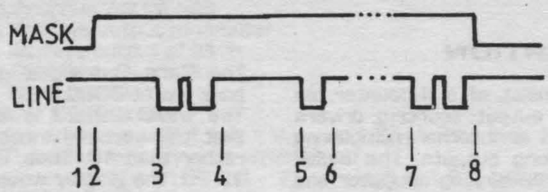
Break: Make Ratio

ratio	voltage on pin
70 : 30	clock
66.6 : 33.3	V_{DD}
60 : 40	V_{SS}
50 : 50	clock

KEYBOARD INPUTS — a pulse of logic „0" is sequentially switched around the three keyboard scan outputs, taking 5 ms for a complete scan cycle. When a key is pressed the pulse appears on one of the four key inputs 1 — 4 (provided with pull-up resistors to logic „1") and if it occurs on the same input on the next scan cycle, the data is entered into the digit store. Before a second key depression may be recognized, the first key must be released and a full scan cycle completed without a pulse on any input. If two keys are pressed during the same scan cycle, the data will be rejected and again a full scan cycle must be completed without a pulse appearing on any of the inputs before another key depression may be recognized. If a key is pressed during an inhibit period or two keys are pressed simultaneously, all three scan outputs will go to logic „0" until the key or keys is/are released.

REDIAL OPERATION — the # button may be used to redial the number in the digit store. If the redial mode is used, power must be maintained on VDD1 at all times.

LINE AND MASK OUTPUT TIMING



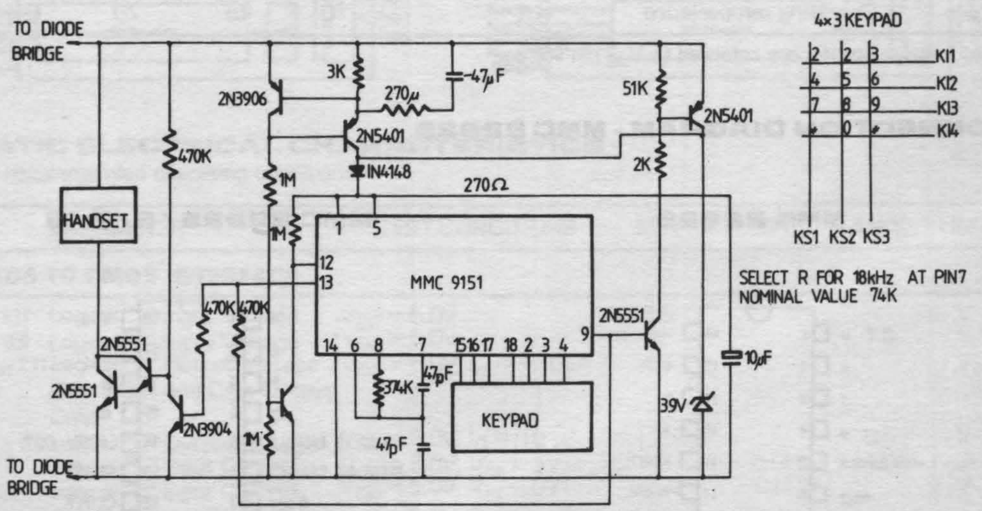
The above sequence of events is that wich occur when the digit store is initially empty. The time intervals quoted in the folowing explanation aree valid only for a clock frequency of 18 kHz. The time intervals are inversely proportional to the clock frequency.

Event	Time interval
1 The first key is depressed and the anti bounce timer is started.	T_{1-2} = 5—10 ms after end of bounce
2 The data from the keyboard is accepted. The mask output appears and the pre digital pause commences. This is the same duration as the interdigital pause and is pin selectable.	T_{2-3} = 700, 800 or 500 ms
3 Dialling of the first digit starts. The example shown is a digit 2.	T_{3-4} = n x 100 ms where n = digit dialed
4 End of 1 st digit and start of inter digital pause.	T_{4-5} = 700, 800 or 500 ms.
5 Dialling of 2nd digit starts. The example shown is digit 1.	T_{5-6} = n x 100 ms where n = digit dialed
6 End of second digit and start of inter digital pause	T_{6-7} = 700, 800 or 500 ms

Dialling of further digits continues in a similar manner until the last digit.

7 Dialling of last digit commences, in this case a digit 2.	T_{7-8} = n x 100 ms where n = digit dialed
8 End of last digit and end of mask signal.	

TYPICAL APPLICATION



4-DIGIT COUNTERS WITH MULTIPLEXED 7-SEGMENT OUTPUT DRIVERS

GENERAL DESCRIPTION

Theese CMOS counters consist of a 4-counter, an internal output latch, NPN output sourcing drivers for a 7-segment display and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.
The MMC 22925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs (16 pins package).
The MMC 22926 is like the MMC 22925 except that it has a Display Select and a Carry-Out used for cascading counters.
The Carry-Out signal goes high at 6000 and goes back low at 0000.
The MMC 22927 is like the MMC 22926 except that the secound most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59:9).
The MMC 22928 is like the MMC 22926 except that the most significant digit divides by 2 rather than 10 and the Carry Out is an overflow indicator which goes high at 2000, and goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

FEATURES

- Supply voltage range 3 V to 6 V
- Internal multiplexing circuitry
- High segment sourcing current: 40 mA at $V_{OUT} = V_{DD} - 1.6$ V, $V_{DD} = 5$ V
- Guaranteed noise margin 1 V

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	−0.3	to	6.5	V
V_i	Input voltage	−0.3	to	V_{DD}+0.3	V
I_i	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation	Refer	to $P_{D(MAX)}$	vs T_A	Graph
T_A	Operating temperature	0	to	70	C
Tstg	Storae temperature	−40	to	125	C

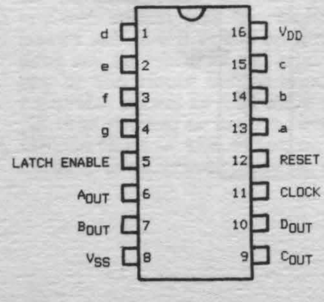
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage	3	to	6	V
V_i	Input voltage	0	to	V_{DD}	V
T_A	Operating temperature	0	to	70	C

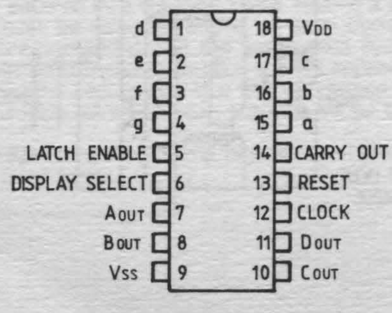
* All voltage voluies are referred to V_{SS} pin voltage

CONNECTION DIAGRAM - MMC 22925

MMC 22925



MMC 22925/6/7/8

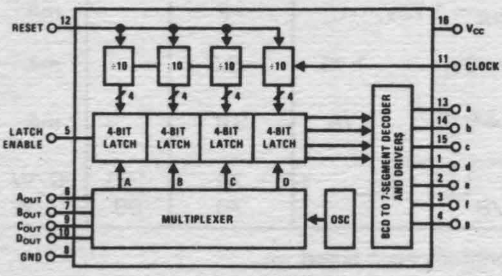


FUNCTIONAL DESCRIPTION

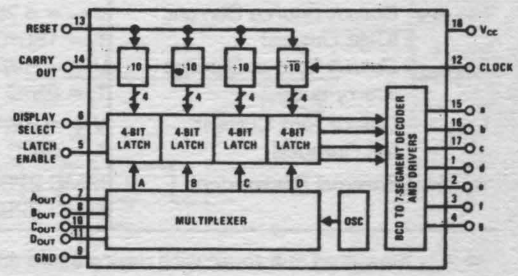
Reset	— Asynchronous, active high
Display Select	— High, displays output of counter
	— Low, displays output of latch
Latch Enable	— High, flow through condition
	— Low, latch condition
Clock	— Negative edge sensitive
Digit Output	— Current sourcing with 1 mA $V_{OUT} = 1.75$ V. Also sink capability = 2 LTTL loads
Carry-out	— 2 LTTL loads (see caryy-out waveforms)
Segment Output	— Current sourcing with 80 mA $V_{OUT} = V_{DD} - 1.6$ V typical (T_j = = 25 C). Also sink capability = 2 LTTL loads.

BLOCK DIAGRAM

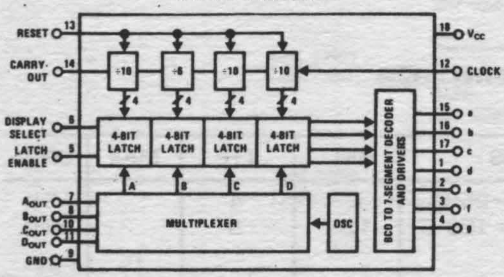
MMC 22925



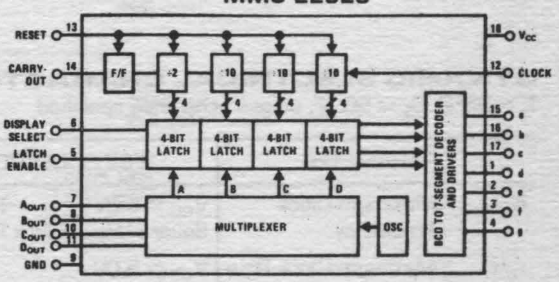
MMC 22926



MMC 22927



MMC 22928



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS TO CMOS INTERFACE						
V_{IN} (1)	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
V_{IN} (0)	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
V_{OUT} (1)	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	$V_{CC} = 5.0V$, $I_O = -10\mu A$	4.5			V
V_{OUT} (0)	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = 10\ \mu A$			0.5	V
I_{IN} (1)	Logical "1" Input Current	$V_{CC} = 5.0V$, $V_{IN} = 5V$		0.005	1.0	μA
I_{IN} (0)	Logical "0" Input Current	$V_{CC} = 5.0V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 5.0V$, Outputs Open Circuit, $V_{IN} = 0V$ or 5 V		20	1000	μA

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	$I_{OUT} = -65mA$, $V_{CC} = 5V$, $T_j = 25°C$		$V_{CC}-1.3$		V
		$I_{OUT} = -40mA$, $V_{CC} = 5V$ $T_j=100°C$	$V_{CC}-1.6$	$V_{CC}-1.2$		V
		$T_j=150°C$	$V_{CC}-2$	$V_{CC}-1.4$		V
R_{ON}	Output Resistance (Segment Sourcing Output)	$I_{OUT} = -65mA$, $V_{CC} = 5V$, $T_j = 25°C$		20		Ω
		$I_{OUT} = -40mA$, $V_{CC} = 5V$ $T_j=100°C$		30	40	Ω
		$T_j=150°C$		35	50	Ω
	Output Resistance (Segment Output) Temperature Coeficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	$V_{CC} = 4.75V$, $V_{OUT} = 1.75V$, $T_j = 150°C$	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-out)	$V_{CC} = 5V$, $V_{OUT} = 0V$, $T_j = 25°C$	−1.75	−3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$, $T_j = 25°C$	1.75	3.6		mA
ϕ_{JA}✲	Thermal Resistance	MMC 22925		75	100	°C/W
		MMC 22926/7/8		70	90	°C/W

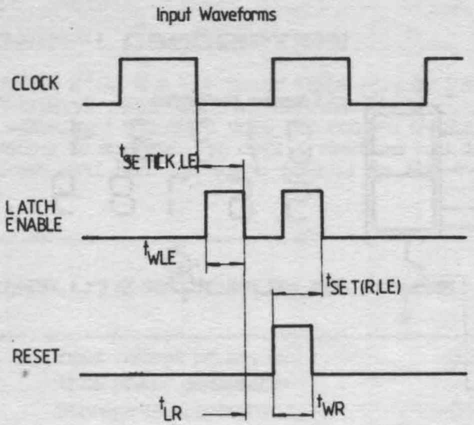
✲ ϕ_{JA} measured in free-air with device soldered into printed circuit board

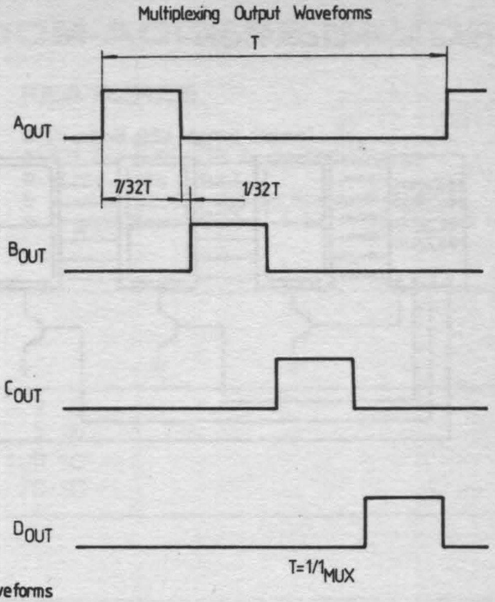
DYNAMIC ELECTRICAL CHARACTERISTICS

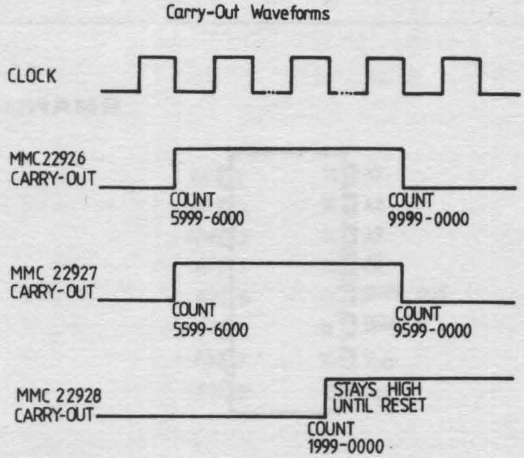
$T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_r	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$				15	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	10		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK,LE)}$	Clock Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset Wait Time	$V_{CC} = 5.0V$	$T_j = 25°C$	0	−100		ns
			$T_j = 100°C$	0	−100		ns
$t_{SET(R,LE)}$	Reset to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	$V_{CC} = 5.0V$			1000		Hz
C_{IN}	Input Capacitance	Any Input			5		pF

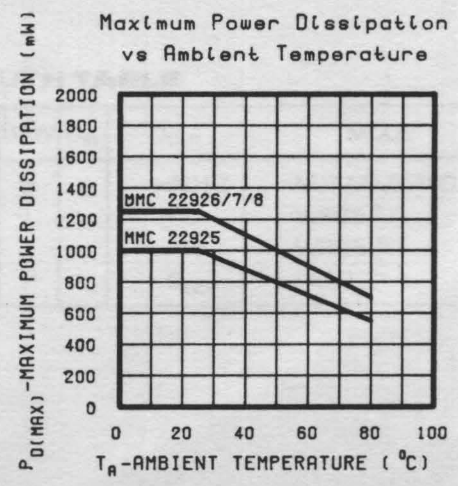
TIMING DIAGRAM



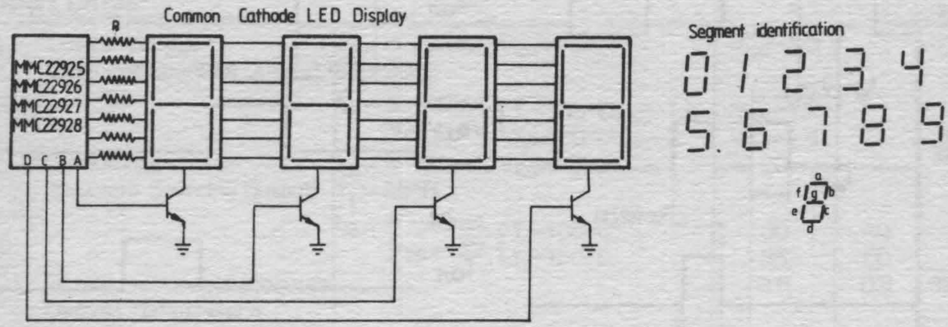




TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATION



1024 BIT STATIC RANDOM-ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 2102 is a high speed 1024 word by 1 static N-channel silicon-gate MOS RAM. The device is fully static and therefore does not require clocks or refreshing to operate. The data is read out non destructively and has the same polarity as the input data.

FEATURES

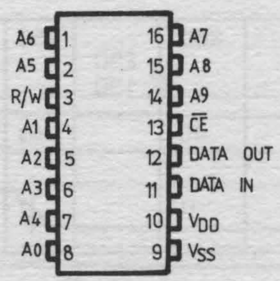
- Power suplly $V_{CC} = 5V$
- TTL compatible all inputs and outputs
- Three-state output
- Input protected against static charge
- Organization 1024 × 1 bit in 16 pin std. package

ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (at any pin)	-0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-33 to 125	°C
T_{op}	Operating temperature under bias	0 to 70	°C

All voltages are referred to GND pin voltage

CONNECTION DIAGRAMS



TRUTH TABLE

CE	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

5

STATIC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, T_A = 0 to 70°C unless otherwise specified)

PARAMETER		TEST CONDITIONS	MMN 2102 MMN 2102-4			MMN 2102-2			MMN 2102-6			UNIT
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
V_{IH}	Input high voltage		2		V_{CC}	2		V_{CC}	2.2		V_{CC}	V
V_{IL}	Input low voltage		-0.5		0.8	-0.5		0.8	-0.5		0.65	V
V_{OH}	Output high voltage	$I_{OH} = -100\mu A$	2.4			2.4			2.2			V
V_{OL}	Output low voltage	$I_{OL} = 2.1$ mA			0.4			0.4			0.45	V
I_{LI}	Input load current	V_I = 0Vto 5.25 V		1	10		1	10		1	10	µA
I_{OH}	Output leakage current	$\overline{CE}$ = 2V, $V_O = V_{OH}$		1	5		1	5		1	5	µA
I_{OL}	Output leakage current	$\overline{CE}$ = 2V, V_O = 0.4 V		-1	-10		-1	-10		-1	-10	µA
I_{CC}	Supply current	V_I = 5.25V, T_A = 0°C D_{OUT} open		33	55		45	65		33	55	mA

Note: typical values for T_A = 25°C and nominal supply voltage

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5 V unless otherwise specified)

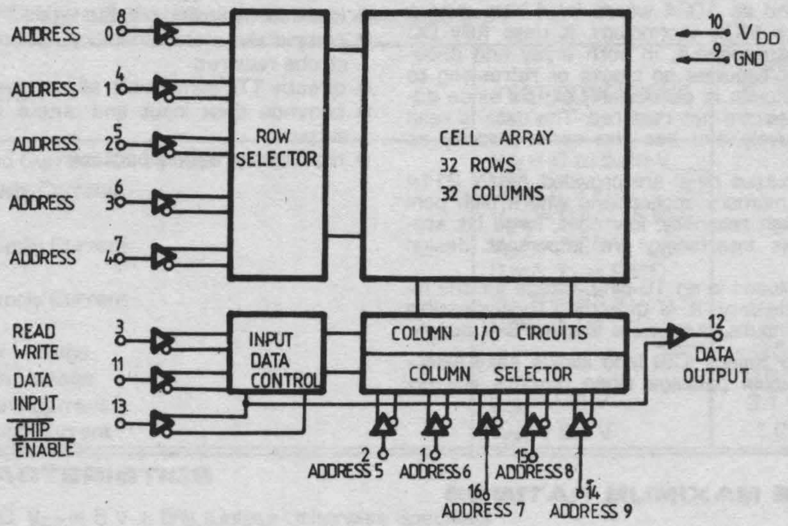
PARAMETER		TEST CONDITIONS	MMN 2102-2		MMN 2102		MMN 2102-4		MMN 2102-6		UNIT
			min.	max.	min.	max.	min.	max.	min.	max.	
	Read Cycle										
t_{rc}	Read cycle		250		350		450		650		ns
t_a	Access time			250		350		450		650	ns
t_E	CE to output time			130		180		230		400	ns
t_{OH1}	Previous read data valid with respect to address	$t_R t_F$ = 10 ns Load = 1 TTL gate and	40		40		40		50		ns
t_{H2}	Previous read data valid with respect to chip enable	C_L = 100 pF	0		0		0		0		ns
	Write Cycle										
t_{WC}	Write cycle		250		350		450		650		ns
t_{AW}	Address to with setup time	$t_R t_F$ = 10 ns	20		20		20		200		ns
t_{WP}	Write pulse width	Load = 1 TTL	180		250		300		400		ns
t_{WR}	Write recovery time	gate and	0		0		0		50		ns
t_s	Data setup time	C_L = 100 pF	180		250		300		450		ns
t_{CW}	Chip enable to write Set up time		180		250		300		550		ns

CAPACITANCE

(T_A = 25°C, f = 1 Mhz)

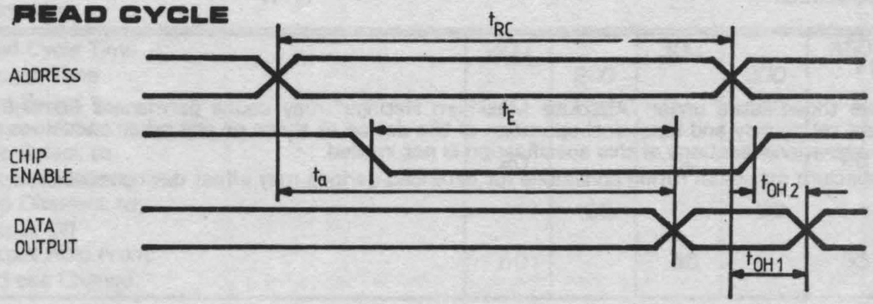
PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
C_I	Input capacitance	V_I = 0 V		3	5	pF
C_O	Output capacitance	V_O = 0 V		7	10	pF

BLOCK DIAGRAM

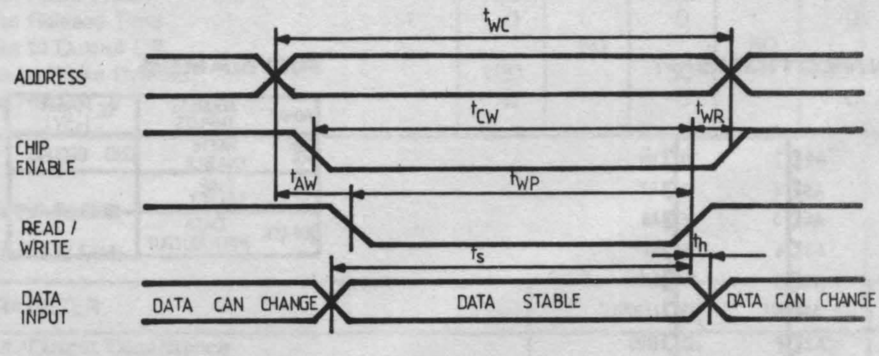


WAVEFORMS

READ CYCLE



WRITE CYCLE



1024 × 4 BIT STATIC RAM

GENERAL DESCRIPTION

MMN 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using a high performance MOS technology. It uses fully DC static circuitry throughout, in both array and decoding; therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data.
Common input/output pins are provided. MMN 2114 is designed for memory applications where high performance and high reliability, low cost, large bit storage, and simple interfacing are important design objectives.
MMN 2114 is placed in an 18-pin package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, a single +5 V supply.

A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

FEATURES

- single +5 V supply
- identical cycle and access times
- completely static memory — no clock or timing strobe required
- directly TTL compatible: all inputs and outputs
- common data input and output using three-state outputs
- high density 18 pin package

ABSOLUTE MAXIMUM RATINGS

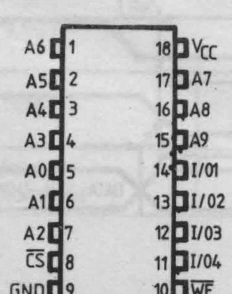
T_A	Temperature under bias	-10°C to 80°C
T_{stg}	Storage Temperature	−65°C to 150°C
V_i	Voltage on any Pin with Respect to ground	−0.5 V to +7 V
P_{tot}	Power dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affeet device reliability.

PIN CONNECTIONS



PIN NAMES

A0–A9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/01–I/04	DATA INPUT/OUTPUT		

D.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$ (Unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MMN 2114-2, 2114-3, 2114 min.	MMN 2114-2, 2114-3, 2114 max.	UNIT
I_{LI}	Input Load Current (All input pins)	$V_{IN} = 0$ to $5.25\ V$		10	μA
$\|I_{LO}\|$	I/O Leakage Current	$\overline{CS} = 2.4\ V$, $V_{I/o} = 0.4\ V$ to V_{CC}		10	μA
I_{CC1}	Power Supply Current	$V_{CC} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 25°C$		95	mA
I_{CC2}	Power Supply Current	$V_{CC} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 0°C$		100	mA
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
I_{OL}	Output Low current	$V_{OL} = 0.4\ V$	2.1	6.0	mA
I_{OH}	Output High current	$V_{OH} = 2.4\ V$	−1.0	−1.4	mA

A.C. CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 5\%$ (Unless Otherwise Specified)

	PARAMETER	2114-2 min.	2114-2 max.	2114-3 min.	2114-3 max.	2114 min.	2114 max.	UNIT
Read cycle								
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Select to Output Valid		70		100		120	ns
t_{CX}	Chip Select to Output Enabled	20		20		20		ns
t_{OTD}	Chip Deselect to Output Off		60		80		100	ns
t_{OHA}	Output Hold From Address Change	50		50		50		ns
Write cycle								
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Pulse Width	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Write to Output Off		60		80		100	ns
t_{DW}	Data to Write Overlap	120		150		200		ns
t_{DH}	Data Hold	0		0		0		ns

CAPACITANCE

$T_A = 25°C$, $f = 1.0\ MHz$

	PARAMETER	typ	max	UNIT
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note:This parameter is periodically sampled and not 100% tested.

A.C. TEST CONDITIONS

Input Pulse Levels		0.8 V to 2V
Input Rise and Fall Time		10 ns
Timing Measurement Levels:	Input	1.5 V
	Output	0.8 V and 2V
Output Load		1 TTL Gate and 100 pF

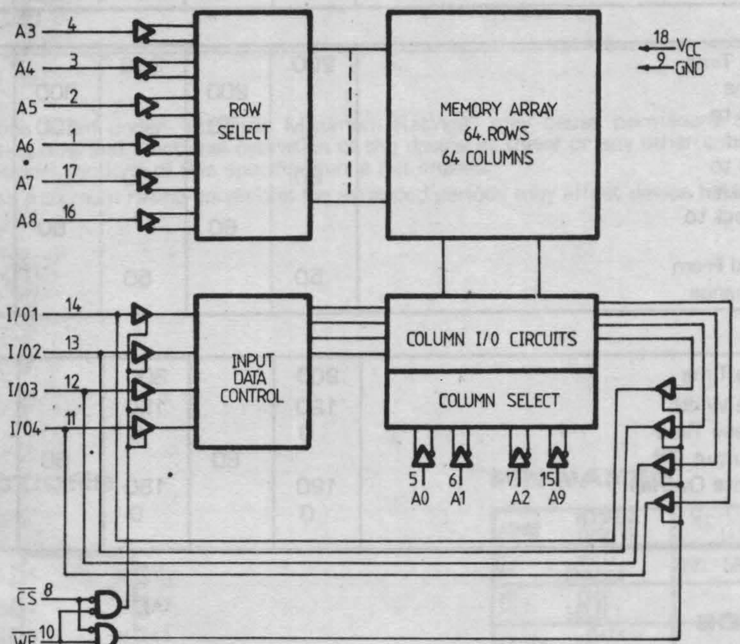
DATE STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be afected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as CS is high. Either CS or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

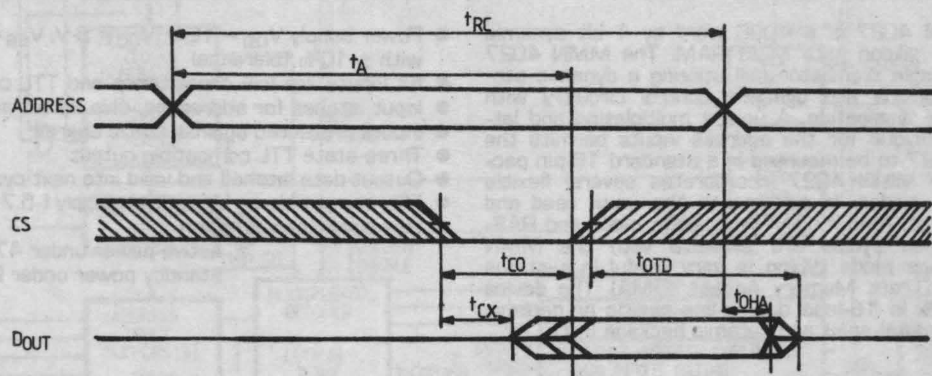
Data within the array can only be changed during Write time-defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.
Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

BLOCK DIAGRAM

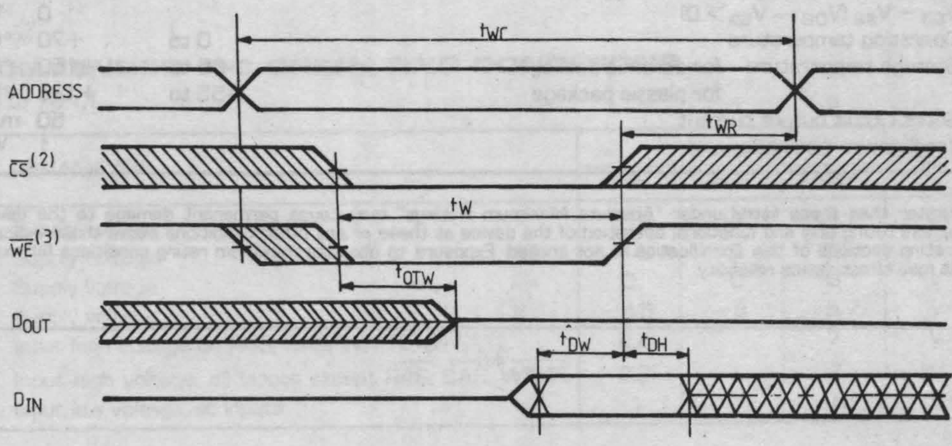


WAVEFORMS

Read cycle (1)



Write cycle



Notes:
1. $\overline{WE}$ is high for a Read cycle.
2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state
3. $\overline{WE}$ must be high during all address transitions

4096 - BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 4027 is a 4096 word by 1 bit dynamic N-channel silicon gate MOS RAM. The MMN 4027 uses a single transistor cell utilizing a dynamic storage technique and dynamic control circuitry with low power dissipation. A unique multiplexing and latching technique for the address inputs permits the MMN 4027 to be mounted in a standard 16-pin package. The MMN 4027 incorporates several flexible operating modes. In addition to the usual read and write cycles, read modify write, page mode and RAS-only refresh cycles are available with the MMN 4027. Page mode timing is very useful in systems requiring Direct Memory Access (DMA). The device is available in 16-lead dual in-line plastic or ceramic package (metal-seal), and ceramic package (frit-seal).

FEATURES

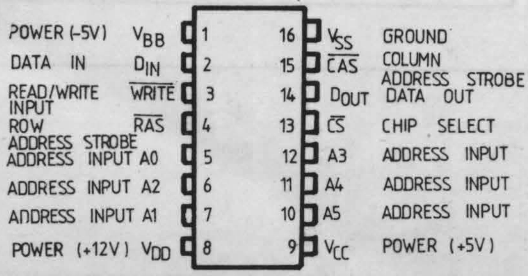
- Power supply V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = -5 V (all with ± 10% tolerance)
- All inputs are low capacitance and TTL compatible
- Input latches for addresses, chip select and data in
- Inputs protected against static charge
- Three-state TTL compatible output
- Output data latched and valid into next cycle
- ECL compatible on V_{BB} power supply (-5.7 V.)
- Low power consumption :
  active power under 470 mW
  standby power under 27 mW

ABSOLUTE MAXIMUM RATINGS*

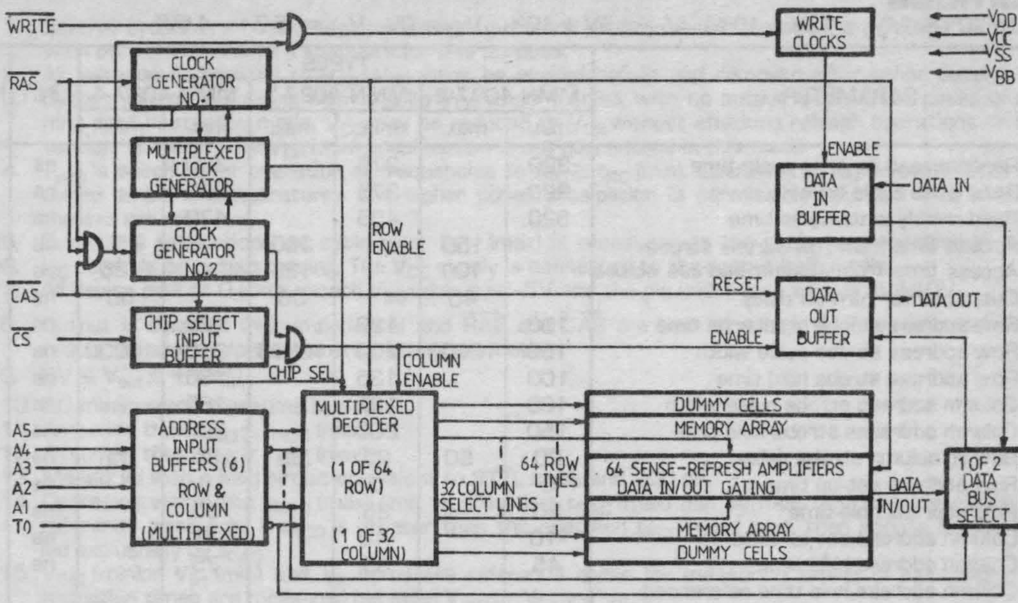
	Voltage on any pin relative to V_{BB}		-0.5 to	+20	V
	Voltage on V_{DD}, V_{CC} relative to V_{SS}		-1 to	+15	V
	$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0$)			0	V
T_A	Operating temperature		0 to	+70	°C
T_{stg}	Storage temperature	for ceramic package	-65 to	+150	°C
		for plastic package	-55 to	+125	°C
I_o	Short circuit output current			50	mA
P_{tot}	Total power dissipation			1	W

* Stresses grater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification in not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70°C)

	PARAMETER	VALUES			UNIT	NOTES
		min	typ	max		
V_{DD}	Supply voltage	10.8	12	13.2	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2,3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	−4.5	−5	−5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V	2
V_{IH}	Input high voltage, all inputs except RAS, CAS, WRITE	2.2		7	V	2
V_{IL}	Input low voltage, all inputs	−1		0.8	V	2

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C) (V_{DD} = 12V ± 10%) (V_{CC} = 5V ± 10%, V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

	PARAMETER	VALUES			UNIT	NOTES
		min.	typ.	max.		
I_{DD1}	Average V_{DD} power supply current			35	mA	5
I_{DD2}	Standby V_{DD} power supply current			2	mA	8
I_{DD3}	Average V_{DD} power supply current during „$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} power supply current				mA	6
I_{BB}	Average V_{BB} power supply current			150	μA	
$I_{I(L)}$	Input leakage current (any input)			10	μA	7
$I_{O(L)}$	Output leakage current			10	μA	8,9
V_{OH}	Output high voltage (I_{SOURCE} = -5mA)	2.4			V	
V_{OL}	Output low voltage (I_{SINK} = 3.2 mA			0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

($T_A = 0$ to 70°C) ($V_{DD} = 12V \pm 10\%$) ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5.7$ to $-4.5V$)

	PARAMETER	MMN 4027-2 min.	MMN 4027-2 max.	MMN 4027-3 min.	MMN 4027-3 max.	MMN 4027-4 min.	MMN 4027-4 max.	UNIT	NOTE
t_{RC}	Random read or write cycle time	320		375		380		ns	
t_{RWC}	Read write cycle time	320		375		395		ns	
t_{RMW}	Read modify write cycle time	320		405		470		ns	
t_{RAC}	Access time from row adress strobe		150		200		250	ns	11-13
t_{CAC}	Access time from column address strobe		100		135		165	ns	12-13
t_{OFF}	Output buffer turn-off delay		40		50		60	ns	
t_{RP}	Row address strobe precharge time	100		120		120		ns	
t_{RAS}	Row address strobe pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	Row address strobe hold time	100		135		165		ns	
t_{CAS}	Column address strobe pulse width	100		135		165		ns	
t_{CSH}	Column addreess strobe hold time	150		200		250		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	35	85	ns	14
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	-10		-10		-10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CSC}	Chip select set-up time	-10		-10		-10		ns	
t_{CH}	Chip select hold time	45		55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition time (rise and fall)	3	35	5	50	5	50	ns	15
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to row strobe lead time	50		70		85		ns	
t_{CWL}	Write command to column strobe lead time	50		70		85		ns	
t_{DS}	Data in set-up time	0		0		0		ns	16
t_{DH}	Data in hold-time	45		55		75		ns	16
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		80		110		ns	
t_{RFSH}	Refresh period		2		2		2	ns	
t_{WCS}	$\overline{Write}$ $\overline{command}$ set-up time	0		0		0		ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	17
t_{DOH}	Data out hold time	10		10		10		ns	

CAPACITANCES

($T_A = 0$ to 70°C, $V_{DD} = 12V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5.7$ to $-4.5V$)

	PARAMETER	typ.	max.	UNIT	NOTES
C_{I1}	Input capacitance (A_0-A_5, D_{IN}, $\overline{CS}$)	4	5	pF	18
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	18
C_O	Output capacitance (D_{OUT})	5	7	pF	8-18

NOTES

1. Several cycles are requiered after power-up before proper device operation is achieved. Any 8 cycles wich perform refresh are adequate for this purpose.
2. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. T_{amb} is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).
6. I_{CC} depends on output loading. The V_{CC} supply is connected to the output buffer only.
7. All device pins at 0 volts except V_{BB} wich is at -5V and the pin under test wich is at +10V.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is requiered prior to measurement of this parameter.
9. $0V \leq V_{out} \leq +10V$.
10. AC measurement assume $t_T = 5ns$.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geq t_{RCD}$ (max)
13. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a referance point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. V_{IHC} (min)or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modifywrite cycles.
17. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min. the cycle is a read-write cycle and Data Out will contain data read from the selected, cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
18. Effective capacitance is calculated from the equation :

$$C = \frac{\Delta Q}{\Delta V} \quad \text{with } \Delta V = 3 \text{ volts.}$$

ADDRESSING

The 12 address bits required to decode one of 4096 cell locations within the M 4027 are multiplexed onto the 6 address inputs and latched into the on-chip row and column address latches.
Row Address Strobe ($\overline{RAS}$) latches the six row address bits conto the chip. Column Address Strobe ($\overline{CAS}$) latches the six column address bits plus Chip Select ($\overline{CS}$) onto the chip.
Since the internal circuitry allows the columns information to be externally applied to the chip before it is actually required, the hold time requirements for column address and $\overline{CS}$ are also referenced to $\overline{RAS}$. However, this gates $\overline{CAS}$ feature allows the systems designer to compensate for timing skews that may be encountered in the multiplexing operation.
Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.
Additional timing margin is gained because column address is not required until $\overline{CAS}$ makes its negative transition.
The timing is further simplified by the positive transition of $\overline{CAS}$ not being referenced to the positive transition of $\overline{RAS}$. In fact, $\overline{CAS}$ need not go HIGH until the beginning of the next cycle.

DATA INPUT/OUTPUT

Data to be written into selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active.
The later of this signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In into the latch. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is activated prior to $\overline{CAS}$, the Data In is strobe by $\overline{CAS}$, and set-up time and hold time are referenced to $\overline{CAS}$, If the Data In input is not available at $\overline{CAS}$ time or the cycle is a read-write or readmodify-write, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is re-

ferenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data in referenced to $\overline{CAS}$) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ comands are not executed and, consequently, data stored in the memory is unaffected. Data is retrieved from the memory in read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

At the beginning of a memory cycle, the state of the Data Out latch and buffer depend on the previous memory cycle.

Changes in the condition of Data Out latch are initiated by $\overline{CAS}$. The negative transition of $\overline{CAS}$ causes the Data Output (D_{OUT}) to unconditionnaly go to its open-circuit state. If will remain open-circuited until after the access D_{OUT} time, the will assume the proper state for the type of cycle performed.

If the cycle is read, read-modify-write, or a delayed write and the chip is selected, then the D_{OUT} latch and buffer will contain the data from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then D_{OUT} will contain the input data.

Once the D_{OUT} goes active, it will remain active until the next negative transition of $\overline{CAS}$.

If the cycle is a $\overline{CAS}$ only cycle (no $\overline{RAS}$ signal), then D_{OUT} will assume the open circuit state.

The same istrue for normal cycles (both $\overline{RAS}$ and $\overline{CAS}$ present-when the chip is unselected D_{OUT} remains in the open-circuit state until the next negative transition of $\overline{CAS}$.

$\overline{RAS}$ only refresh cycles (no $\overline{CAS}$) have no effect on the D_{OUT}.

However, when $\overline{Ras}$ only refresh cycles are continued for extended periods of time, D_{OUT} may eventually go open-circuit.

If the chip unselected, it will not accept a write command and the D_{OUT} will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, interface directly with TTL.

The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements.

The 3-state output buffer is a low impedance to V_{CC} for a logic "1" and a low impedance to V_{SS} for a logic "0".

The output resistance to V_{CC} (logic "1" state) is 420 ohm maximum and 135 ohm tipically.

The output resistance to V_{SS} (logic "0" state) is 125 ohm maximum and 35 ohm tipically.

The separate V_{CC} pin allows the output buffer to be powered from supply voltage of the logic to wich chip is interfaced.

During battery stand-by operation, the V_{CC} pin may be unpowered without effecting the MMN 4027 refresh operation.

This allows all system logic, except $\overline{RAS}$ timing circuitry and refresh address logic, to be turned off during battery stand-by to save power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row address every two millisecond or less.

Any cycle in which a $\overline{RAS}$ signal occurs, accomplished a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input.

A write or read-modify-write cycle also refreshes the selected row, but the chip should be unseleced to prevent writing data into the selected cell.

If, during a refresh cycle, the MMN 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (when $\overline{RAS}$ is the only signal applied to the chip) are contained for extended periods, the output buffer may eventually lose proper data and go open-circuit.

The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MMN 4027 and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle.

Tipically, the power is 170 mW at 1 μsec cycle rate for MMN 4027 with a worse case power of less than 470 mW at 320 μsec cycle time.

To reduce the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips.

The $\overline{CAS}$ must be supplied to all chips (to turn of the unselected output.).

Those chips that did not receive a $\overline{RAS}$, however will not dissipate any power on the $\overline{CAS}$ edges, except for that requiered to turn off the outputs.

If the $\overline{RAS}$ signal is decoded and supplied only the selected chips, then the chip select ($\overline{CS}$) input of all chips can be at a logic 0.

Then chips that receive a $\overline{CAS}$ but no, $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.

For refresh cycles, however, either the $\overline{CS}$ input for all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR" outputs from turning on with opposing force. Note that the MMN 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page mode" feature of the MMN 4027 allows for succesive memory operations at multiple column location of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at logic 0 throughout all succesive memory cycles in which the row address is common.
This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. The time requiered for strobing in a new row address is eliminated thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not ecessary that the chip be selected during the first operation in sequence of page cycles.

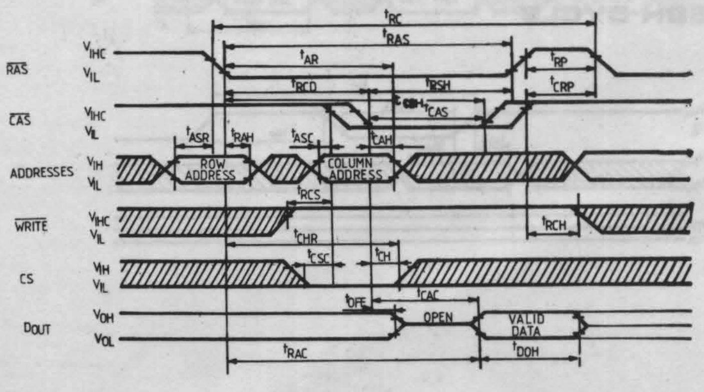
Likewise, the $\overline{CS}$ input can be used to select or disable any cycle (s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column location in a single chip.

The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

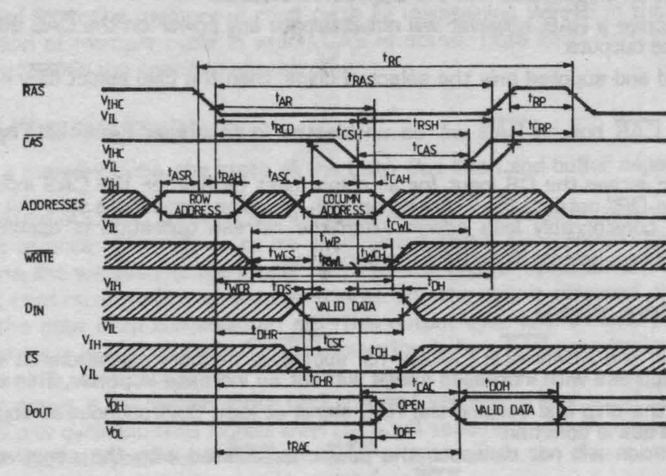
POWER UP

The MMN 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, Microelectronica recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
Under system failure condiction in which one or more supplied exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state. After power is applied to the device, the MMN 4027 requires several cycles before proper device operation is achieved.
Any 8 cycles which perform refresh are adequate for this purpose.

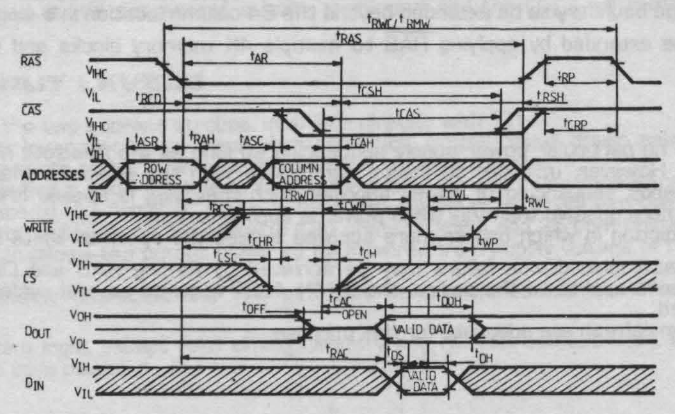
READ CYCLE



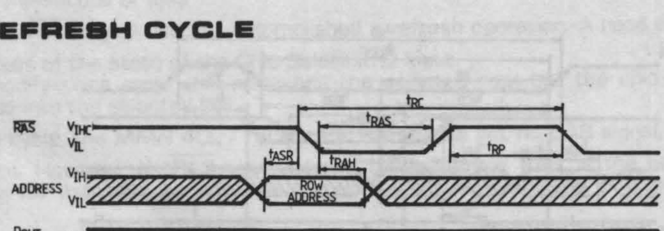
WRITE CYCLE
(early write)



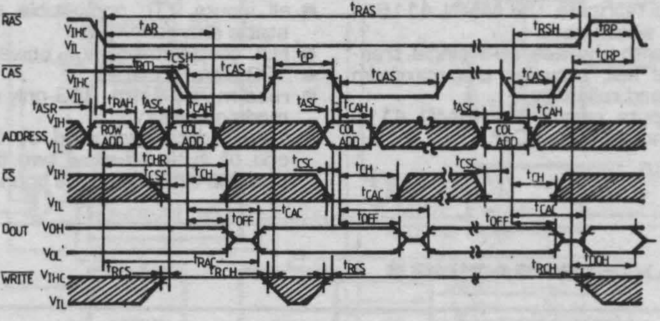
READ WRITE / READ MODIFY-WRITE CYCLE



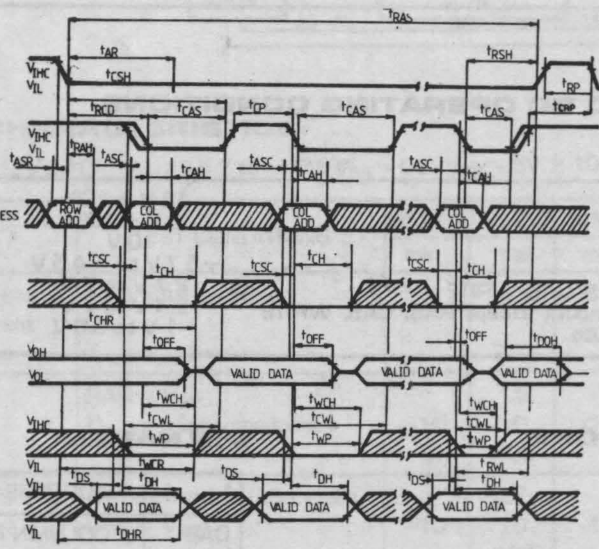
RAS ONLY REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



16384-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 4116 is a MOS dynamic random access memory circuit organized as 16384 words by 1 bit. The technology used to fabricate the MMN 4116 is double-poly N-channel silicon gate.

This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability.

Multiplexed address inputs permit the MMN 4116 to be packaged in a standard 16-pin DIP.

FEATURES

- ±10% tolerance on all power supplies (+12 V, ±5 V)
- low power: 462 mW active, 20 mW standby (max)
- all inputs TTL compatible and protected against static charge.
- ECL compatible on V_{BB} power supply (−5·7 V)
- 128 refresh cycles
- read-modify-write, RAS-only refresh, and page-mode capability
- output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary

ABSOLUTE MAXIMUM RATINGS

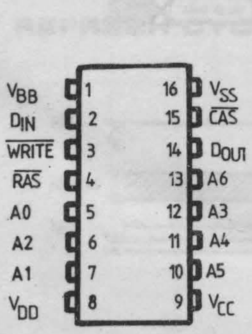
	Voltage on any pin relative to V_{BB}	−0.5 V	to	+20 V
	Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	−1 V	to	+15 V
	$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0$)			0V
T_A	Operating temperature	0°C	to	+70°C
T_{stg}	Storage temperature	−55°C	to	+125°C
I_o	Short circuit output current			50 mA
P_{tot}	Total power dissipation			1 W

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70°C)[1]

V_{DD} supply voltage	12 V ± 10%	Note 2
V_{CC} supply voltage	5 V ± 10%	Note 2,3
V_{SS} supply voltage	0 V	Note 2
V_{BB} supply voltage	−5.7 V to − 4.5 V	Note 2
Input high voltage on RAS, CAS, WRITE	2.7 V to 7 V	Note 2
Input high voltage, all inputs except RAS, CAS, WRITE	2.4 V to 7 V	Note 2
Input low voltage, all inputs	−1 V to 0.8 V	Note 2

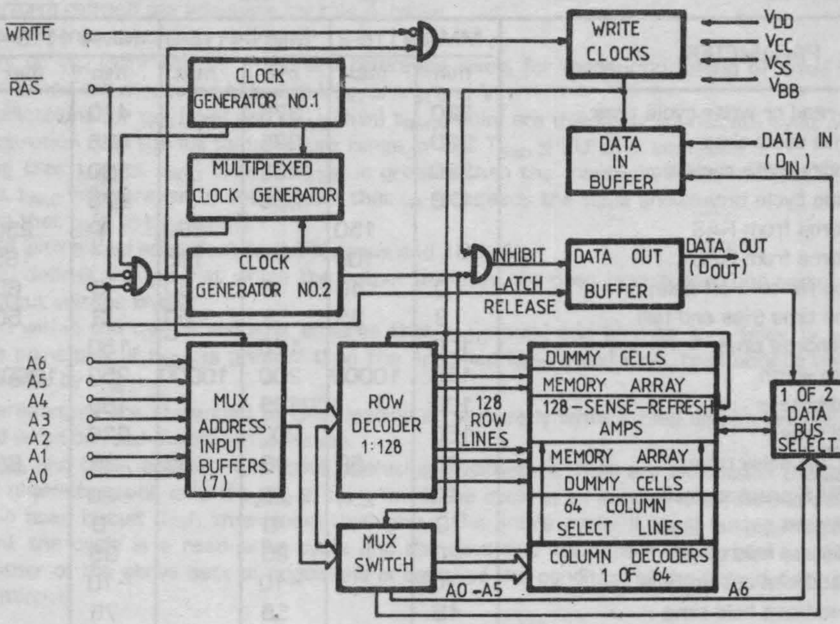
PIN CONNECTIONS



PIN NAMES

$A_0 - A_6$	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
DIN	DATA IN
D_{OUT}	DATA OUT
RAS	ROW ADDRESS STROBE
WRITE	READ/WRITE INPUT
V_{BB}	POWER (−5 V)
V_{CC}	POWER (+5 V)
V_{DD}	POWER (+12 V)
V_{SS}	GROUND

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C)[1], (V_{DD} = 12V ± 10%; V_{BB} = -5.7 to -4.5V; V_{SS} = 0V; V_{CC} = 5V ± 10%)

	PARAMETER	TEST CONDITIONS	MMN 4116-2/3 min	MMN 4116-2/3 max	MMN 4116-4 min	MMN 4116-4 max	UNIT	NOTES
I_{DD1}	Average operating current	$\overline{RAS}$, $\overline{CAS}$ cycling		35		35	mA	4
I_{CC1}	Average operating current							5
I_{BB1}	Average operating current	$t_{RC} = t_{RC}$ (min)		200		200	μA	
I_{DD2}	Standby current	$\overline{RAS} = V_{IHC}$		1.5		1.5	mA	
I_{CC2}	Standby current	D_{OUT} = High impedance	-10	10	-10	10	μA	
I_{BB2}	Standby current			100			μA	
I_{DD3}	Refresh average current	Refresh mode: RAS cycling		27		27	mA	4
I_{CC3}	Refresh average current	$\overline{CAS} = V_{IHC}$	-10	10	-10	10	μA	
I_{BB3}	Refresh average current	$t_{RC} = t_{RC}$ (min)		200			μA	
I_{DD4}	Page mode average current	Page mode: RAS = V_{IL}		27		27	mA	4
I_{CC4}	Page mode average current	CAS cycling					A	5
I_{BB4}	Page mode average current	$t_{PC} = t_{PC}$ (min)		200			μA	
$I_{I(L)}$	Input leakage current	$V_{BB} = -5$ V $0V \leq V_{IN} \leq +7$ V, all other pins not under test = 0V	−10	10	−10	10	μA	
$I_{O(L)}$	Output leakage current	D_{OUT} is disabled $0V \leq V_{OUT} \leq +5.5$ V	−10	10	−10	10	μA	
V_{OH}	Output high voltage	$I_{OUT} = -5$ mA	2.4		2.4		V	3
V_{OL}	Output low voltage	$I_{OUT} = 4.2$ mA		0.4		0.4	V	3

AC ELECTRICAL CHARACTIRISTICS AND RECOMMENDED OPERATING CONDITIONS

(T_A = 0 to 70°C)[1], (V_{DD} = 12 V ± 10%; V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{BB} = −5.7 to −4.5 V)

PARAMETER		MMN 4116-2		MMN 4116-3		MMN 4116-4		UNIT	NOTES
		min	max	min	max	min	max		
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read modify write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	9
t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	10,12
t_{CAC}	Access time from $\overline{CAS}$		100		135		165	ns	11,12
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ precharge time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	$\overline{RAS}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	50	25	65	35	86	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	−20		−20		−20		ns	
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	−10		−10		−10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to RAS	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	15
t_{DH}	Data-in hold time	45		55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	CAS precharge time (for page mode cycle only)	60		80		100		ns	
t_{REF}	Refresh period		2		2		2	ms	
t_{WCS}	$\overline{WRITE}$ command set-up time	−20		−20		−20		ns	16
t_{CWD}	CAS to $\overline{WRITE}$ delay	60		80		90		ns	16
t_{RWD}	RAS to $\overline{WRITE}$ delay	110		145		175		ns	16

NOTES

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention.However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3} and I_{DD4} depend on cycle rate.

5. I_{CC1} and I_{CC4} depend upon output loading. During read out of high level data V_{CC} is connected through a low impedance to data out. At all other times I_{CC} consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume $t_T = 5$ ns.
8. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) and t_{RWC} (min) t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_{amb} \leq 70°C$) is assured.
10. Assuming that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assuming that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100 pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is exclusively controlled by t_{CAC}.
15. These parameters are eferenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and data output pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta v = 3$ volts and power supplies at nominal levels.
18. $\overline{CAS} = V_{IHC}$ to disable D_{OUT}.

DESCRIPTION

System oriented features include ±10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MMN 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MMN 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MMN 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information. Note that CAS can be activated at any time after t_{RAH} and it will have no effect on the worst case data acces time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max.) No data storage or reading errors will result if $\overline{CAS}$ is applied to the MMN 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to CAS. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$). Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MMN 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition. If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address. Strobe during read operations. Note also that even through data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection — Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X, Y) chip select array can be realized.

Extended Page Boundary — Page — mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column location in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically.

The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MMN 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MMN 4116 allows for successive memory operations at multiplie column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MMN 4116 is limited to the 128 column locations determined by all combi-

nations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and the $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MMN 4116 is dynamic and most of the power drawn is the result of an address strobe edge.

Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle. This current characteristic of the MMN 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability, Bulk capacitance requirements are minimal since the MMN 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipations, the operating frequency (cycle rate) of the MMN 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit equation.

Note: The MMN 4116 is guaranteed to have a maximum I_{DD1} requirement with an ambient temperature from 0° to 70°C.

1 microsecund cycle, results in a reduced maximum I_{DD1} requirement of under 20 mA with an ambient temperature range from 0° to 70°C.

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoder and used as a chip select signal for the MMN 4116 overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

POWER UP

The MMN 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MICROELECTRONICA recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

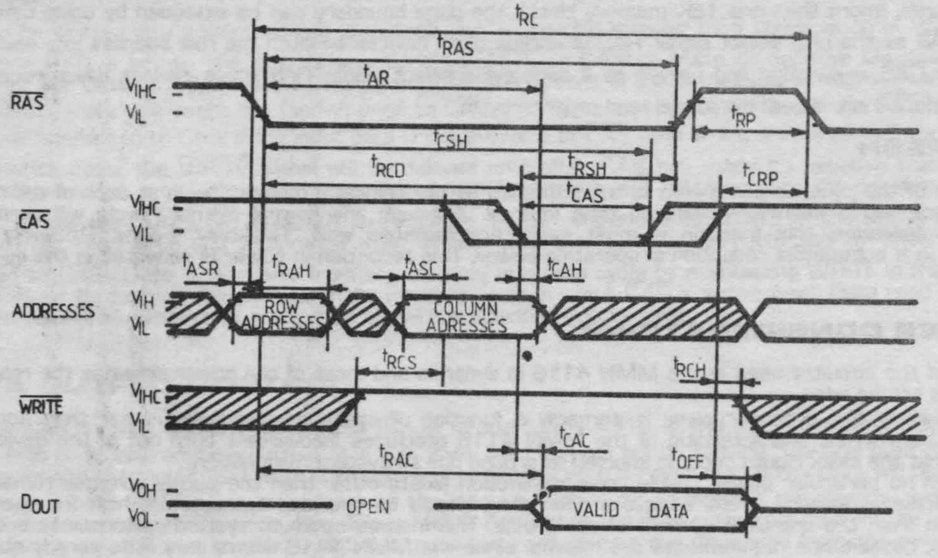
After power is applied to the device, the MMN 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

CAPACITANCES

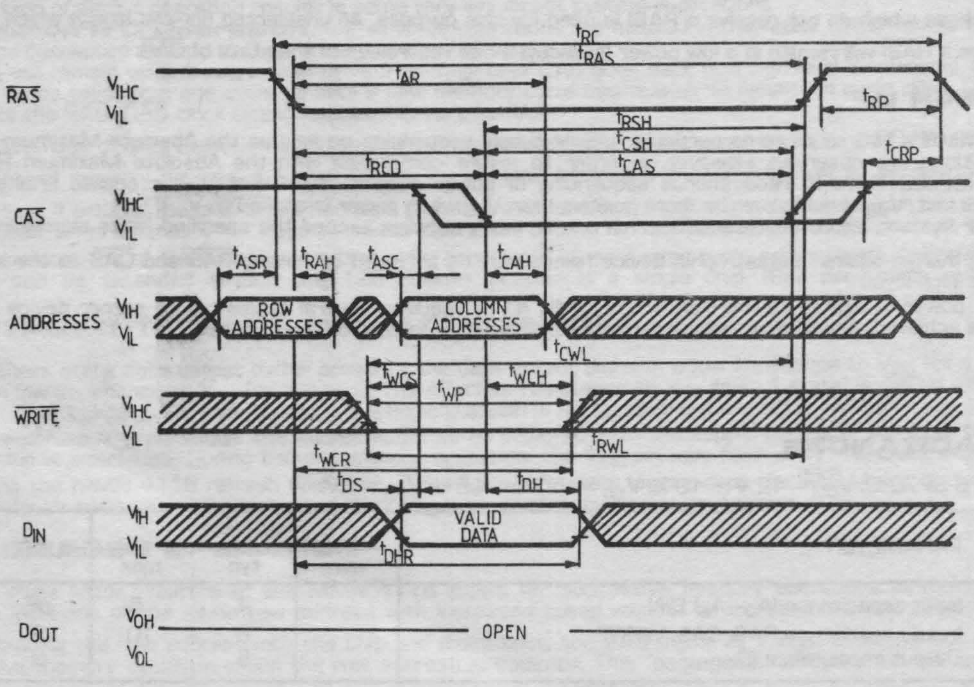
(T_{amb} = 0 to 70°C; V_{DD} = 12 V ± 10%; V_{BB} = -5.7 to -4.5 V; V_{SS} = 0V)

	PARAMETER	RATING min	RATING typ	RATING max	UNIT	NOTES
C_{i1}	Input capacitance (A_0—A_6) DIN		4	5	pF	17
C_{i2}	Input capacitance RAS, CAS, WRITE		8	10	pF	17
C_o	Output capacitance (D_{OUT})		5	7	pF	17,18

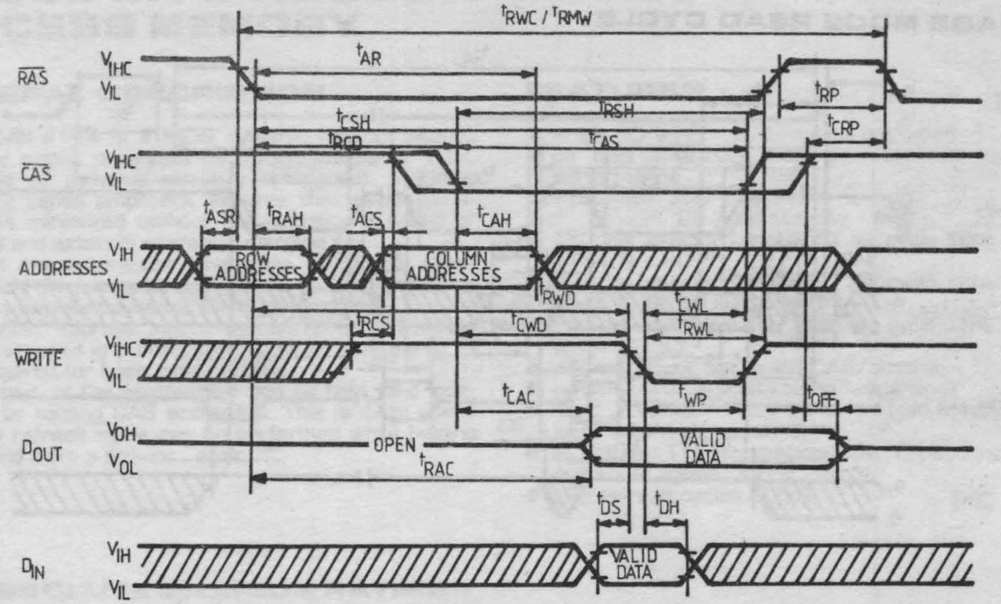
READ CYCLE



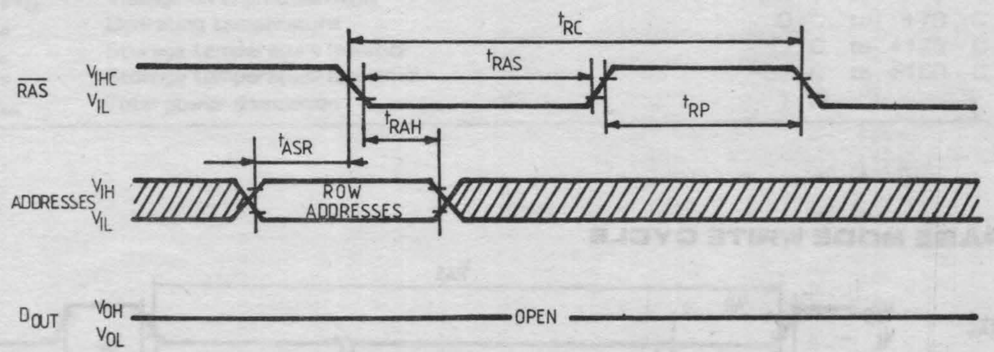
WRITE CYCLE (EARLY WRITE)



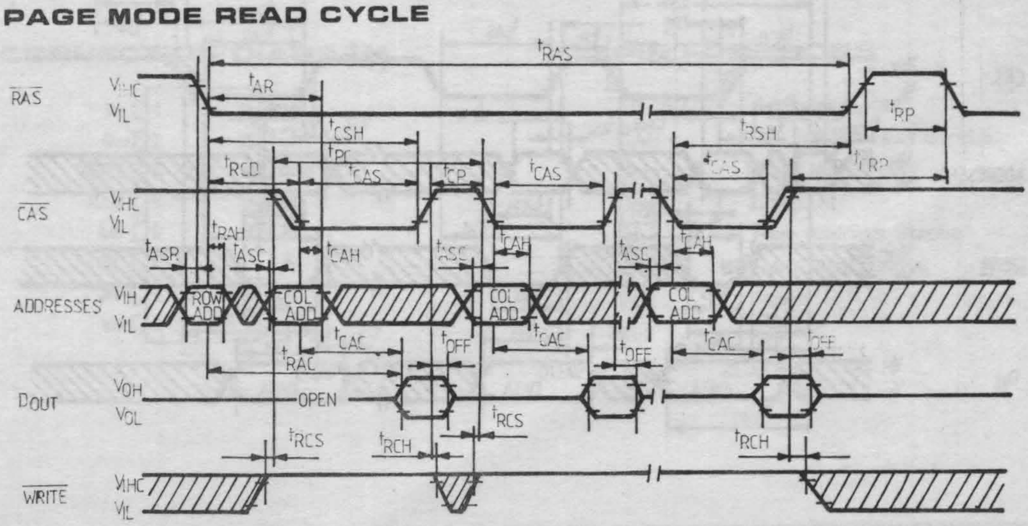
READ WRITE/READ MODYFY - WRITE CYCLE



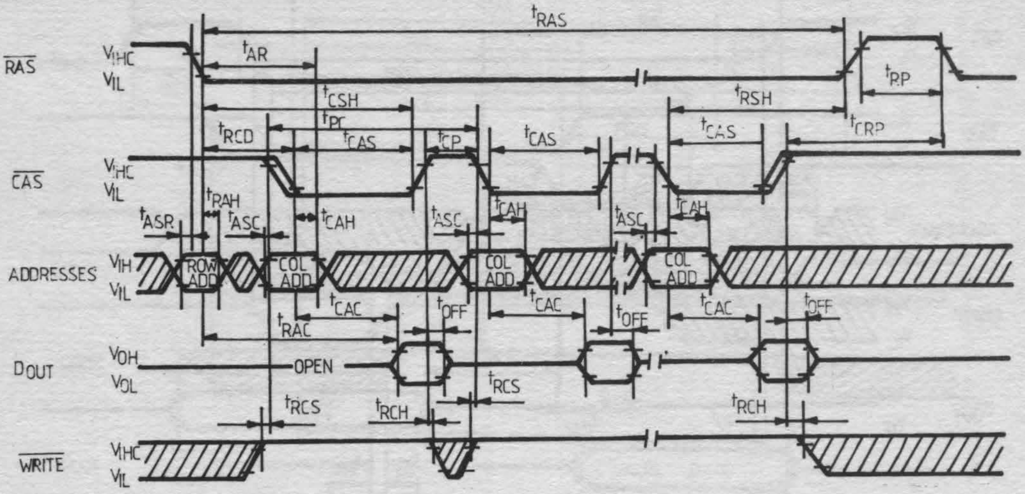
"RAS-ONLY" REFRESH CYCLE



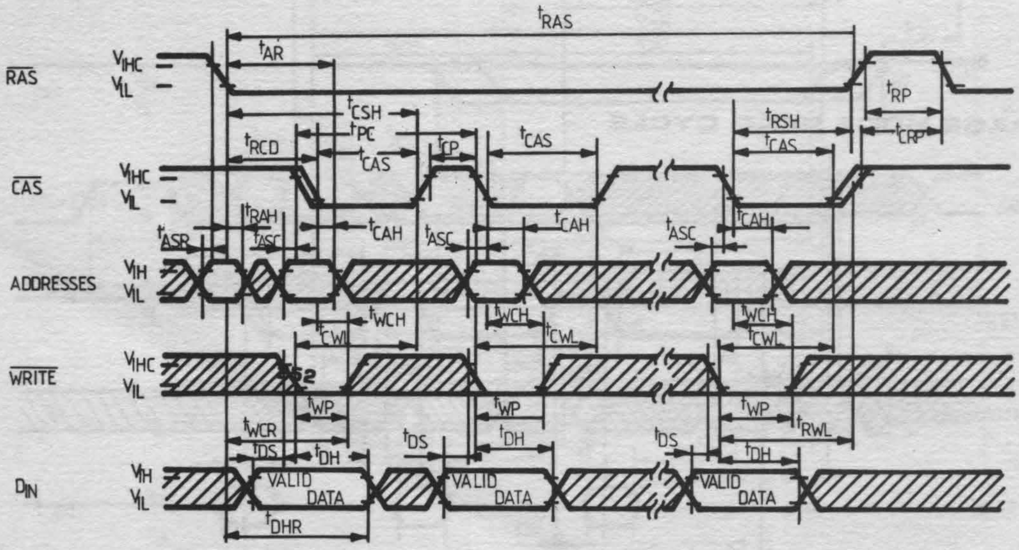
PAGE MODE READ CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



65536-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 4164 is a MOS dynamic random access memory circuit organized as 65536 words by 1 bit. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins.
Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.
Multiplexed address inputs permits the MMN4164 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality.
The output of the MMN4164 can be held valid indefinitely by holding $\overline{CAS}$ active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previou cycle.

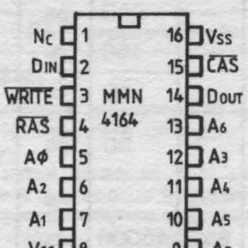
FEATURES

- single +5 V (+/−10%) supply operation
- on chip substrate bias generator for optimum performance
- low power 300 mW active max
28 mW standby max
- 150 ns access time, 270 ns cycle time (MMN 4164.1)
- 200 ns access time, 330 ns cycle time (MMN 4164.2, .3)
- 250 ns access time, 410 ns cycle time (MMN 4164.4)
- indefinite Dout hold using CAS/control
- common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- all inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2 mS)

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage relative to V_{SS}	−0.5 V	to	+7.0	V
V_I, V_O	Voltage on anyI/O terminal	−2.0 V	to	+7.0	V
T_A	Operating temperature	0 C	to	+70	C
T_s	Storage temperature (plastic)	−55 C	to	+125	C
Ts	Storage temperature (ceramic)	−65 C	to	+150	C
P_{tot}	Total power dissipation	1 W			

CONNECTION DIAGRAM



PIN FUNCTIONS

A0...A7	Address inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read Write Input
Vcc	Power (+5 V)
Vss	Ground

RECOMMENDED DC OPERATING CONDITIONS

($T_A = 0$ to 70°C)

PARAMETER		MMN 4164.2 MIN	MMN 4164.2 TYP	MMN 4164.2 MAX	MMN 4164.1,.3,.4 MIN	MMN 4164.1,.3,.4 TYP	MMN 4164.1,.3,.4 MAX	UNIT	NOTES
V_{CC}	Supply voltage	4,5	5,0	5,5	4,75	5,0	5,25	V	1
V_{iH}	Input high (logic 1) voltage	2,4	—	5,5	2,4	—	5,25	V	1
V_{iL}	Input low (logic 0) voltage*	−0,3	—	0.8	−0,3	—	0,8	V	1

*) Input low voltage may reach −2V for a time period shorter than 40 ns.

DC ELECTRICAL CHARACTERISTICS

($T_A = 0$ to 70°C, $V_{CC} = 5.0$ V ±5% or 10% depending on type specified above)

PARAMETER		CONDITIONS	VALUE MIN	VALUE MAX	UNIT	NOTES
I_{cco}	Operating current ($\overline{RAS} - \overline{CAS}$ cycle)	$t_{RLRL} = t_{RLRL}$min $T = 25$°C	—	55	mA	2
I_{ccr}	Standby current	$\overline{RAS} = V_{ih}$ DO = High Z	—	5	mA	2
I_{li}	Input leakage	$V_i = 0 ... Vcc$	−10	10	μA	
I_{lo}	Output leakage	$Vo = 0...Vcc$ DO = High Z $\overline{RAS}$ $\overline{CAS}$ $= V_{ih}$	−10	10	μA	
V_{oH}	Output high (logic 1) voltage	$I_O = -4$ mA	2,4	—	V	
V_{oL}	Output low (logic 0) voltage	$I_O = 4$ mA	—	0,4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(NOTES 3, 4, 5, 15)

($T_A = 0$ to 70°C, $V_{CC} = 5.0$ V +/− 5% or 10% depending on type)

PARAMETER		MMN 4164.1 min.	MMN 4164.1 max.	MMN 4164.2, .3 min.	MMN 4164.2, .3 max.	MMN 4164.4 min.	MMN 4164.4 max.	UNIT	NOTES
t_{RLRL}	Random read or write cycle time	270	—	330	—	410	—	ns	6,7
t_{RLRL}	Read modify write cycle time	300	—	375	—	445	—	ns	6,7
t_{CLCL}	Page mode cycle time	170	—	200	—	280	—	ns	6,7
t_{RLOV}	Access time from RAS	—	150	—	200	—	250	ns	7,8
t_{CLOV}	Access time from CAS	—	100	—	110	—	150	ns	7,9
t_{CHOX}	Output buffer turn-off delay	—	50	—	50	—	50	ns	10
t_{THL} t_{TLH}	Transition time (rise and fall)	3	50	3	50	3	50	ns	5
t_{RHRL}	$\overline{RAS}$ precharge time	100	—	120	—	150	—	ns	
t_{RLRH}	$\overline{RAS}$ pulse width	150	10000	200	10000	250	10000	ns	
t_{CLRH}	$\overline{RAS}$ hold time	100	—	110	—	150	—	ns	
t_{RLCH}	$\overline{CAS}$ hold time	150	—	200	—	250	—	ns	
t_{CLCH}	$\overline{CAS}$ pulse width	100	10000	110	10000	150	10000	ns	
t_{RLCL}	$\overline{RAS}$ to $\overline{CAS}$/delay	25	50	45	90	75	100	ns	11

PARAMETER		MMN 4164.1		MMN 4164.2, .3		MMN 4164.4		UNIT	NOTES
		min.	max.	min.	max.	min.	max.		
t_{RHWL}	Read command hold time from $\overline{RAS}$	0	—	0	—	0	—	ns	12
t_{ZVRL}	Row address set-up time	0	—	0	—	0	—	ns	
t_{RLZX}	Row address hold time	15	—	30	—	45	—	ns	
t_{SVCL}	Column address set-up time	0	—	0	—	0	—	ns	
t_{CLSX}	Column address hold time	45	—	45	—	60	—	ns	
t_{RLSX}	Column address hold time from $\overline{RAS}$	95	—	135	—	160	—	ns	
t_{WHCL}	Read command set-up time	0	—	0	—	0	—	ns	
t_{CHWL}	Read command hold time from $\overline{CAS}$	0	—	0	—	0	—	ns	12
t_{CLWH}	Write command hold time	45	—	40	—	50	—	ns	
t_{RLWH}	Write command hold time from $\overline{RAS}$	95	—	130	—	155	—	ns	
t_{WLWH}	Write command pulse width	45	—	45	—	50	—	ns	
t_{WLRH}	Write command to $\overline{RAS}$ lead time	60	—	50	—	60	—	ns	
t_{WLCH}	Write command to $\overline{CAS}$ lead time	60	—	50	—	60	—	ns	
t_{IVCL}	Data-in set-up time from $\overline{CAS}$	0	—	0	—	0	—	ns	13
t_{IVWL}	Data-in set-up time from $\overline{WE}$	0	—	0	—	0	—	ns	13
t_{CLIX}	Data-in hold time	45	—	45	—	60	—	ns	13
t_{RLIX}	Data-in hold time from $\overline{RAS}$	95	—	135	—	160	—	ns	
t_{CHCL}	$\overline{CAS}$ precharge time for page mode only	60	—	80	—	120	—	ns	
t_{REF}	Refresh period	—	2	—	2	—	2	ms	
t_{WLCL}	Write command set-up time	0	—	0	—	0	—	ns	14
t_{CLWL}	$\overline{CAS}$ to $\overline{WE}$ delay	70	—	85	—	120	—	ns	14
t_{RLWL}	$\overline{RAS}$ to $\overline{WE}$ delay	120	—	175	—	220	—	ns	14
t_{CHCL}	$\overline{CAS}$ precharge time	25	—	45	—	90	—	ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 100 μs is required after power-up followed by 8 RAS cycles before proper device operation is achieved.
4. AC characteristics assume $t_T = 5$ ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RLCL} \leq t_{RLCL}$ (max). If t_{RLCL} is greater than the maximum recommended value shown in this table, t_{RLOV} will increase by the amount that t_{RLCL} exceeds the value shown.
9. Assumes that $t_{RLOV} \geq t_{RLCL}$ (Max).
10. t_{CHOX} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

11. Operation within the t_{RLCL} (max) limit insures that t_{RLOV} (max) can be met t_{RLCL} (max) is specified as a reference point only is t_{RLCL} is greater than the specified t_{RLOV} (max) limit, then access is controlled exclusively by t_{CLOV}.
12. Either t_{RHWL} or t_{CHWL} must be satisfied for a read cycle.
13. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read modify write cycles.
14. t_{WLCL}, t_{CLWL} and t_{RLWL} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only if $t_{WLCL} \geq t_{WLCL}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CLWL} \geq t_{CLWL}$ (min) and $t_{RLWL} \geq t_{RLWL}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until CAS goes back to V_{IH}) is indeterminate.
15. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

OPERATION

The 16 address bits required to decode 1 of 65.536 cell locations within the MMN4164 are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock. Row Address Strobe (RAS), latches the 8 row addresses into the chip.

The high-to-low transition of the second clock, Column Address Strobe (CAS), subsequently latches the 8 column addresses into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the CAS clock sequence are inhibited until the occurence of a delayed signal derived from the RAS clock chain. The "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated CAS" feature permits CAS to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of CAS which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if CAS is applied to the MMN4164 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAS}) rather than from RAS (t_{RAS}), and RAS acces time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The latter of WRITE or CAS to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS being brought low (active); the D_{IN} is strobed by CAS, and the Input Data set-up and hold times are referenced to CAS. If the input data is not available at CAS time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the WRITE signal should be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which both the RAS and CAS are low (active) Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MMN4164 is the high impedance (open-circuit) state, any time CAS is high (inactive) the D_{OUT} pin will be floating .Once the output data port has gone active it will remain valid until CAS is taken to the precharge (inactive high) state. Note that CAS can be left active (low) indefinitely. This permits either RAS-only or RFSH refresh cycles to occur without invaliding D_{OUT}.

PAGE MODE OPERATION

The Page Mode feature of the MMN 4164 allows for succesive memory operations at multiple column locations within the same row address.This is done by strobing the row address into the chip and maintaining the RAS signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to CAS). With the MMN 4164 this results in as much as a 50% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MMN 4164 is limited to the 256 column locations determined by all combinations of the 8 column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read write and read modify-write cycles are permitted within the page mode operation.

REFRESH

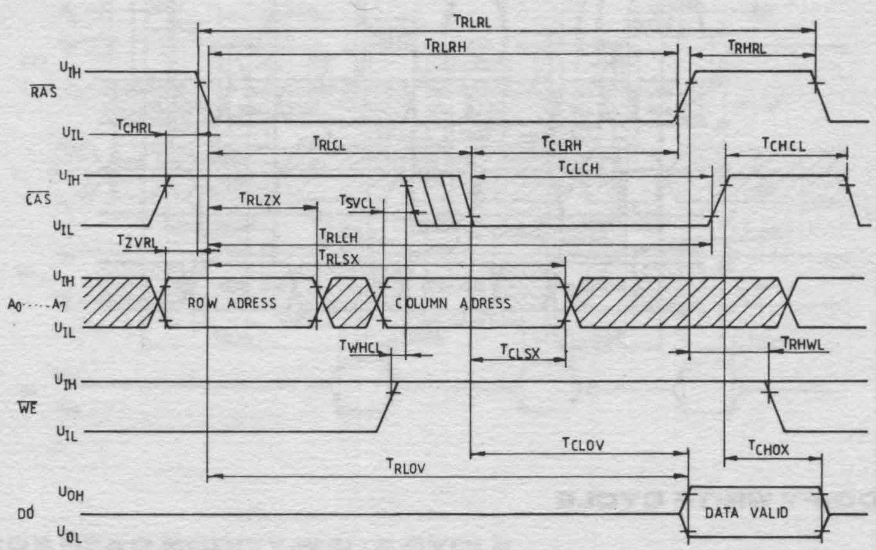
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing this function is easily accomplished by using either RAS-only or RFSH type refreshing.

RAS-ONLY REFRESH

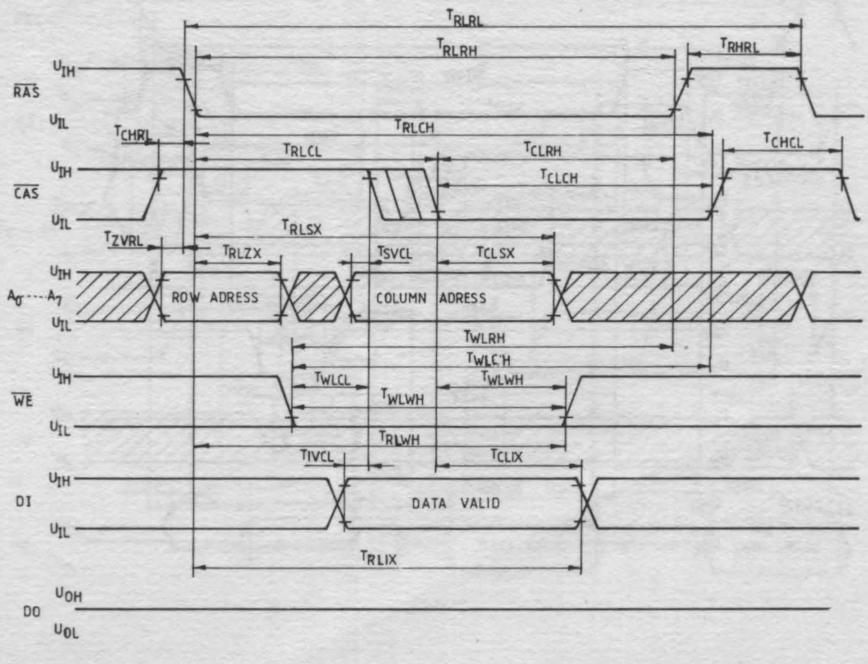
The RAS-only refresh cycle supported by the MMN

4164 requires that a 7 bit refresh address be valid at the device address inputs when RAS goes low (active). The state of the output data port during a RAS-only refresh is controlled by CAS. If CAS is high (inactive) during the entire time that RAS is asserted, the output will remain in the high impedance state. If CAS is low (active) the entire time that RAS is asserted, the output port will remain in the same state that it was prior to the issuance of the RAS signal. This is useful for single step operation. If CAS makes a low-to-high transition during the RAS-only refresh cycle, the output data buffer will assume the high impedance state.

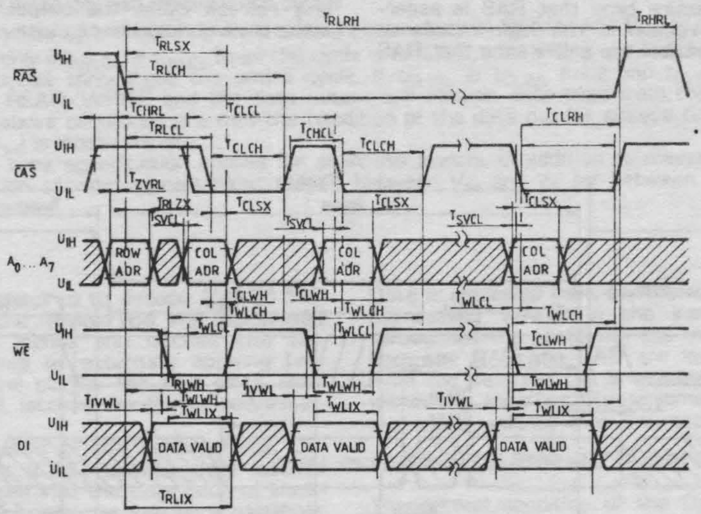
READ CYCLE



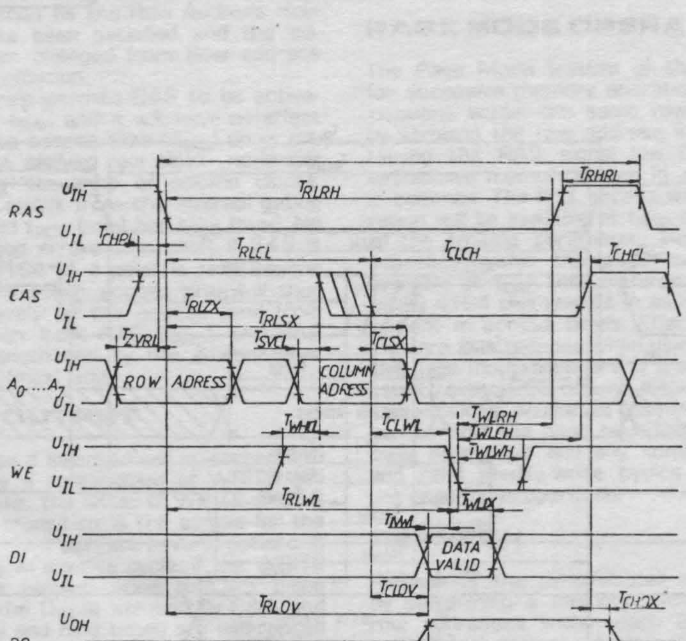
WRITE CYCLE



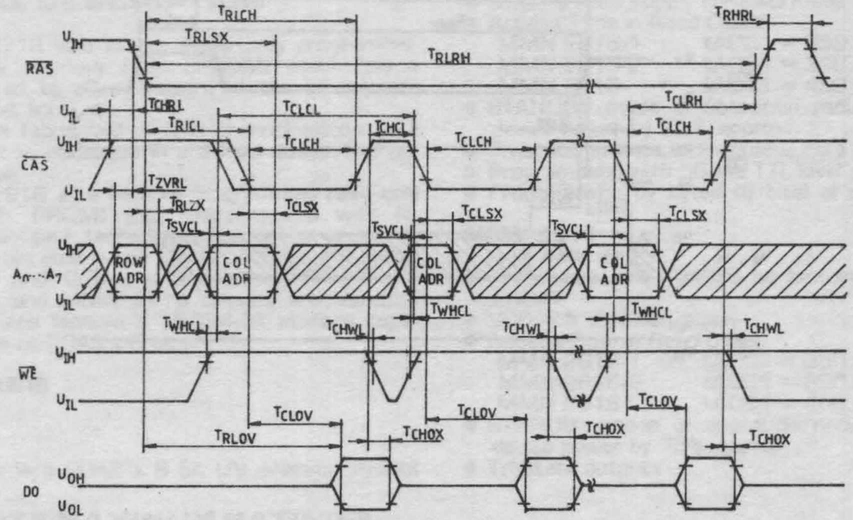
PAGE MODE WRITE CYCLE



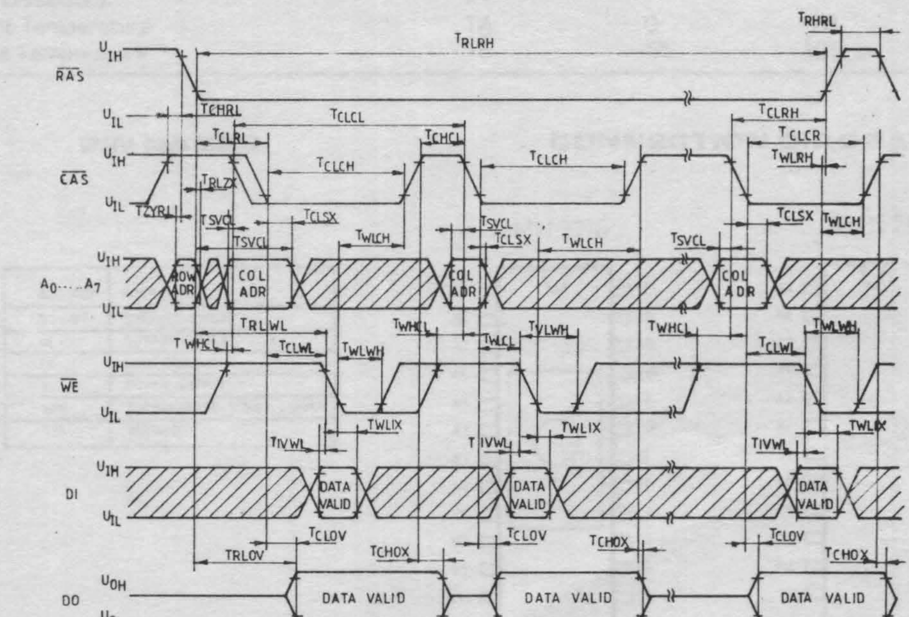
READ MODIFY WRITE CYCLE



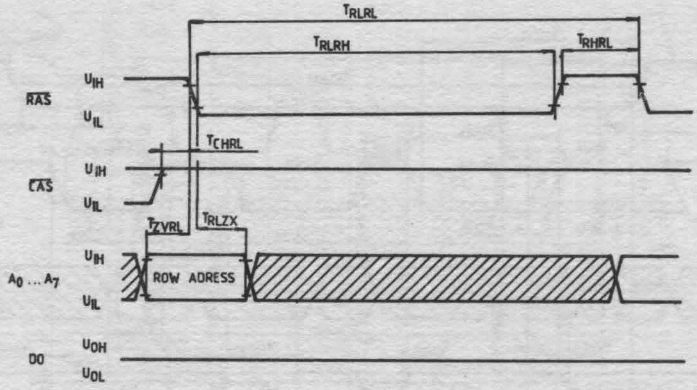
PAGE MODE READ CYCLE



PAGE MODE READ MODIFY-WRITE CYCLE



RAS-ONLY-REFRESH CYCLE



MMN 2716:2048 x 8 BIT EPROM

MMN 2616:2048 x 8 BIT PROM

GENERAL DESCRIPTION

The MMN 2716 is a static, electrically programmable read-only memory (16k EPROM) which has a transparent lid to allow erasure of the bit pattern with ultraviolet light.
The device is fabricated with N-channel silicon gate technology. It is packaged in a 24-pin dual-in-line ceramic package.
The MMN 2616 is a factory-programmed read-only memory (16k PROM) also manufactured with N-channel silicon gate technology. The device is packaged in a 24-pin dual-in-line plastic pckage. Pin assignment; A.C. and D.C. characteristics of both the MMN 2616 and MMN 2716 circuits are identical. The two devices feature a 16,384-bit storage capacity organized as 2048 x 8 bits.

FEATURES

MMN2716

- The device is a 2048 x 8 bit UV erasable PROM
- Single 5 volts supply in READ mode
- Access Time in Read Cycle:
  MMN 2716-1 tACC1 = 350 ns
  MMN 2716-2 tACC1 = 390 ns
  MMN 2716 tACC1 = 450 ns
- STANDBY mode of operation reduces the active device power by 75% approx.
- Tri-state outputs, bidirectional data pins
- Programming with 50-ms TTL level pulses
- Programming by bytes (8 bits) of data is possible

MMN 2616

- The device is a 2048x8 bit factory-programmable PROM
- VCC = 5 V power supply
- Access Time in Read Cycle:
  MMN 2616-1 tACC1 = 350 ns
  MMN 2616-2 tACC1 = 390 ns
  MMN 2616 tACC1 = 450 ns
- STANDBY mode of operation reduces the active device power by 75% approx.
- Tri-state outputs

ABSOLUTE MAXIMUM RATINGS
(Voltages relative to Vss = 0V)

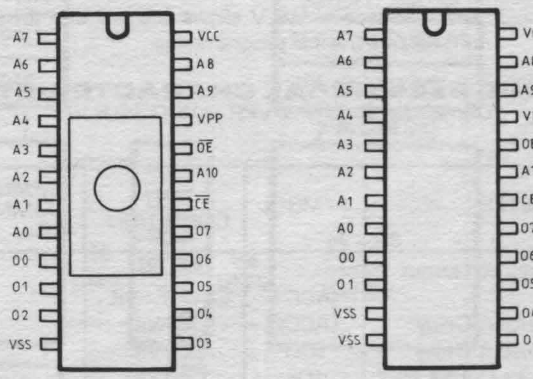
PARAMETER	SYMBOL	Min.	Max.	UNITS
Voltage on any pin except VPP	VT	–0,5	6,5	V
VPP Supply Voltage	VPP	–0,5	26,0	V
Power Dissipation	PT		1	W
Ambient Temperature	TA	0	70	°C
Storage Temperature	TS	–55	125	C

PIN NAMES

A0 A10	ADDRESSES
00 - 07	OUTPUTS INPUTS
OE	OUTPUT ENABLE
CE	CHIP ENABLE
VCC	POWER SUPPLY
VPP	PROGRAMMING POWER SUPPLY
VSS	GROUND

CONNECTION DIAGRAM

MMN 2716 MMN 2616



STATIC ELECTRICAL CHARACTERISTICS
(Voltages relative to Vss = 0V)

PARAMETER	SYMBOL	TEST CONDITION	Min.	Typ.	Max.	UNITS
Supply Voltage	VCC		4,75	5	5,25	V
VPP Supply Voltage with respect to Ground during Read	VPP		VCC −0,6	VCC	VCC +0,6	V
Input Low Voltage	VIL		−0,3		0,8	V
Input High Voltage	VIH		2,0		VCC +1	V
Input Leakage Current	ILI	VI=5,25 V			10	μA
Output Leakage Current	ILO	VO=5,25 V OE=VIH			10	μA
Output Law Voltage	VOL	IOL = 2,1 mA			0,4	V
Output High Voltage	VOH	IOH=−0,4 mA	2,4			V
Operating Temperature	TA		0	25	70	°C

PARAMETER	SYMBOL	TEST CONDITION	MMN2616 MMN2716 Min.	Max.	MMN2716-1 MMN2616-1 Min.	Max.	MMN2716-2 MMN2616-2 Min.	Max.	UNITS
VCC Standby Power Supply Current	ICC1	OE=VIL CE=VIH		25		30		25	mA
VCC Active Power Supply Current	ICC2	OE=VIL CE=VIL		100		120		100	mA
VPP Supply Current (in READ mode)	IPP1	VPP=5,25		5		6		5	mA
VPP Supply Current during Programming Pulse (MMN2716)	IPP2	VPP=25		30		40		30	mA

NOTES :
1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP
2. VPP may be connected directly to VCC except during programming. The supply current would then be the sum of ICC and IPP1.
3. The tolerance of 0,6 V allows the use of a driver circuit for switching the VPP supply pin from VCC in read to 25 V for programming.

DYNAMIC ELECTRICAL CHARACTERISTICS
(TA = 0C − 70C, VCC = 5V ±5%, VPP = VCC ±0,6 V)

PARAMETER	SYMBOL	TEST CONDITION	MMN2616 MMN2716 Min.	Max.	MMN2716-1 MMN2616-1 Min.	Max.	MMN2716-2 MMN2616-2 Min.	Max.	UNITS
Addresses to Output Delay	tACC1	$\overline{CE}$=$\overline{OE}$=VIL		450		350		390	ns
$\overline{CE}$ to Output Delay	tACC2	$\overline{OE}$=VIL		450		350		390	ns
$\overline{OE}$ to Output Delay	tCO	$\overline{CE}$=VIL		120		120		120	ns
$\overline{OE}$ High to Output Hi-Z	tDF	$\overline{CE}$=VIL		100		100		100	ns
$\overline{CE}$ High to Output Hi-Z	tPF			100		100		100	ns

CAPACITANCES

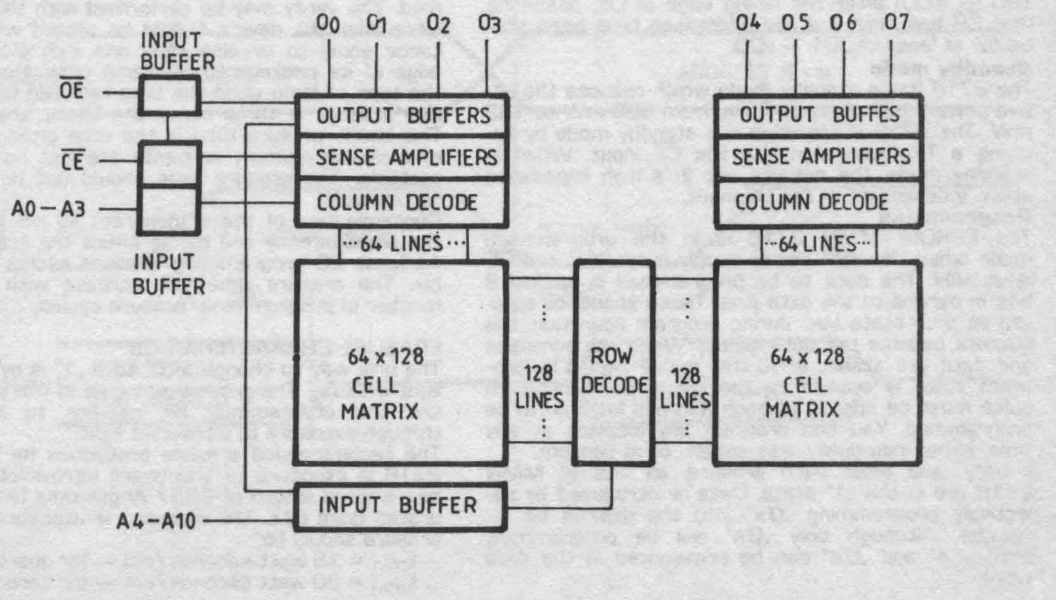
PARAMETER	SYMBOL	TEST	Min.	Max.	UNITS
Input capacitance (A0-A10, CE, OE)	CIN	f = 1 MHz		6	pF
		V = 0 V			
Output capacitance	COUT	TA = 25°C		12	pF

PROGRAM OPERATION

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNITS
VPP Supply Voltage	VPP	24	25	26	V
Operating Temperature	TA	20	25	30	C
Address Setup Time	tAS	2			μs
$\overline{OE}$ Setup Time	tCSS	2			μs
Data Setup Time	tDS	2			μs
Address Hold Time	tAH	2			μs
$\overline{OE}$ Hold Time	tCSH	2			μs
Data Hold Time	tDH	2			μs
$\overline{OE}$ = VIH to Output Hi-Z Delay ($\overline{CE}$ = VIL)	tDF	0		120	ns
$\overline{OE}$ = VIL to Output Delay ($\overline{CE}$ = VIL)	tCO			120	ns
Program Pulse Width	tPW	45	50	55	ms
Program Pulse Rise Time	tPRT	10			ns
Program Pulse Fall Time	tPFT	10			ns

NOTES :
1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP. The 2716 must not be inserted into or removed from a board with VPP at 25±1 V to prevent damage to the device.
2. The maximum allowable voltage which may be applied to the VPP pin during programming is +26 V. Care must be taken when switching the VPP supply to prevent overshoot exceeding this 26 V maximum specification.

BLOCK DIAGRAM



DEVICE OPERATION

The modes of operation of the MMN2716 and MMN2616 are listed in Table 1 and Table 2.
The power supplies required are VCC and VPP. The VPP power supply must be at 25 V during the three programming modes and must be at 25 V in the three modes.
All input signals are fully TTL compatible during both read and program modes. The data outputs are three state to facilitate memory expansion by OR tying.

Table 1 MMN2716 MODE SELECTION

Mode	VCC (24)	VPP (21)	CE (18)	OE (20)	OUTPUTS 9; 11; 13—17
Read	+5	+5	VIL	VIL	Data Output
Outputs Deselected	+5	+5	VIL	VIH	High impedance state
Standby Mode	+5	+5	VIH	VIL/VIH	High impedance state
Programming	+5	+25	VIH	VIH	Data Input
Program Verify	+5	+25	VIL	VIL	Data Output
Program Inhibit	+5	+25	VIL	VIH	High impedance state

Table 2 MMN2616 MODE SELECTION

Mode	VCC (24)	VPP (21)	CE (18)	OE (20)	OUTPUTS 9; 11; 13—17
Read	+5	+5	VIL	VIL	Data Output
Outputs Deselected	+5	+5	VIL	VIH	High impedance state
Stabdby Mode	+5	+5	VIH	VIL/VIH	High impedance state

Read Mode
The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs.
CHIP ENABLE ($\overline{CE}$) is the power control and should be used for device selection. OUTPUT ENABLE ($\overline{OE}$) is the output control and should be used to gate data to the output pin, independent of device selection. Assuming that addresses are stable, address access time (tACC1) is equal to the delay from $\overline{CE}$ to output (TACC2). Data is available at the outputs 120 ns (tCO) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC1 — tCO.

Standby mode
The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Programming
The EPROM MMN 2716 is in the programming mode when the VPP power supply is at 25V and $\overline{OE}$ is at VIH. The data to be programmed is applied 8 bits in parallel to the data pins. These should be treated as a tri-state bus: during program operation, the outputs become the data inputs. When the adresses and data are stable, a 50 ms, active high, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time, either individually, sequentially or at random.
Initially, and after each erasure, all bits of MMN 2716 are in the „1" state. Data is introduced by selectively programming „0's" into the desired bit locations. Although only „0's" will be programmed, both „1's" and „0's" can be pressented in the data word.

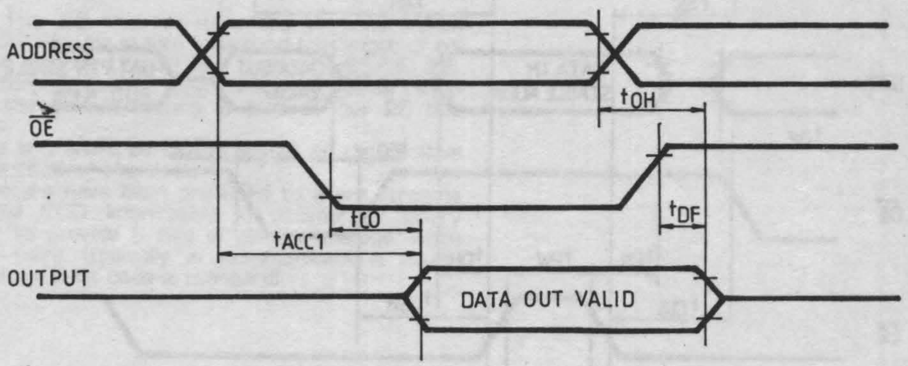
Program inhibit
Programming of multiple MMN 2716 in parallel with different data is also easily accomplished. A TTL level program pulse applied to a MMN 2716's CE input, with VPP at 25V will program that MMN 2716. A low level $\overline{CE}$ input inhibits the other MMN 2716 from being programmed.

Program verify
A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with VPP at 25V. Note that the device should be placed within a distance equal to or less than one inch from the top edge of its package to the lamp tube. Depending on the type of lamp used the time required for an effective erasure is three times the latent erasure time. The latent erasure time is the time after the elapse of wich the memory contents are just no longer detectable. The erasure time should not be less than ten minutes.
Contamination of the transparent lid will deteriorate the transparency and hence affect the erasure time. At least 20 programming/erasure cycles are possible. The erasure time will increase with a greater number of programming/erasure cycles.

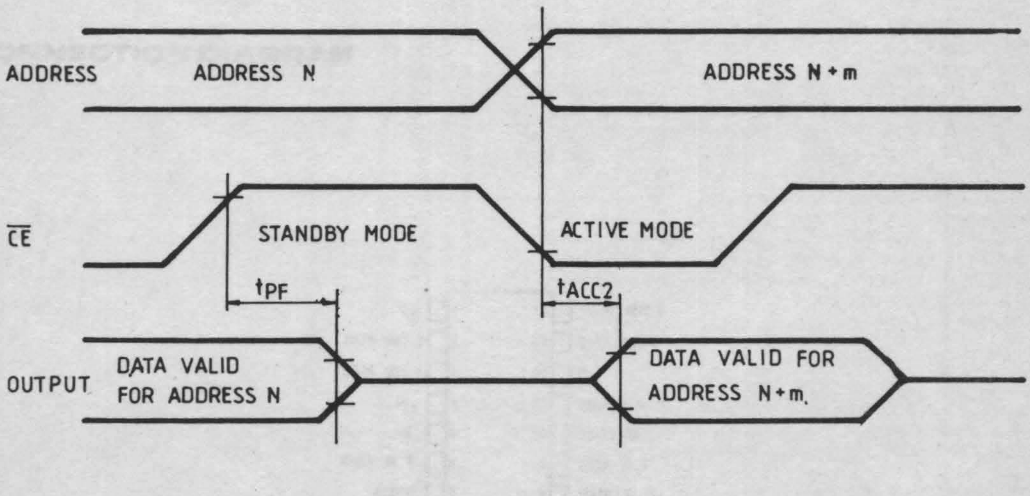
ERASURE CHARACTERISTICS
The only way to change a „0" to a „1" is by ultraviolet light erasure. The window provided in the package allow the programmed bit pattern to be erased through exposure to ultraviolet light.
The recommended erasure procedure for the MMN 2716 is exposure to shortware ultraviolet light wich has a ware length of 2537 Angstroms (A). The integrated dose (U.E. UV intensity ✲ exposure time), for erasure should be:

λ_{min} = 15 watt seconds/cm — for quartz lids.
λ_{min} = 30 watt seconds/cm — for ceramic lids.

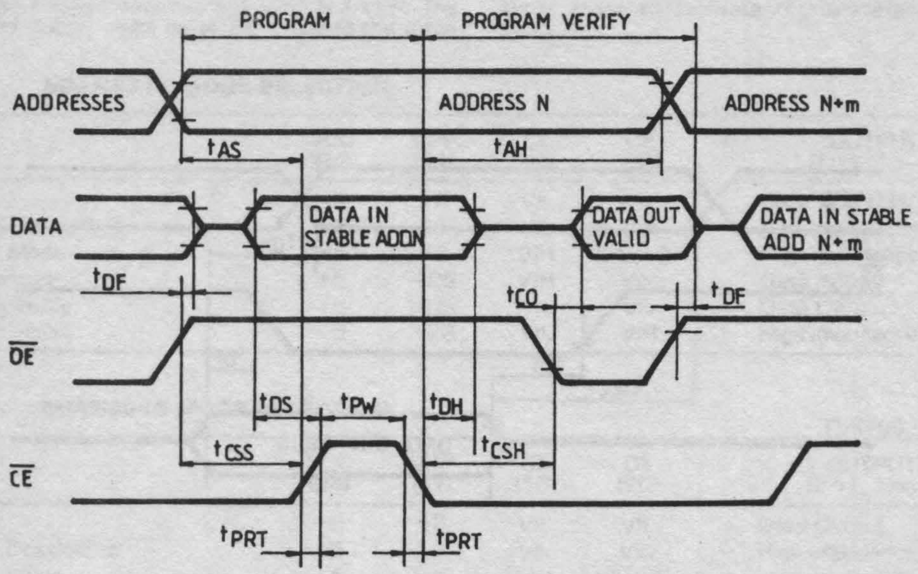
READ WAVEFORMS



POWER DOWN READ WANEFORMS



PROGRAMMING WAVEFORMS



QUAD 25/32 BITS STATIC SHIFT REGISTER

GENERAL DESCRIPTION

The MMN 425 contains four similar N channel silicon gate MOS static shift registers, controlled by a common clock. The length of registers can be 25 or 32 bits each, depending on the voltage level applied on the 25/32 SEL pin. When the 25/32 SEL pin is tied
to V_{CC}, four 25 bits registers are obtained. When the 25/32 SEL pin is tied to ground the length of registers is extended to 32 bits each. The 25/32 SEL pin is internally tied to V_{CC} through a pull-up resistor, so the default setting is that of four 25 bits registers.
The data is transfered to the output on the positive going transition of the clock.
The registers have been produced to store streams of parallel BCD information in decimal or binary bytes or to provide 8 bits of parallel storage, when used in pairs (typically in communications equipments where 8 bit code is standard).

FEATURES

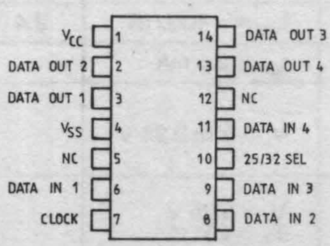
- Power supply $V_{CC} = 5$ V
- TTL compatible inputs and outputs
- Input protected against static charge.

ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (at any pin)	−0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	−33 to 125	°C
T_{op}	Operating temperature under bias	0 to 70	°C

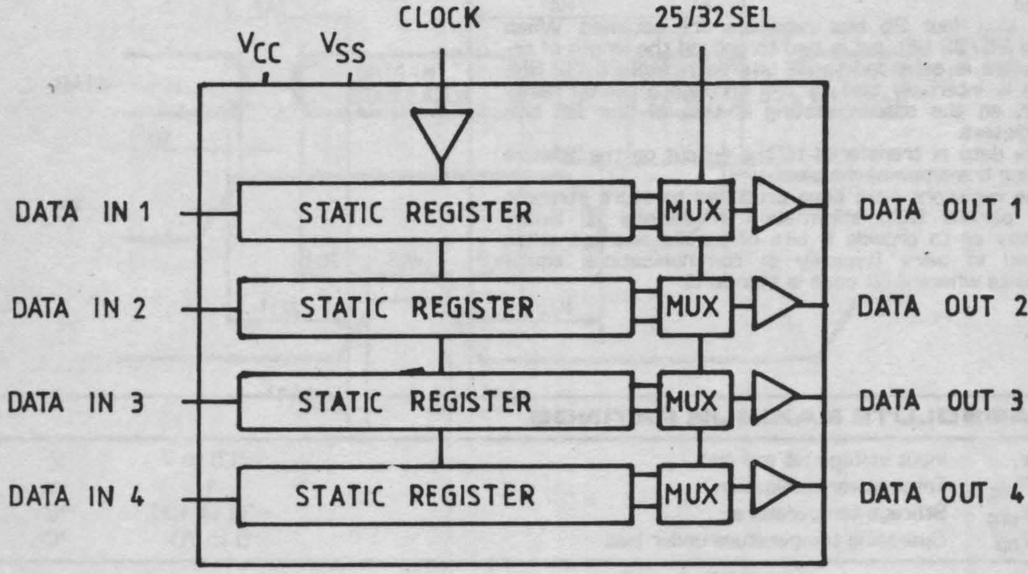
All voltages are referred to GND pin voltage

CONNECTION DIAGRAM



NC=not connected

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4 . 75 to 5 . 25 V, T_A = 0 to 70° C unless otherwise specified)

	PARAMETER	TEST CONDITIONS	VALUES			UNITS
			min.	typ.	max.	
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{OH}	Output High Voltage	$I_{OH} = -100/\mu a$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.4	V
(*) I_{LI}	Input Load Current Data Inputs, Clock Input 25/32 SEL Input	$V_I = 0$ to 5.25 V		1	10 100	/μA /μA
(*). I_{CC}	Supply Current	$V_I = 5.25$ V $T_A = 25°$ C			50	mA

* Typical values for $T_A = 25°$ C and nominal supply voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70° C, V_{CC} = 5 V unless otherwise specified t_r, t_f = 20 ns)

	PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNITS
t_{PHL}	Propagation Delay Time				400	ns
t_{PLH}	Propagation Delay Time				400	ns
t_{THL}	Transition Time				40	ns
t_{TLH}	Transition Time				400	ns
t_{WL}	Minimum Clock Pulse Width		250			ns
$t_{SET\ UP}$	Set-Up Time				100	ns
t_H	Hold Time				300	ns
f_{CL}	Maximum Clock Frequency			2		MHz
C_I	Input Capacitance	T_A = 25° C f = 1 MHz V_I = 0 V			5	pF

INFRARED RECEIVING CIRCUIT FOR REMOTE CONTROL

GENERAL DESCRIPTION

MMN 806 is designed to process 63 commands received (in infrared or by cable) from the emitting MMC 807, its pair circuit. The circuit is also provided with 5 command inputs (LOC A, LOC B, LOC C, LOC D, LOC E) which enable the self generating of 31 commands out of the possible 63, named "Local commands".
The data, sent by the emitter are applied at the RSIGI input and then are checked and decoded in the bit recognition and word forming block.
The obtained signal is transmitted to the internal bus (IBUS) where depending on the command type is ronted to one of the output blocks. Functionally, MMN 806 is structured into two parts: a receiving one for processing the commands LOCAL or remote control) from the emitter and an emitting one for processing the commands of IBUS and generating the output signals. The two parts are connected by a 12 bit IBUS, out of which 6 bits are for data and 6 are inverted.
The commands of the internal bus are valid at the DATA output when DLEN is LOW.
MMN 806 is synchronized by applying a 62.5 kHz frequency at the C input.
The clock frequence is the same respectively to the emitter operating mode (local or infrared remote control) and in order to perform the correct reception and decoding of the command words the following ratio should be observed.
The MMC 807 emitter oscillator frequency (4 MHz) or 62.5 kHz.
The MMN 806 receiver clock frequency (62.5 kHz).

TABLE 1 - MODE SELECT

TYPE	MODE
MMN 806	code ASCII
MMN 806.1	local
MMN 806.2	local

TABLE 2 - PIN FUNCTION

PRIN No.	PIN	FUNCTION
1	RSIGI	Serial input
2	C	Clock
3	RSVD	Inputs/outputs for reservation
10	RSVA	
11	RSVB	
4	MODEP	Selecting input/output
5	ANAL 2	OPEN-DRAIN outputs
6	ANAL 3	
7	ANAL 4	
8	VOLU	
9	OFF	STAND-BY input/output
12	V_{DD}	Power supply
13	DLEN	VALID DATA OPEN DRAIN
14	DATA	Serial data output OPEN-DRAIN
15	PRGD	Input/outout for programm memory
16	PRGC	Outputs OPEN-DRAIN for programm memory
17	PRGA	
18	PRGB	
19	LOCE	Local commands inputs
20	LOCD	
21	LOCC	
22	LOCB	
23	LOCA	
24	V_{SS}	Ground

CONNECTION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage:	−0.3 ...	7	V
V_I	Input voltage	−0.3 ...	15	V
I_I	Input current	−2 ...	2	mA
Io	Output current	0 ...	10	mA
P_o	Output power		50	mW
P_{tot}	Total power dissipation		500	mW
T_A	Operating temperature	0 ...	70	°C
T_{stg}	Storage temperature	−55 ...	125	°C

BLOCK DIAGRAM

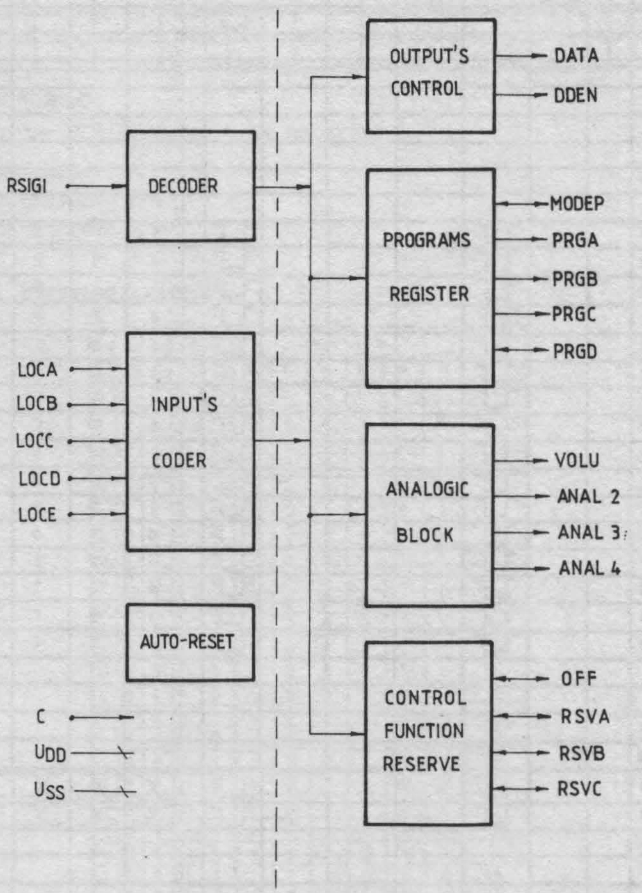


TABLE 3 - IBUS CODE

NO CODE	IBUS CODE F	E	D	C	B	A	1)	OFF	RSVA	RSVB	VOLU	ANAL 2	ANAL 3	ANAL 4	RSVD	MODEP	PRG A	PRG B	PRG C	PRG D	STATUS MMN 806
0	0	0	0	0	0	0	S				19/64	31/64	31/64	31/64							ANALOG POSITION
1	0	0	0	0	0	1	S	0			0										MUTE / ON
2	0	0	0	0	1	0	S	1								1					OFF
3	0	0	0	0	1	1	S		0/1												RESERVE A
4	0	0	0	1	0	0	R8	0								1					ON
5	0	0	0	1	0	1	S	0													ON
6	0	0	0	1	1	0	S	0													RESERVE B / ON
7	0	0	0	1	1	1	S	0													RESERVE C / ON
8	0	0	1	0	0	0	R8														RESERVE D 2)
9	0	0	1	0	0	1	R8														–
10	0	0	1	0	1	0	R8														–
11	0	0	1	0	1	1	R8														–
12	0	0	1	1	0	0	R8														–
13	0	0	1	1	0	1	R8														–
14	0	0	1	1	1	0	R8														–
15	0	0	1	1	1	1	R8														–
16	0	1	0	0	0	0	S	0									1	1	1	1	ON / PROGRAM 16
17	0	1	0	0	0	1	S	0									0	0	0	0	ON / PROGRAM 1
18	0	1	0	0	1	0	S	0									1	0	0	0	ON / PROGRAM 2
19	0	1	0	0	1	1	S	0									0	1	0	0	ON / PROGRAM 3
20	0	1	0	1	0	0	S	0									1	1	0	0	ON / PROGRAM 4
21	0	1	0	1	0	1	S	0									0	0	1	0	ON / PROGRAM 5
22	0	1	0	1	1	0	S	0									1	0	1	0	ON / PROGRAM 6
23	0	1	0	1	1	1	S	0									0	1	1	0	ON / PROGRAM 7
24	0	1	1	0	0	0	S	0									1	1	1	0	ON / PROGRAM 8
25	0	1	1	0	0	1	S	0									0	0	0	1	ON / PROGRAM 9
26	0	1	1	0	1	0	S	0									1	0	0	1	ON / PROGRAM 10
27	0	1	1	0	1	1	S	0									0	1	0	1	ON / PROGRAM 11
28	0	1	1	1	0	0	S	0									1	1	0	1	ON / PROGRAM 12
29	0	1	1	1	0	1	S	0									0	0	1	1	ON / PROGRAM 13
30	0	1	1	1	1	0	S	0									1	0	1	1	ON / PROGRAM 14
31	0	1	1	1	1	1	S	0									0	1	1	1	ON / PROGRAM 15
32	1	0	0	0	0	0	S														–
33	1	0	0	0	0	1	S														–
34	1	0	0	0	1	0	S	0													ON
35	1	0	0	0	1	1	S	0													ON
36	1	0	0	1	0	0	R2	0													ON / PROGRAM +
37	1	0	0	1	0	1	R2	0													ON / PROGRAM –
38	1	0	0	1	1	0	R2	0													ON
39	1	0	0	1	1	1	R2	0													ON
40	1	0	1	0	0	0	R8				→ 1										INTENSITATEA SUNETULUI +
41	1	0	1	0	0	1	R8				→ 0										INTENSITATEA SUNETULUI -
42	1	0	1	0	1	0	R8					→ 1									ANALOG 2+
43	1	0	1	0	1	1	R8					→ 0									ANALOG 2-
44	1	0	1	1	0	0	R8						→ 1								ANALOG 3+
45	1	0	1	1	0	1	R8						→ 0								ANALOG 3 -
46	1	0	1	1	1	0	R8							→ 1							ANALOG 4+
47	1	0	1	1	1	1	R8							→ 0							ANALOG 4-

CODE NO	IBUS CODE F	E	D	C	B	A	1)	I/O OFF	RSVA	RSVB	VOLU	ANAL 2	ANAL 3	ANAL 4	RSVD	MODEP	PRG A	PRG B	PRG C	PRG D	STATUS MMN 806
48	1	1	0	0	0	0	S														–
49	1	1	0	0	0	1	S														–
50	1	1	0	0	1	0	S														–
51	1	1	0	0	1	1	S	0													ON
52	1	1	0	1	0	0	R8	0													ON
53	1	1	0	1	0	1	R8	0													ON
54	1	1	0	1	1	0	R8	0													ON
55	1	1	0	1	1	1	R8	0													ON
56	1	1	1	0	0	0	R8	0								0					ON
57	1	1	1	0	0	1	R8	0								0					ON
58	1	1	1	0	1	0	R8	0								0					ON
59	1	1	1	0	1	1	R8	0								0					ON
60	1	1	1	1	0	0	R8	0								0					ON
61	1	1	1	1	0	1	R8	0								0					ON
62	1	1	1	1	1	0	R8	0								0					ON
63	1	1	1	1	1	1	R8	0								0					ON

Program memory not affected

Program register change

MUTE command for VOLU (output pulse for other pins)

1) S: single command
R2: Repeated command 2/s
R8: Repeated command 8/s

2) MODEP: LOW

TABLE 4 - LOCAL COMMANDS

LOCE	LOCD	LOCC	LOCB	LOCA	IBUS CODE F	E	D	C	B	A	No. Code
1	1	1	1	1	–	–	–	–	–	–	–
0	0	1	1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	0	1	0	2
1	0	1	1	1	0	0	0	1	0	0	4
1	1	0	1	1	0	0	0	1	0	1	5
0	0	1	1	0	0	0	0	1	1	0	6
0	0	1	0	1	0	0	0	1	1	1	7
0	0	0	1	0	0	1	0	0	0	1	17
1	0	1	1	0	1	0	0	0	0	0	32
1	1	1	0	1	1	0	0	0	0	1	33
1	0	0	0	0	1	0	0	0	1	0	34
0	0	0	0	1	1	0	0	0	1	1	35
1	1	1	1	0	1	0	0	1	0	0	36
0	1	1	1	1	1	0	0	1	0	1	37
1	1	0	1	0	1	0	0	1	1	0	38
1	0	0	0	1	1	0	0	1	1	1	39
1	1	0	0	1	1	0	1	0	0	0	40
1	1	0	0	0	1	0	1	0	0	1	41
1	0	1	0	1	1	0	1	0	1	0	42
1	0	1	0	0	1	0	1	0	1	1	43
1	0	0	1	1	1	0	1	1	0	0	44
1	0	0	1	0	1	0	1	1	0	1	45
0	1	0	1	1	1	0	1	1	1	0	46
0	1	0	1	0	1	0	1	1	1	1	47
0	1	1	0	1	1	1	0	0	0	0	48
0	1	1	0	0	1	1	0	0	0	1	49
0	1	0	0	1	1	1	0	0	1	0	50
0	1	0	0	0	1	1	1	0	0	0	56
0	0	1	0	0	1	1	1	0	0	1	57
0	0	0	1	1	1	1	1	0	1	0	58
0	0	0	0	0	1	1	1	0	1	1	59

STATIC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

PARAMETER		TEST CONDITIONS	VALUES		UNIT
			min.	max.	
I_L	Quiescent current	V_i=0V; V_{iL}=0.8V V_{iH}=3.5V; V_o=12V; V_{DD}=5V		35	mA
V_{IL}	Input low voltage	V_{DD}=4.5V	−0.3	1,2	V
V_{IH}	Input high voltage	V_{DD}=5.5V	3.5	12	V
I_I	Input leakage current at RSGI and C	V_{DD}=5.5V; $-3.5 < V_i < 15V$		−10	μA
I_I	Input current at LOCA, LOCE	V_{DD}=5V;V_i=0V; V_i(RSGI,C)=0V		250	μA
I_I	Input current at DLEN; PRGD; MODEP; OFF; RSVD	V_{DD}=5,5V; V_i=0V; V_{IH}=3.5V		250	μA
I_o	Output leakage current at low to high transition for OFF; RSVD; MODEP; DLEN DATA; PRGA; PRGB; PRGD; RSVA; RSVB; PRGC; ANAL2, 3, 4; VOLU	V_{DD}=5V; V_o=15V		25	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	VALUES		UNIT
			min.	max.	
f_C	Clock frequency		56.25	68.8	kHz
	Duty cycle		0.4	0.6	%
t_r	Rise time clock at input			1	μs
t_f	Fall time at clock input			1	μs

FUNCTIONAL DESCRIPTION

The input for remote control receiving of signals (RSIGI).

The serial date generated by MMN 807 (operated in local mode or infrared remote control) are applied at the RSIGI input Where they are checked and decoded. Then the bus is validated and thus the input operating is started.
The signal structure at the RSIGI input is the same with that of the signal at the REMO output of MMC 807.
Thus only the signals consisting of sequences of 7 bit-words (out of which a command bit or start bit noted S and 6 data bits noted A, B, C, D, E, F) are recognized by the receiver and can be decoded.
By inserting the start bit in the command word receiver could be controlled by two emitters, the selection of one of them could be made by connecting the RSVD pin at LOW or HIGH.

From the modulated signal received from the emitting circuit MMC 807 (consisting at least of two 7 bit — words) the following tests are.

- the test of the space between words
- the bit number in the command word
- the word comparing
- the observance of the minimal pause between the synchronization signals ("burst")

TABLE 5

RSVD	HIGH	LOW
Start bit logic level	0	1

The local keyboard inputs: LOC A, LOC B, LOC C, LOC D, LOC E.

By means of the command inputs: LOC A, LOC B, LOC C, LOC D, LOC E could be generated up to 31 local commands. The command realization is made by applying a parallel code on the five connexions.
In "stand-by" the LOC A, LOC B, LOC C, LOC D, LOC E inputs are pulled by "pull-up" transistors at V_{DD}.
Each local command represents a 5 bit-code in which at least one bit is "0" logic. Then all local command inputs are connected at a potential that corresponds to "1" logic signifies the absence of a local command.
When a local command exists, it has priority and appears at the end of the command on the IBUS. The 5 bit code for the local command is obtained by means of a diode matrix and which is presented in table 4. The signals on the IBUS, resulted after applying the local commands, are to be found at DATA, as long as the signal at the DLEN output is at LOW.

The internal bus outputs, DATA and DLEN.

All the signals reaching the internal bus are presented at the DATA output synchronized with the system clock, as long as the DLEN signal is LOW. A received command is repeated on the IBUS during the key pressing. The repeating period Tr is different according to the selected output mode and according to the emitter operating mode.
The values of Tr are specified in table 6.
MMN 806 has 3 command output modes according to the subsystem optiopns.
They are:

- singular command: e.g. the figure;
- repetitive command with a repeating rate of 2/sec: e.g. stop functions (in steps);
- repetitive command with a repeating rate of 8/sec: e.g. analogue functions.

A command on the IBUS has 7 bits: a bit for a command and 6 bits for data and it is synchronized with the clock system (fig. 4). The command is to be found inverted at the DATA output. Thus if the start bit is "0" logic in the command word, at the DATA output it will have the value "1" logic. The duration of a bit is two clock periods.
The command action especially influences the subsystems which are activated by this command. Because the subsystems are able to give commands to words the IBUS, the DLEN output should be checked before the IBUS output. When DLEN = LOW (the bus is busy) the command output is delayed with a duration: $32 \times Tc = 512\ \mu s$.

TABLE 6

Repeat rate	Single command	Repeated commands	
		2/sec	*8/sec*
Local command	n. 131	524	131
Remote command	n. 109	436	109

The command outputs of the analogue signals: VOLU, ANAL 2, ANAL 3, ANAL 4.

The analogue part contains 4 registers series of 6 bits for binary counting the analogue values, each one with the D/A converter of 63 steps. The analogue values are obtained by modifying the duty cicle at a signal with the frequence fc: 32 = 1, 95 kHz. These pulses are integrated with a filter circuit RC, thus resulting a continuous voltage proportional to the ratio HIGH/LOW.
Both the passing time from one step to another and the passing duration between "0" and "1" logic are different for the two operating modes and are specified in table 7.
When connecting the power supply, the circuit is in Stand-BY, at the analogue outputs, there are the reference analogue values (where the signals at the ANAL 2, ANAL 3, ANAL 4 outputs have the duty factor 31/64 and VOLU, 19/64, respectively) which corresponding to the main configuration selected by the "0" command in the table. 3.
The duty cycle values for the analogue command signals are modified by applying the corresponding commands specified in table 3.

TABLE 7

MODE	Passing time for one step	Passing duration betwenn „0" to „1" logic
LOCAL	131 ms	8.3 s
REMOTE	109 ms	6.9 s

Also, at the volume command output (VOLU) it could be established the mode MUTE (VOLU=LOW) for the following situations:

- for a short time, Ts, at the program switching, when the program memory is coupled (MODEP= HIGH). The value of Ts is 260 msec, for the local commands and 200 msec for the infrared remote control instructions;
- through the command 1 when the flip flop is set its output is the VOLU connection. The flip flop could be reset by means if the following commands:

— a new command 1 or a command 2 (OFF state) when the sound nominal value is maintained.
— command 40: "sound intensity growth" (the volume begins to grow from 0/64).
— a new command 0.

In stand by, the analogue memories cannot be changed. The output VOLU=LOW, irrespective of the memory values.

Input/output OFF.

The OFF connexion is the output of a flip flop and shows the circuit operating state. Thus:

- for OFF=HIGH, it is selected the mode STAND-BY.
- for OFF=LOW, it is selected the mode ON.

MMN 806 could also be brought in stand-by by connecting the power supply, V_{DD}.
The flip flop whose output is the OFF pin could be reset (brought in LOW) by one of the commands specified in table 3.

As an input, the OFF connexion allows the commanding of the flip flop in both states (LOW or HIGH). For this the duration of the setting signal should be longer, than two clock periods.

Program selecting outputs (RSVA, RSVB and RSVD).

RSVA is the output of a flip flop and it changes its state after each command of this type (command 3 in table 3).
RSVB generates a single positive pulse of 1 msec receiving the command (command 6).
A RSVC command generates a HIGH level at the RSVB output as long as the key is pressed.
The RSVD output operation depends on the MODEP output state. For MODEP=LOW, the RSVD output= LOW as long as the command 8 is received. The corresponding to the command should be pressed for minimum 100 msec.
If MODEP=HIGH, during the modification of the program memories through the commands 16—31, 36 and 37), a LOW pulse is generated at the RSVD output.
The MMN 806 behaviour at the RSVA, RSVB, RSVD is shown in timing diagram.

TABLE 8 — ON CONDITION

PIN	OUTPUT	INPUT	TEST
RSVA	$0=V_{OL}$	$1=V_{DD}$	MODE 1
RSVB	$0=V_{OL}$	$1=V_{DD}$	MODE 2

TABLE 9 — OFF CONDITION

PIN	OUTPUT	INPUT	TEST
RSVA	$1=V_{OH}$	$0=V_{SS}$	MODE 1
RSVB	$1=V_{OH}$	$0=V_{SS}$	MODE 2

RSVD could also be used as an input, by ground connection (V_{SS}), the circuit will be prepared to receive command words from distance with the start bit value "1" logic.
The RSVA and RSVB outputs, could operate as well as test inputs.
The test modes are switched to ON/OFF by connecting these inputs at antivalent signals through a small value resistor. In ordes to avoid the operating of test modes, the IOL output current of the RSVA and RSVB outputs should be smaller than 2.5 mA. In tables 8 and 9 it is presented the operating of the RSVA and RSVB connexions as test modes.

Program addressing memory outputs PRGA, PRGB, PRGC, PRGD and subsystem selecting input/output, MODEP.

PRGA, PRGB, PRGC, RPGD are the outputs of a program memory whose content is modified by the commands 16—31 (programs 1—16) or the commands 36 and 37 (incrementation/decrementation of the program number).
MODEP showns whether a subsystem is selected (MODEP=LOW) or not (MODEP=High). A subsystem will be selected by one of the commands 56÷63.

When a subsystem is selected or when MODEP= LOW (brought by an external command) the commands 16—31, 36 and 37 do not influence either the program memory contains or the VOLU and RSVD outputs. RSVD state is modified only by the command 8.
At the commands 2(OFF) or 4(ON) or after the power supply connection, MODEP=HIGH, PRGD could operate as an input; by its connection at the ground (V_{SS}) the program cycle decreases from 16 to 12.

Stand-by state.

MMN 806 is provided with an auto-reset circuit. After the circuit supply in the following 2,...,4 clock periods the stand-by mode is established.
This means that the circuit will have the following characteristics at the output:

- VOLU=LOW
- ANAL 2 ANAL 3, ANAL 4 presents the reference analogue values (with the dudy cycle 31/64)
- the program register selects the program 1
- the OFF output=HIGH
- the MUTE mode (command 1) is passive
- all intervalls outputs are in LOW, excepting RSVD

After the clock frequence connection for the circuit synchronization the supply voltage value should be and not smaller than $V_{DD} = 4.5$ V in order to make possible the operating of the auto-reset circuit.
In it is presented the application diagram for generating a delay start clock.

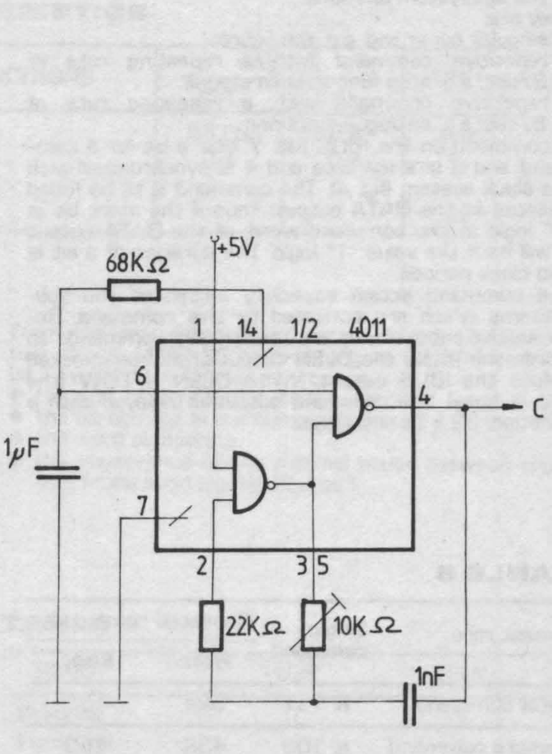
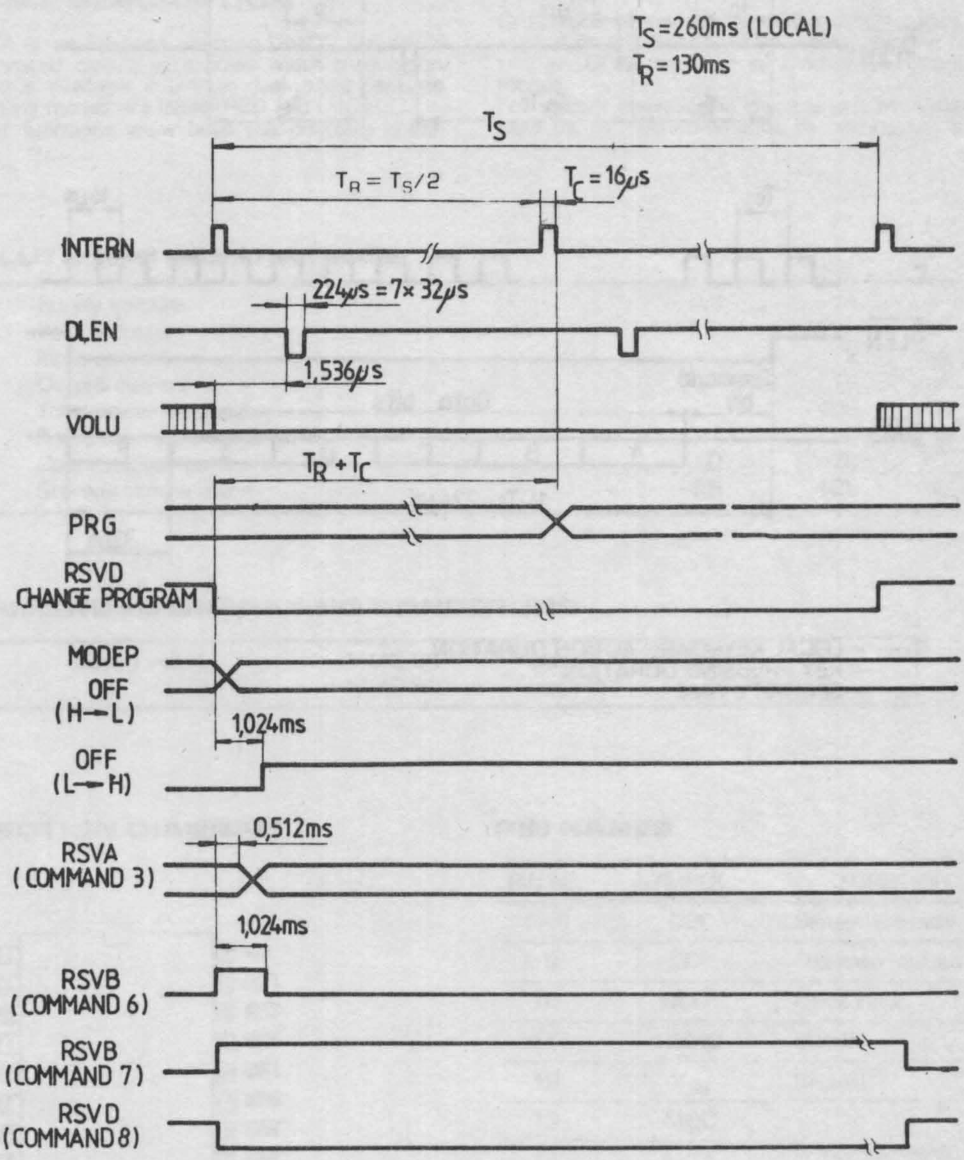


FIG.6 THE DELAYED CLOCK CIRCUIT

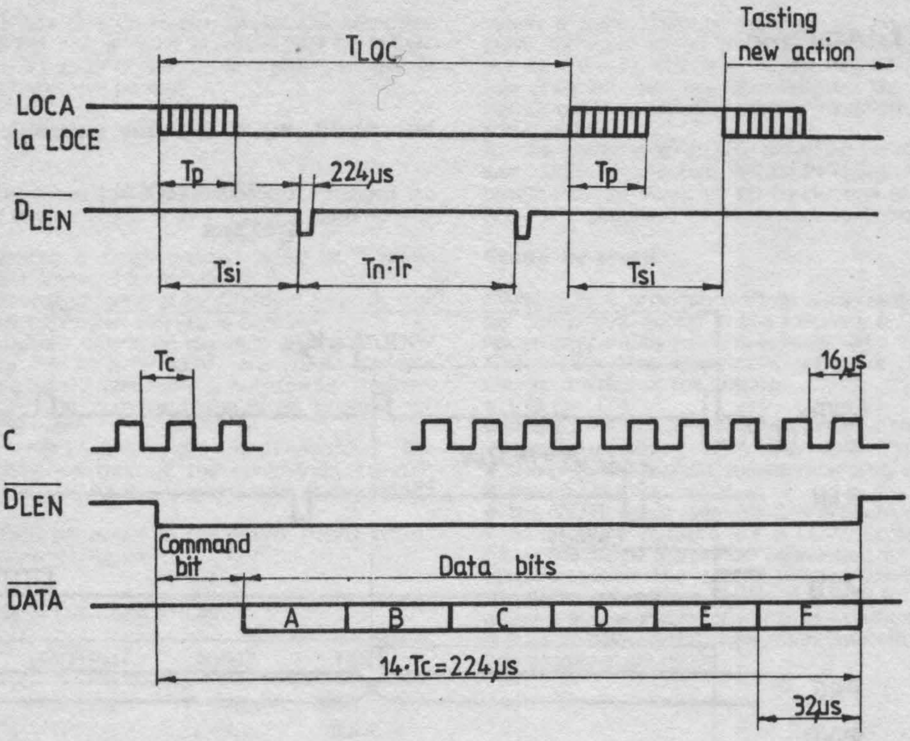
TIMING DIAGRAM



T_S MUTE MODE DURATION

T_R COMMAND REPEAT MINIMUM PERIOD

T_C CLOCK PERIOD



T_{LOC} = LOCAL KEYBOARD ACTION DURATION
T_P = KEY PRESSING DURATION
T_{SI} = SECURITY TIME

INFRARED EMITTING CIRCUIT FOR REMOTE CONTROL

GENERAL DESCRIPTION

MMC 807 is an infrared emitting CMOS polysilicon gate integrated circuit with pulse width modulation. The circuit is available in 24 pin dual-in-line package. The operating modes are INFRARED and LOCAL. The circuit functions allow both the emitting in LOCAL mode of the corresponding ASCII codes, parallel applied on the SENØ, SEN7 inputs and the transmitting in LOCAL mode or infrared of 64 different commands.
For special applications there is the possibility to extend up to 128 commands by setting the start bit.

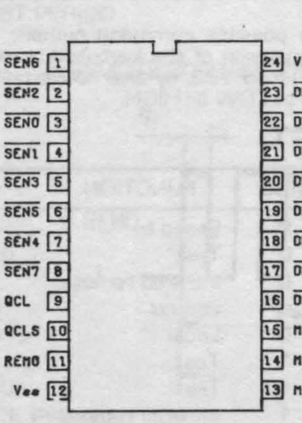
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage:	−0.3	...	11	V
V_I	Input voltage	−0.3	...	$+V_{DD}$	V
I_i	Input current			2	mA
Io	Output current			10	mA
P_{max}	Total power dissipation			400	mW
P_o	Dissipation per output buffer			50	mW
T_A	Operating temperature	0	...	70	°C
T_{stg}	Storage temperature	−55	...	125	°C

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	MMC 807.1	class 1	4.3...11	V
		MMC 807	class 2	7...11	V

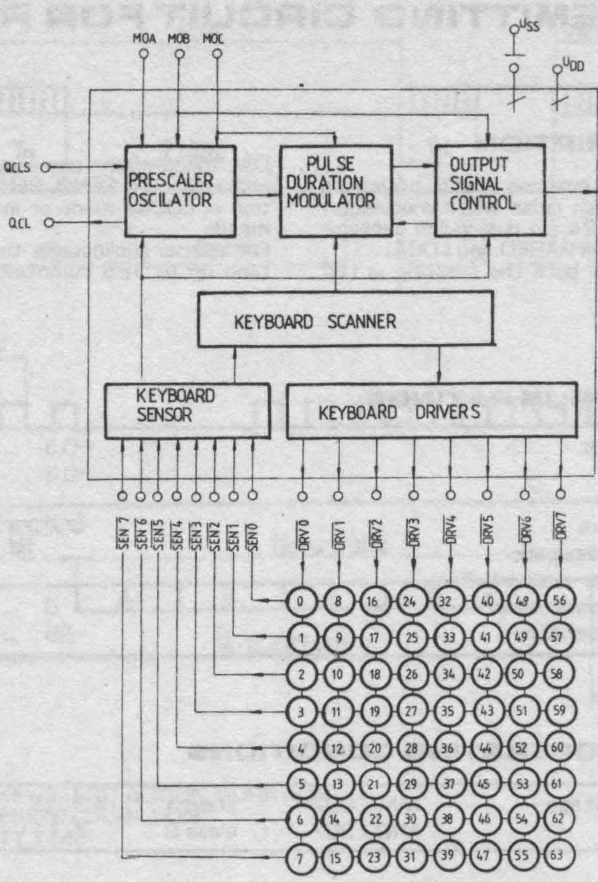
CONNECTION DIAGRAM



PIN NAMES

PIN No.	SYMBOL	FUNCTION
1–8	QCL	Sensorial inputs
9	QCL	Oscillator output
10	QCLS	Clock input
11	REMO	Output
12	V_{SS}	Ground
13	MOC	Selecting mode control inputs
14	MOA	
15	MOB	
16–23	DRV0—DRV7	OPEN-DRAIN outputs
24	V_{DD}	Power pupply

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

MMC 807 is an infrared emitting remote control circuit designed to generate 128 commands for receiver control.

In the receiver decoding and demodulation are performed by MMN 806.

MMC 807 could be operated in LOCAL mode, where the RENO output is directly connected at the MMN 806 receiver input and at the QCLS pin is coupled an external frequence, f = 62.5 kHz, common with that of the receiver. In this configuration the two circuits are synchronously operating.

Besides there is the possibility to send in LOCAL mode the ASCII combinations parallel applied at the SENØ—SEN7 inputs.

For selecting the operating mode the circuit has three command inputs: MOA, MOB, MOC:

— by the states of the MOA and MOB connections the operating mode is selected as follows:
  — for MOA=HIGH (and MOB=HIGH) the LOCAL mode is selected
  — for MOA=LOW (and MOB=High) the infrared remote control mode is selected
  — for MOA=LOW (and MOB=LOW; MOC=LOW) the circuit is in stand by mode
  — for MOA=don't care and MOB=LOW is selected one of the modes of test used by the manufacturer. This case has no interest for the users.

The logic level applied at the MOC input is the logic state of the command bit noted 8 (start bit).

MOC=LOW: S="0" logic
MOC=HIGH: S="1" logic

Using of the additional MOC pin offers two advantages to the circuit:

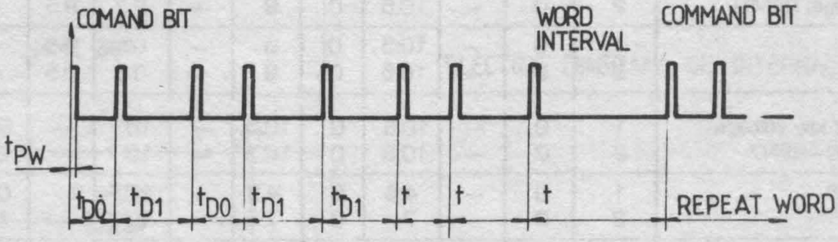
1. Extention of the possible command number from 64 (which is the dimension of the keyboard matrix: 8 rows x 8 columns) up to 128, by alternative connecting of the MOC pin to LOW or HIGH.

MODE SELECT

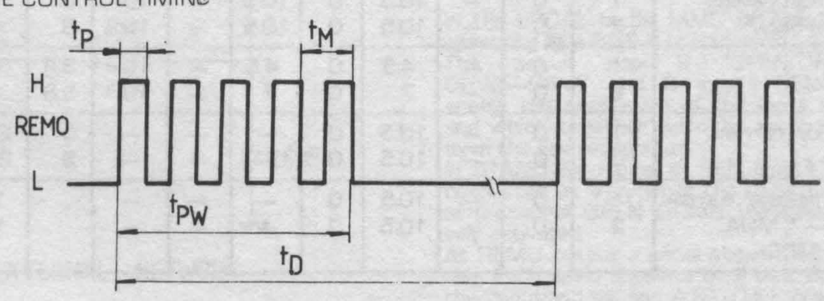
MOA	MOB	MOC	FUNCTION	S
0	0	0	Stand-by	—
1	0	0	Test	0/1
0	1	0	Infrared remote control	0
1	1	0	Local	0
1	0	1	Test	1
0	0	1	Test	0/1
0	1	1	Infrared remote control	1
1	1	1	Local	1

2. Possible control of 2 receiver systems from the same emitter.
The two receivers will be selected by the state of the start bit in the command word.
After pushing and identifying the key by scanning all command outputs: DRVØ—DRV7, the key analyser generates a binary word.
The codification of the binary code elements is made by combining the LOW and HIGH logic states with two different periods of time, noted tDØ and tD1. Both periods are preceded by a (pulse) "burst" which enables the bit separation in the command word and the operating mode identification at reception. At emission the encoded word will be formed of a succesion of "bursts", separated by periods of time tDØ or tD1.
The number and the periods of the pulses in the burst are different at the local transmission mode from the infrared remote control mode.
In figures bellow is presented the "burst" structure specifying the most important values (period, pulse number, logic state codes). Each seven bit-word is followed by a period which represents the code of the space between words, noted tDW.
At the disconnection of a key for a short time: t<19$\times$tUD, followed by the immediate pushing of the same key or of another one in the output signal instead of the simple space between words is inserted the double space between words. Thus the receiver will be able to differentiate between a long pressing of the emission key and a repeated pressing. The four coding periods: tDØ, tD1, tDW and tDS behave both at the infrared operation and at the local mode within the rations: 5:7:14:19 in comparison with the time tUD.

REMO PIN OUTPUT SIGNAL

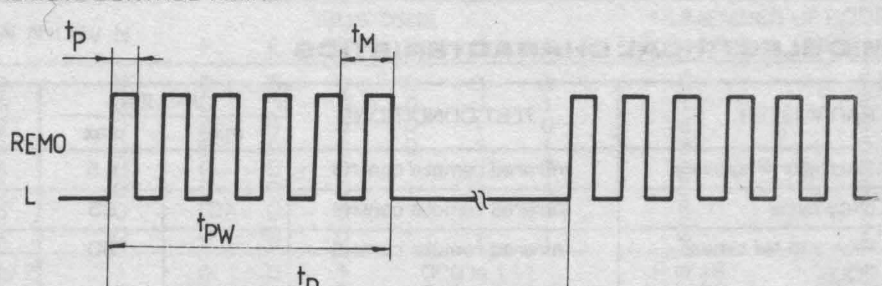


LOCAL REMOTE CONTROL TIMING



CLOCK PERIOD	$t_C = 16\ \mu s$	BURST DURATION	$t_{PW} = 4{,}5\ t_M$
TIME UNIT	$t_{UD} = 64\ t_C$	„LOW„ WIDTH	$t_{DO} = 5\ t_{UD}$
PULSE WIDTH	$t_P = t_C$	„HIGH" WIDTH	$t_{D1} = 7\ t_{UD}$
BURST PERIOD	$t_M = 2\ t_C$	SIMPLE WORDS INTERVAL	$t_{DW} = 14\ t_{UD}$
		DOUBLE WORDS INTERVAL	$t_{DS} = 19\ t_{UD}$

INFRARED REMOTE CONTROL TIMING



CLOCK PERIOD	$t_Q = 250$ ns	BURST DURATION	$t_{PW} = 5{,}5\ t_M$
TIME UNIT	$t_{UD} = 4096\ t_Q$	„LOW„ WIDTH	$t_{DO} = 5\ t_{UD}$
PULSE WIDTH	$t_P = 56\ t_Q$	„HIGH" WIDTH	$t_{D1} = 7\ t_{UD}$
BURST PERIOD	$t_M = 112\ t_Q$	SIMPLE WORDS INTERVAL	$t_{DW} = 14\ t_{UD}$
		DOUBLE WORDS INTERVAL	$t_{DS} = 19\ t_{UD}$

STATIC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

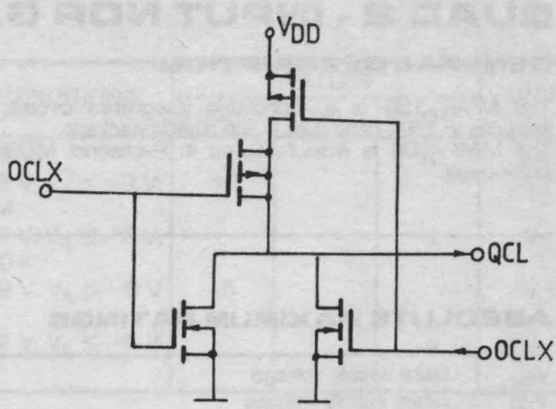
	PARAMETER	CLASS	TEST CONDITIONS V_{SS} (V)	V_I (V)	V_{DD} (V)	V_{IL} (V)	V_{IH} (V)	V_O (V)	I_O (mA)	VALUES min.	max.	UNIT
I_{DDo}	Quiescent current	1	0	—	10.5	0	10.5	—	—		10	μA
		2	0	—	10.5	0	10.5	—	—		10	μA
V_{OL}	Output low voltage: QCL, REMO	1	0	—	4.5	0	4.5	—	1.0		1	V
		2	0	—	7	0	7	—	0.8		1	V
	DRV0—DRV7	1	0	—	4.5	0	4.5	—	0.8		1	V
		2	0	—	7	0	7	—	0.6		1	V
V_{OH}	Output high voltage: REMO	1	0	—	10.5	0	8	—	2.7	9.5	—	V
		2	0	—	10.5	0	8	—	2.7	9.5	—	V
	QCL	1	0	—	10.5	0	8	—	0.6	9.5	—	V
		2	0	—	10.5	0	8	—	0.6	9.5	—	V
V_{IL}	Input low voltage: SEN0—SEN7	1	0	—	10.5	0	10.5	—	10^{-3}	—	2.1	V
		2	0	—	10.5	0	10.5	—	10^{-3}	—	2.1	V
	QCLS	1	0	—	4.5	0	4.5	—	10^{-3}	—	0.9	V
		2	0	—	7	0	7	—	10^{-3}	—	1.4	V
V_{IH}	Input high voltage: SEN0—SEN7	1	0	—	10.5	0	10.5	—	10^{-3}	8	—	V
		2	0	—	10.5	0	10.5	—	10^{-3}	8	—	V
	QCLS	1	0	—	4.5	0	4.5	—	10^{-3}	3.6	—	V
		2	0	—	7	0	7	—	10^{-3}	5.6	—	V
I_{IL}	Input low current SEN0—7	1	0	—	10.5	0	—	—	—	5	250	μA
		2	0	—	10.5	0	—	—	—	5	250	μA
I_{IR}	Input leakage current: SEN0—7; MOA; MOB; MOC	1	0	—	10.5	0	—	—	—		1	μA
		2	0	—	10.5	0	—	—	—		1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

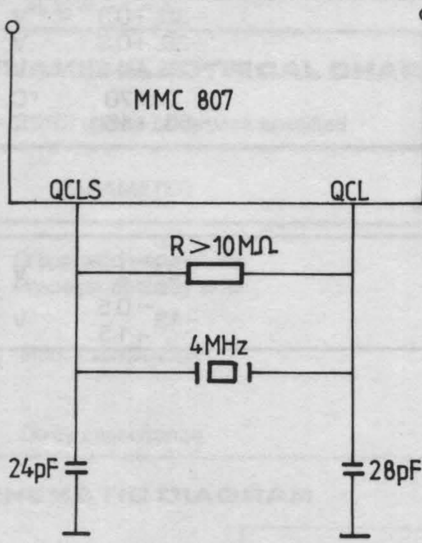
	PARAMETER	TEST CONDITIONS	VALUES min.	max.	UNIT
FQLS	Oscillator frequency	Infrared remote control	—	4.5	MHz
	Duty cycle	Infrared remote control	45	55	%
t_r, t_f	Rise and fall timeat FQLS	Infrared remote control		50	us
	Duty cycle	Local		60	%
t_r	Rise time	Local		50	us
t_f	Fall time	Local		70	us

FUNCTIONAL ELECTRICAL CHARACTERISTICS

Depending on the selected operating mode, the MMC 807 synchronizing frequency is differently generated and has other values.
Thus in the infrared mode the clock frequency is 4 MHz obtained by a quartz connected between the QCLS and QCL pins.



ELECTRIC DIAGRAM OF INTERNAL OSCILATOR



EXTERNAL NETWORK OF EMITTER'S OSCILLATOR

In the LOCAL mode, MMC 807 and MMN 806 are operating at a 62,5 kHz frequency.
The circuit has 8 "OPEN-DRAIN" outputs: DRVØ—DRV7 and 8 inputs SENØ—SEN7 which enable the realisation of the input matrix (8x8=64) and which together with the keyboard decoder perform the key recognition.
In STAND-BY mode, all SEN inputs are HIGH, being connected at V_{DD}, while the DRV outputs consisting of n-channel OPEN DRAIN transistors are succesively activated.
At REMO output a serial sequence of words is obtained. Each word consists of 7 bits: S,A,B,C,D,E,F. S is the command bit and A,B,C,D,E,F represent the 6 bit command of the internal bus (IBUS).

CODIFICATION KEY NUMBER TO BUS CODE

SEN .N	IDRV .N	IBUS CODE F	E	D	C	B	A	NUMEMBER OF CODE MOC = LOW	MOC = HIGH
0	0	0	0	0	0	0	0	0	64
1	0	0	0	0	0	0	1	1	65
2	0	0	0	0	0	1	0	2	66
3	0	0	0	0	0	1	1	3	67
4	0	0	0	0	1	0	0	4	68
5	0	0	0	0	1	0	1	5	69
6	0	0	0	0	1	1	0	6	70
7	0	0	0	0	1	1	1	7	71
0 la 7	1	0	0	1	000 la 111			8 la 15	72 la 79
0 la 7	2	0	1	0	000 la 111			16 la 23	80 la 87
0 la 7	3	0	1	1	000 la 111			24 la 31	88 la 95
0 la 7	4	1	0	0	000 la 111			32 la 39	96 la 103
0 la 7	5	1	0	1	000 la 111			40 la 47	104 la 111
0 la 7	6	1	1	0	000 la 111			48 la 55	112 la 119
0 la 7	7	1	1	1	000 la 111			56 la 63	120 la 127

QUAD 2 - INPUT NOR GATE

GENERAL DESCRIPTION

The MMP 106 is a monolithic integrated circuit, available in 16 — lead dual in line plastic package.
The MMP 106 is manufactured in P-channel MOS technology.

FEATURES

- High input resistance
- Inputs fully protected
- Two supply voltage

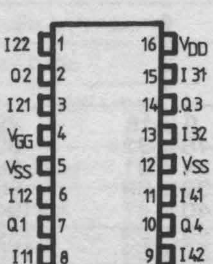
ABSOLUTE MAXIMUM RATINGS

V_{GG}	Gate supply voltage	−30...+0.3	V
V_{DD}	Drain supply voltage	−30...+0.3	V
V_I	Input voltage	−25...+0.3	V
T_A	Operating ambient temperature	0...+70	°C
T_S	Storage temperature	−55...+150	°C

RECOMMENDED OPERATING CONDITIONS

V_{GG}	Gate supply voltage	-27^{-1}_{+2}	V
V_{DD}	Drain supply voltage	$-13^{-0.5}_{+1.5}$	V

PIN CONNECTIONS



TRUTH TABLE

I_{n1}	I_{n2}	O_n
H	H	L
H	L	H
L	H	H
L	L	H

n = 1, 2, 3, 4

STATIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$) unless otherwise specified

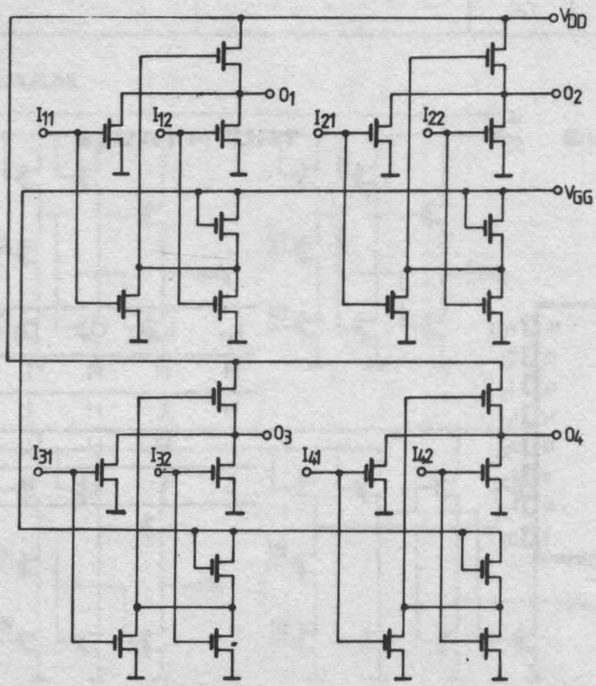
PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
I_I Input current	$V_I = -25$ V			10	μA
V_{OL} Low level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 1$ M	10			V
V_{OH} High level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 100$ K			1	V
V_{OL} Low level output voltage at $I_O = +1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V	5			V
V_{OH} High level output voltage at $I_O = -1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V			4	V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$) unless otherwise specified

PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PHL} Propagation delay time			320		ns
t_{PHL} Propagation delay time			120		ns
C_{IN} Input capacitance	$V_{GG} = V_{DD} = 0$ V; $V_I \geq 0.2$ V; f = 0.5...2 MHz			1	pF
C_{st} Stray capacitance		30			pF

SCHEMATIC DIAGRAM



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QUAD 2 - INPUT AND (NAND) GATE

GENERAL DESCRIPTION

The MMP 107 is a monolithic integrated circuit, available in 16 — lead dual in line plastic package.
The MMP 107 is manufactured in P-channel MOS technology.

FEATURES

- High input resistance
- Inputs fully protected
- Two supply voltages

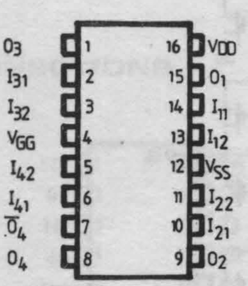
ABSOLUTE MAXIMUM RATINGS

V_{GG}	Gate supply voltage	−31...+0.3	V
V_{DD}	Drain supply voltage	−31...+0.3	V
V_I	Input voltage	−25...+0.3	V
T_A	Operating ambient temperature	0...+70	°C
T_{stg}	orage temperature	−55...+150	°C

RECOMMENDED OPERATING CONDITIONS

V_{GG}	Gate supply voltage	-27^{-1}_{+2}	V
V_{DD}	Drain supply voltage	$-13^{-0.5}_{+1.5}$	V

PIN CONNECTIONS



TRUTH TABLE

I_{n1}	I_{n2}	O_n	$\overline{O}_4$
H	H	H	L
H	L	H	L
L	H	H	L
L	L	L	H

n = 1, 2, 3, 4

STATIC ELECTRICAL CHARACTERISTICS

(T_A = 25° C) unless otherwise specified

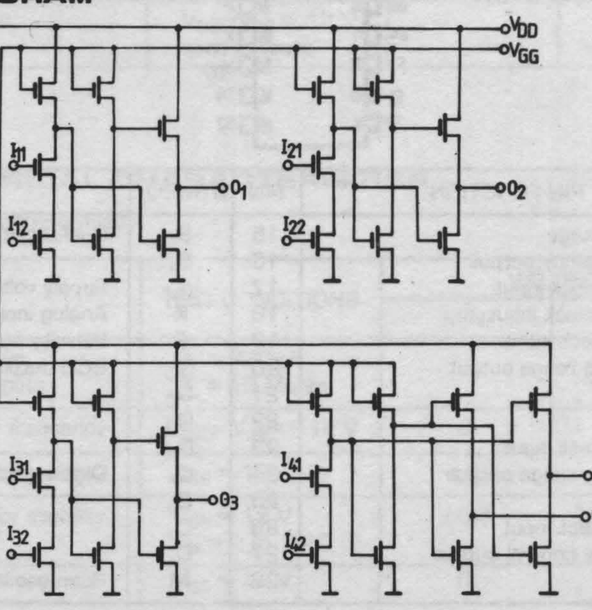
	PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
I_I	Input current	$V_I = -25$ V			10	μA
V_{OL}	Low level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 1$ MΩ	10			V
V_{OH}	High level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 100$ KΩ			1	V
V_{OL}	Low level output voltage at $I_O = +1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V	5			V
V_{OH}	High level output voltage at $I_O = -1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V			4	V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C) unless otherwise specified

	PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}	Propagation delay time for 01...03, $\overline{04}$			320		ns
t_{PLH}	Propagation delay time for 04			150		ns
t_{PHL}	Propagation delay time			200		ns
C_{IN}	Input capacitance	$V_{GG} = V_{DD} = 0$ V; $V_I \geq 0.2$ V; f = 0.5...2 MHz			6	pF
C_{st}	Stray capacitance for 01...03, $\overline{04}$		30			pF
C_{st}	Stray capacitance 04		20			pF

SCHEMATIC DIAGRAM



DIGITAL MULTIMETER LOGIC

GENERAL DESCRIPTION

MMP 190 is a digital multimeter logic integrated circuit fabricated in PMOS enhancement-depletion aluminium gate technology. The circuit consists of 2 internal oscilators (one for multiplexing, one for counting), a 4 decades BCD counter, an output multiplexer which can drive a LED or LCD 3 3/4 digit display and an autoranging and dual-slope A/D conversion control logic.
MMP 190 is supplied in 28-lead dual-in-line plastic packages.

FEATURES

- 3 3/4 digit digital multimeter logic (max. 599.9)
- autoranging
- multiplexed BCD output
- dual-slope integration
- overrange indicated (blinking)
- low-power dissipation
- CMOS compatibility

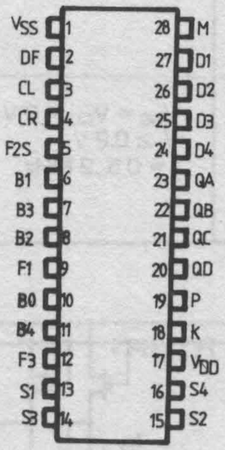
APPLICATIONS

- digital multimeter
- decade counter

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-20 to +0.3	V
V_I	Voltage between any pin and ground	-20 to +0.3	V
I_F	Input current (V_I = 0.3 V; V_{SS} = 0 V)	1	mA
T_A	Operating ambient temperature	0 to +70	°C
T_{stg}	Storage temperature	-55 to +125	°C

PIN CONNECTIONS



PIN	SYMBOL	PIN FUNCTION	PIN	SYMBOL	PIN FUNCTION
1	V_{SS}	Supply voltage	15	S_2	Dual-slope control output
2	DF	LCD frequency output	16	S_4	"
3	CL	External clock input	17	V_{DD}	Supply voltage
4	CR	Counting clock input	18	K	Analog input
5	F_{2S}	Range select input	19	P	Polarity output
6	B_1	Measuring range output	20	Q_D	BCD output
7	B_3	"	21	Q_C	"
8	B_2	"	22	Q_B	"
9	F_1	Range select input	23	Q_A	"
10	B_0	Measuring range output	24	D_4	Digit selection output
11	B_4	"	25	D_3	"
12	F_3	Range select input	26	D_2	"
13	S_1	Dual-slope control output	27	D_1	"
14	S_3	"	28	M	Scan oscilator input

STATIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified)

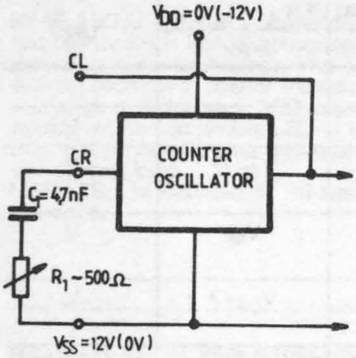
	PARAMETER	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
V_{DD}	Supply voltage	reference	0	0	V
V_{SS}	Supply voltage	V_{DD} = 0 V	8	14	V
V_{IL}	K input low voltage	V_{DD} = 0 V f_N = 30 kHz	0	V_{SS}–7	V
V_{IH}	K input high voltage	V_{DD} = 0 V f_N = 30 kHz	V_{SS}–2	V_{SS}	V
V_{IL}	Input low voltage (except K input)	V_{DD} = 0 V f_N = 30 kHz	0	V_{SS}–7	V
V_{IH}	Input high voltage (except K input)	V_{DD} = 0 V f_N = 30 kHz	V_{SS}–0.5	V_{SS}	V
V_{OL}	Output low voltage (Q_A, Q_B, Q_C, Q_D, D_1, D_2, D_3, D_4, P outputs)	I_O = 25 μA	0	1	V
V_{OH}	Output high voltage (Q_A, Q_B, Q_C, Q_D, D_1, D_2, D_3, D_4, P outputs)	I_O = –200 μA	V_{SS}–1	V_{SS}	V
V_{OL}	Output low voltage (B_0, B_1, B_2, B_3, B_4, S_1, S_2, S_3, S_4 outputs)	I_O = 50μA	0	1	V
V_{OH}	Output high voltage (B_0, B_1, B_2, B_3, B_4, S_1, S_2, S_3, S_4 outputs)	I_O = –200 μA	V_{SS}–1	V_{SS}	V
V_{OL}	DF output low voltage	I_O = 50 μA	0	1	V
V_{OH}	DF output high voltage	I_O = –50 μA	V_{SS}–1	V_{SS}	V
P_d	Power dissipation	V_{DD}–V_{SS} = 12 V open outputs		70	mW

DYNAMIC ELECTRICAL CHARACTERISTICS

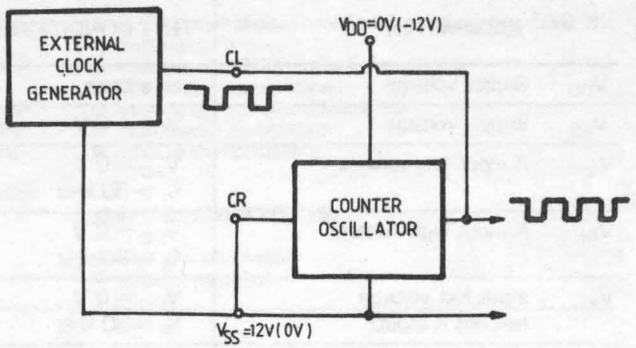
(T_A = 25°C, unless otherwise specified)

	PARAMETER	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
t_d	Delay time between K input and S outputs	C_L = 200 pF R_L = 10 Mohm		4	μs
f_N	Counter oscilator frequency	V_{DD}–V_{SS}= –12 V	0	100	kHz
$F_{N(V)}$	Counting frequency stability	V_{SS} = 12±1 V	±3		%/V
$F_{N(T)}$	Counting frequency stability	V_{SS} = 12 V T_O = 0 to 70°C	±0.8		%/°C
f_M	Multiplexing frequency	V_{SS} = 12 V	0	800	Hz

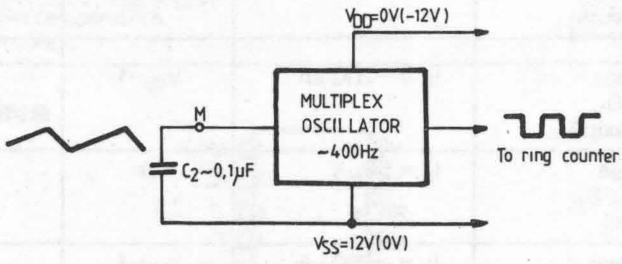
MODES OF OPERATION

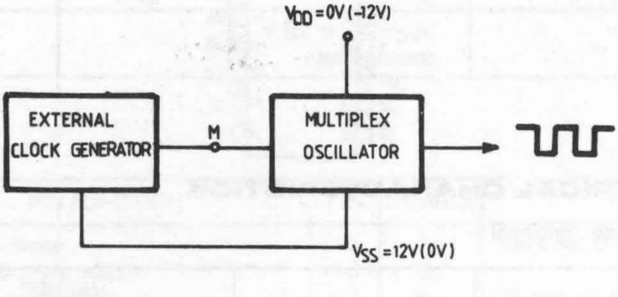


* Input CL open



* Input CR connected to





* Only for testing purposes and R_I 0

FUNCTIONAL DESCRIPTION

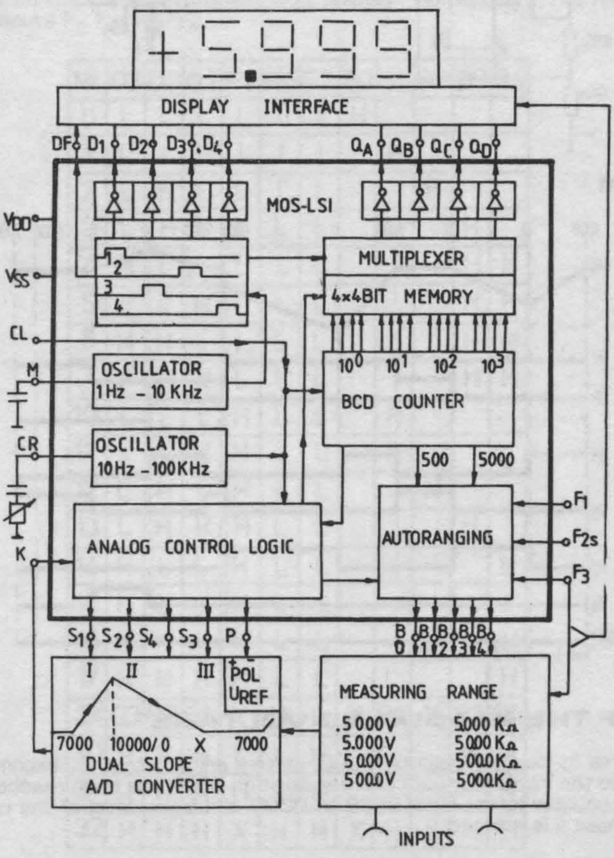
GENERAL

The circuit comprises the logic functions for a digital multimeter, on the basis of dual-slope method, with automatic range switching. By means of four measuring-range outputs, small units with 3 3/4 digits and four measuring ranges can be realized without additional external components for the range selection. By switching the logic range, up to eight different measuring ranges can be switched automatically; however, decoding of these ranges must be done externally.
The maximum display is 6000. 6000 steps mean a relatively small analog circuit requirement, however, that permit the measuring of voltages between 100 μA and 600 V in four measuring ranges. When the highest measuring range is exceeded, the value 6000 is displayed. Through an additional blinking circuit, which does not require an additional connection pin, the user is made aware of the measuring range being exceeded.

FUNCTION

The block diagram shows a simple unit with four automatically selected measuring ranges. The external analog portion consists of only the analog amplifiers, reference voltage source, and the analog switches for the measuring phase and range switching.

BLOCK DIAGRAM

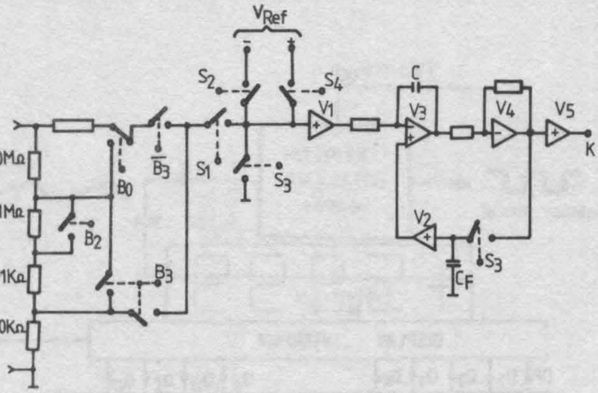


The sequence control and generation of the value measured is done by the MMP 190. The main portion of the circuit is made up of a four decade BCD counter which is driven by a counting oscillator contained on the chip, together with an externally connected RC-circuit. The counting oscillator may be replaced by connecting a clock generator. At particular periods of timing, the contents of the counter is transferred into the 4 x 4-bit memory by means of a strobe pulse derived from the K-input.
The information contained in the memory is transfered by means of a multiplexer in a bit-parallel mode to outputs Q_A through Q_D, whereby outputs D_1 through D_4 indicate the just transferred decimal place ($Q_A \triangleq$ LSB, $Q_D \triangleq$ MSB; $D_1 \triangleq$ units digit, $D_4 \triangleq$ thousands digit, active condition = high level). To ensure reliable driving of the memories in the display interface, e.g. liquid crystal display, the correct BCD-information is maintained at the Q outputs until after the end of the active condition of the D-outputs. The indication of the decimal position occcurs in the sequence 1-3-2-4, to avoid flickering when the display units are driven directly.
For the generation of scan-frequency for the multiplexer a second oscillator has been provided on the MMP 190. Replacement by an external clock generator is possible but should be used only for testing purposes. The display frequency DF of about 50 Hz required by liquid crystal displays is also derived from the multiplex oscillator.

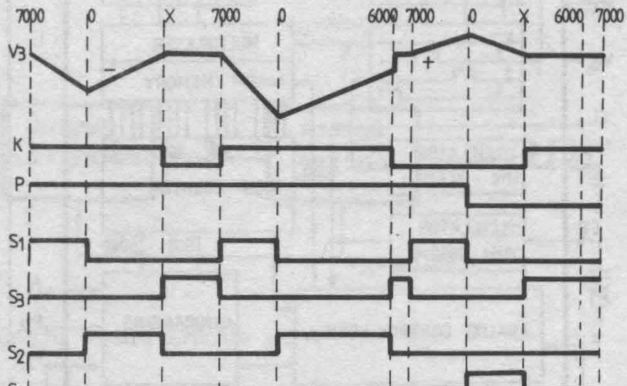
MEASURING-SEQUENCE

The measuring sequence is also controlled by the BCD-counter, via measuring-phase outputs S_1 through S_4 (compare timing diagram and principle circuit diagram).

EXTERNAL ANALOG CIRCUIT



TIMING DIAGRAM



PHASE I, INTEGRATION OF THE MEASURING VOLTAGE

The measuring cycle starts at counter position 7000; at this point output S_1 becomes high, whereby the input voltage is switched to the integrator until counter position 0000 has been reached.
At the moment when the counter jumps from 9999 to 0000, the signal level of the comparator (input k) is stored. At this moment phase II is started.

PHASE II, INTEGRATION OF REFERENCE VOLTAGE

Depending on the condition of the comparator, only S_2 or S_4 is activated whereby the reference voltage is switched to the integrator with a polarity opposite to the previously applied input voltage. With this reference voltage the integrator is reduced until the sensitivity threshold of the comparator has been reached and the signal condition at the input K changes. This change of signal activates S_3. The number of counting pulses between counter position 0000 and X is proportional to the measuring voltage. Through the low-high transition of S_3 the counter contents is loaded into the display memory; at this point of time phase III is started.

PHASE III, ZERO REGULATION

In this process the input of the AD-converter is set to zero and the resulting error voltage is stored in capacitor C_F. An error voltage is compensated by a feedback loop. The duration of phase I is determined by the counter frequency and the fixed number of 3000 counting steps. For a 30 KHz counting frequency, phase I lasts exactly 100 ms. The longer the integration time, the better the suppression of noise voltages superimposed on the measuring signal. If the duration of the noise voltage period is contained in the integration time as an even number, this noise is suppressed completely. As noise voltages can be expected to occur especially at line frequency, 100 ms integration time constitute a favourable compromise between integration time and noise voltage suppression. The duration of phase II is determined by the level of the measuring voltage. If the measuring voltage is too large, the integrator cannot be discharged during the 6000 counting steps available as a maximum; consequently, at step 6000 phase III is initiated. Hence the integrator will have assumed the correct starting position at the begining of phase I which follows. For excessive measuring voltages the display is therefore 6000. In order to bring the incorrectness of this display to the user's attention, the pseudo-decade HHHH is made active at the outputs, synchronously to signal S_1; thereby a blinking effect of approx. 3 Hz is obtained.

AUTOMATIC RANGE SWITCHING

The measuring range is changed whenever the measuring result has been $\geqslant 5500$ or < 500. For $n \geqslant 5500$ the range counter (3 bit up/down counter) is stepped by one count, for $n < 500$ stepped down by one, whereby the counter is blocked on the lowest or highest digit position, respectively. The range selection can be controlled through control inputs F_1, F_{2S} and F_3.

TRUTH TABLE

Nr	Q3	Q2	Q1	F1	F2S	F3	B0	B1	B2	B3	B4
0	L	L	L	L	L	L	H				
1	L	L	H	L	L	L		H			
2	L	H	L	L	L	L			H		
3	L	H	H	L	L	L				H	
4	H	L	L	L	L	L				H	H
5	H	L	H	L	L	L				H	H
6	H	H	L	L	L	L				H	H
7	H	H	H	L	L	L				H	H
10	L	L	L	H	L	L		H			
11	L	L	H	H	L	L		H			
12	L	H	L	H	L	L			H		
13	L	H	H	H	L	L				H	
14	H	L	L	H	L	L					H
15	H	L	H	H	L	L					H
16	H	H	L	H	L	L					H
17	H	H	H	H	L	L					H
2X	Q3	Q2	Q1	X	H	L	X	Q1	X	Q2	Q3
30	H	H	H	L	L	H				H	H
31	H	H	H	H	L	H					H
32	H	H	H	X	H	H	X	H	X	H	H

When the control inputs F_1, F_{2S} and F_3 are in a low condition, the counter can move within the lower 5 positions up or down. Should it be in a higher position, it can step only downward until the "free zone" has been reached; the decoder produces correct values also for counter positions outsside the "free zone" so that the system adjusts itself.
By an H-signal at input F_1 the correlation between the counter position and decoder output can be changed. Thereby it is made possible to perform range setting for the voltage and resistance ranges and the control of the decimal point in a simple unit with four measuring ranges without external decoding. Input F_3 is used to set the counter to the highest level. The highest measuring range is activated and maintained as long as F_2 is kept at a high level. For example, thereby the range 500.0V is activated, which is an advantage for quick overview-measurements.
A high level at input F_{2S} has the effect that the outputs of the range counter are directly transferred to the outputs 8 different ranges are then available which must be decoded by external means. In the case of F_{2S} = H, the "frea zone" of the counter is expanded to the full counting range; the prevention of "running wild" is maintained.

THE TRUTH TABLE FOR SETTING THE MEASURING RANGES SHOULD BE UNDERSTOOD AS FOLLOWS:

The range outputs B_0...B_4 are intended to directly drive the five possible decimal places of a 4 decade display. Simple units with 4 measuring ranges have been taken into consideration. For example, in the case of voltages the measuring ranges with F_1 = low are:

B_0	.5000 V
B_1	5.000 V
B_2	50.00 V
B_3	500.0 V

The total measuring range therefore comprises 0.1 mV through 599.9 V. For resistance measuring, however, F_1 must be high:

B_1	5.000 kohm
B_2	50.00 kohm
B_3	500.0 kohm
B_4	5000. kohm

The total measuring therefore comprises 1 ohm through 5.999 Mohm. Hence, using control input F_1, a choice of one of the two groups is basically possible.
The range outputs are also intended to directly drive the appropriate four selection relays without additional logic gating. When the automatic range selection (e.g. after turn-on) has not yet found the correct range, some measuring range expected to be shown anyway. This side-condition is considered in the truth table of vectors 0...17.
It should be noted, however, that Q_1, Q_2, and Q_3 in the truth table are internal outputs of the built-in up-down counter. It is also possible to select one of 5 measuring ranges automatically. To do this, the 4th and the 5th measuring ranges are separated by external gating at F_1 = low (whereby $MB_4 = B_3$; $\overline{B}_4$ and $MB_5 = B_4$). MB_4 is measuring range 4, MB_5 is measuring range 5.
F_{2S} = high causes an extension of all eight possible measuring ranges. The range selected appears at outputs B_1 ($=Q_1$), B_3 ($=Q_2$), and B_4 ($=Q_3$) dual-coded. Hence, vectors 20...27 of the truth table are fixed.

PROGRAMMABLE CIRCUIT FOR CONTROL OF THYRISTORS, TRIACS OR TRANSISTORS

GENERAL DESCRIPTION

MMP 708 is a PMOS programmable integrated circuit for control of thyristors, triacs or transistors. All inputs are protected with clamping diodes.
The circuit can be used for phase or burst control with fixed reference. The reference voltage is internally generated and has the value:

$$V_{ref} = -3 \div -5\ \text{V}$$

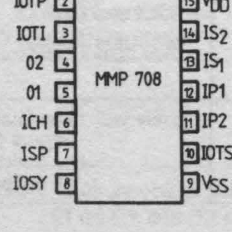
For phase control, the RC network is connected to IOTSY pin and generates a voltage slope that leads to a delay.
This delay is detected by connecting I_v pin to IOTSY pin. The adjustment of the firing angle is made by modifying the RC value. For a negative feedback, the R resistor could be replaced by a transistor in a commanded current generator configuration.
The PO10, PO11, P10 programs are designed to avoid the DC components in the network as a result of thyristors or triacs switching. Thus is used the burst control and is possible only the command of an even number of semiperiods.
In the PO11 and P10 programs, at O1 and O2 outputs are generated signals for control of triacs, making possible the simultaneous command of two independent loads.
In the PO11 program both the commands at O1 and O2 are given for an even number of semiperiods. At O1 the commands can start at L → H transition at IS_1, if IS_2 = L (see table 1).
In the P10 program at the O1 output are generated signals for the phase control of a triac. At the O2 output are given commands for an even number of semiperiods, under the same conditions as in the PO11 program.
In the P11 program the channel selection is made by pulse command from a ring counter. The IS_1 and IS_2 pins are connected to the Q and Q outputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	−31...+.3	V	1)
V_I	Input voltage	−25...+.3	V	1)
V_{IM}	Peak input voltage	−31	V	1)=1:10 t_{pMAX}=10μs
P_{tot}	Total power dissipation	.6	W	T_A=25+45°C
C_L	Load capacitance	10	nF	at 01,02 2)
I_O	Output current	5	mA	at 01,02
I_O	Peak output current	20	mA	at 01,02 3)b=1:4
		80	mA	at 01,02 3)b=1:100
T_A	Operating temperature	0..70	°C	
T_{stg}	Storage temperature	−55...+125	°C	

NOTES: 1) All voltage values are referred to V_{SS} pin voltage
2) Maximum load capacitance is:
a) CL_1=100 nF+10% at IOSY, IOTSY pins
b) CL_2= 25 nF+10% at IOTP, IOTI pins
3) When supplied from mains with frequency f=50+60 Hz

CONNECTION DIAGRAM



PIN NAMES

IIO = input for null current signal
IOTP = input-output for setting the pause time at the firing pulses
IOTI = input-output for setting the pulse width of the firing pulse
O2 = output for the control signal 2
O1 = output for the control signal 1
ICH = chopper input
ISP = inhibit input
IOSY = output for the horizontal syncronization pulses for the phase concurrance/programming input 3
IOTSY = input-output for setting the pulse-width for the syncronization signal
IP2 = programming input 2
IP1 = programming input 1
IS1 = synchronizing and positioning input
IS2 = synchronizing positioning or controlling input
IV = delay/phase control/burst control input

TABLE 1. - PROGRAM TYPES

PROG. NUM.	PROGRAM PINS IP1	IP2	NAME	CONTROL PINS IV	IIO	ISP	ICH	IS1	IS2	IOSY	IOTSY	OUTPUT SIGNAL O1	O2
P00/1	H	H	Zero phase control	L		H	H	S_y 1)	S_y 1)	—	RC	SSP_1	SSP_2
P00/2	H	H	Phase control by a zero current signal	L	L SPC_1	H SPC_1	H	S_y 1)	S_y 1)	—	RC	SSP_1	SSP_2
P00/3	H	H	Phase control	L SPC_1	L	H DC_1	H DC_2	S_y 1)	S_y 1)	RC 2)	RC	SSP_1	SSP_2
P00/4	H	H	Phase control by a zero voltage or current signal	L SPC_1	L SPC_2	H	H	S_y 1)	S_y 1)	RC 2)	RC	SSP_1	SSP_2
P00/5	H	H	Control of commands	L DC_1	L DC_2	H DC_3	H DC_4	SC_1 SPC_1	$SC_{1/2}$ $SPC_{1/2}$	R 3) O3	L,R 4) RC	CCI	CCII
P010	H	L	Burst control by zero current signal for thyristors	L SPC_1 5)	L SPC_2	H	H	S_y 1)	S_y 1)	IP_3=H	R RC	SSP_1	SSP_2
P011	H	L	Burst control by zero current signal (O1) and zero voltage signal (O2) for triacs	L SPC_1	L SPC_1	H 9)	H	S_y	L SPC_3	IP_3=L	RC	$SSP_{1/2}$ CCI	$SSP_{1/2}$ CCI
P10	L	H	Phase control (O1) and burst control by a zero voltage signal (O2) for triacs	L SPC_1	L	H 9)	H	S_y	L SPC_2	RC 2)	RC	$SSP_{1/2}$ CCI	$SSP_{1/2}$ CCII
P11	L	L	Control of transistors/ control of comands/ static inverter	L DC_1	L DC_2	H DC_3	H DC_4	SC_1 8)	SP_2 8)	R 3) O3	L,R 4) LC	CCI	CCII

TABLE 2. - OUTPUT CURRENT SHAPE

PROGR. NUMBER	CURRENT SHAPE AT O1 AND O2 OUTPUTS	IV	IIO	CONTROL PINS ISP	ICH	IS1
P00/1+5	One pulse	RC	H	RC 10)	H	L
	One pulse (chopped)	RC	H	RC 10)	Chopping signal	L
	Signal (180°)	H	H	RC 10)	H	L
	Ground of pulses (180°)	RC	RC	RC 10)	H	L
		H	H	RC 10)	Chopping signal	L
P010	See P00/1÷5					
P011	See P00/1³5 : CCI				Operate on CCI and CCII simultanmeously	
	One pulse: CCII	—	—	RC		
P10	See P011					
P11	See P00/1³5 (Without IV)					Modulating signal for the currents at outputs

NOTES:

1) The channel switching is made at the concurrence of the synchronization signals from IS_1 and IS (SSP$_1$: H,H).
2) The RC network generates a voltage slope in order to obtain a delay.
3) IOSY becomes the 03 output.
4) The L logic level should be applied by the R resistor. After the channel switching, IOTSY stays in the H state.
5) SPC_1 will maintain during the synchronization pulse set at IOTSY and should stay at IV for a time t_p after this pulse is over.
6) The synchronization pulse width at IOTSY should be small as compared to the pulse width al IS_1, SPC_1 and SPC_2 operate at 01 and SPC_3 at 02.
7) SPC_1 operates at 01 and SPC_2 at 02.
8) The channel selection is made by a H level at $SP_1 \neq SP_2$ (for CC1, SP_1 = L, SP_2 = H) IS_1 and IS_2 are internally connected at V_{DD} through a resistor and thus they could be controlled by open-drain outputs.
9) In case that ISP is in a L state, only the 01 output is inhibited.
10) The RC network determines the synchronization pulse width.
11) The abbreviations in tables 1 and 2 have following significances:

RC — RC network with C at H and R at L
R — resistor connected at L
SC — control signal
Sy — synchronization signal
SP — positioning signal
SPC_x — main control signal
DC_n — signal with influence upon the command time
SSP_1 — signal controlled by synchronization or positioning of 1 type (IS_1=IS_2=H)
SSP_2 — signal controlled by synchronization or positioning of 2 type (IS_1=IS_2=L)
$SSP_{1/2}$ — signal controlled by synchronization or positioning of alternative type (IS_1.H → L or IS_1:L → H)

CCI — control channel I
CCII — control channel II
H, L — logic levels
k, n — indexes

STATIC ELECTRICAL CHARACTERISTICS T_A=25°C

	PARAMETER	TEST CONDITIONS						VALUES		UNIT	NOTES
		V_{DD} (V)	V_{IH} (V)	V_{IL} (V)	V_I (V)	V_O (V)	I_O (mA)	Min.	Max.		
I_I	— Input leakage current at IOTI, IOTP pins	−28	—	—	−25	—	—	−10	—	μA	
I_I	Input leakage current at IP1,IS1,IS2,IIO,IV,ICH,IPS pins	-	-	-	−25	-	-	−10	-	μA	
V_{OH}	Output voltage at IOSY pin	−25	−2	−9	-	—	−2	−.4	—	V	
V_{OH}	Output voltage at IOTSY pin	−25	−2	−9	-	-	−1	−.4	-	V	
V_{OH}	Output voltage at 01,02 pins	−25	−2	−9	-	-	−5	−1	-	V	
V_{OH}	Output voltage at IOTI,IOTP pins	−25	−2	−9	-	-	−1	−2	-	V	
I_{OL}	Quiscent output current at IOSY,IOTSY,01,02 pins	−28	−2	−9	-	−28	-	−10	-	μA	
I_{DD}	Static suoply current	−28	−2	−9	—	—	—	−6	—	μA	1)
C_I	Input capacitance	—	—	—	—	—	—	—	10	pF	
C_O	Output capacitance	—	—	—	—	—	—	—	40	pF	2)
V_{OH}	Output high voltage	−25 −28	−2 −2	−9 −9	— —	−25 −28	— —	−2	—	V	
V_{OL}	Output low voltage	−25 −28	−2 −2	−9 −9	— —	−25 −28	— —	—	—	V	

NOTES: 1) All inputs at VIH: IOSY, IOTSY, IOTP, IOTI, 01, 02 not connected.
2) At 01 and 02 outputs is allowed: C_O < 40 pF

BLOCK DIAGRAM

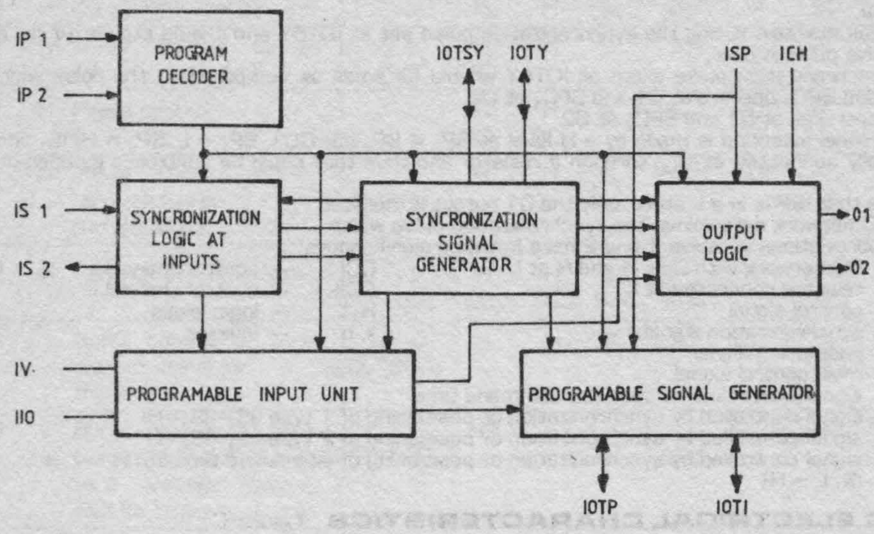


Fig.2 Block diagram

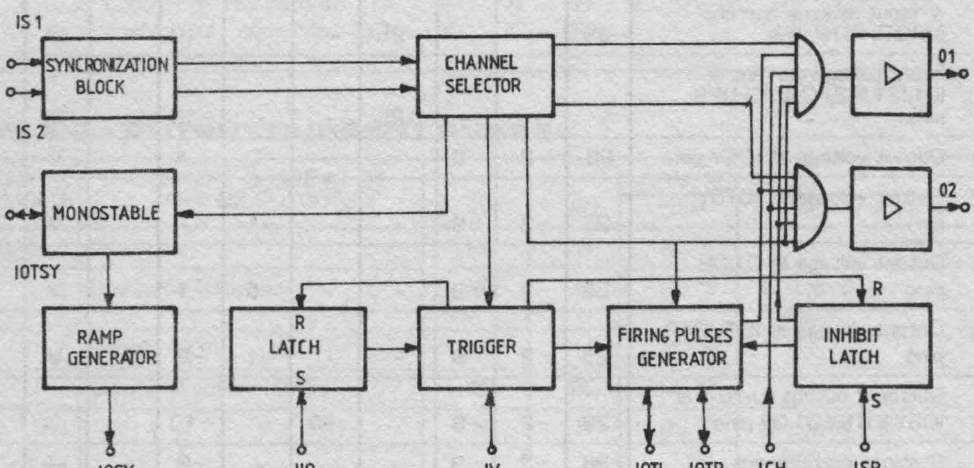


Fig.3a. Block diagram in P00 programs

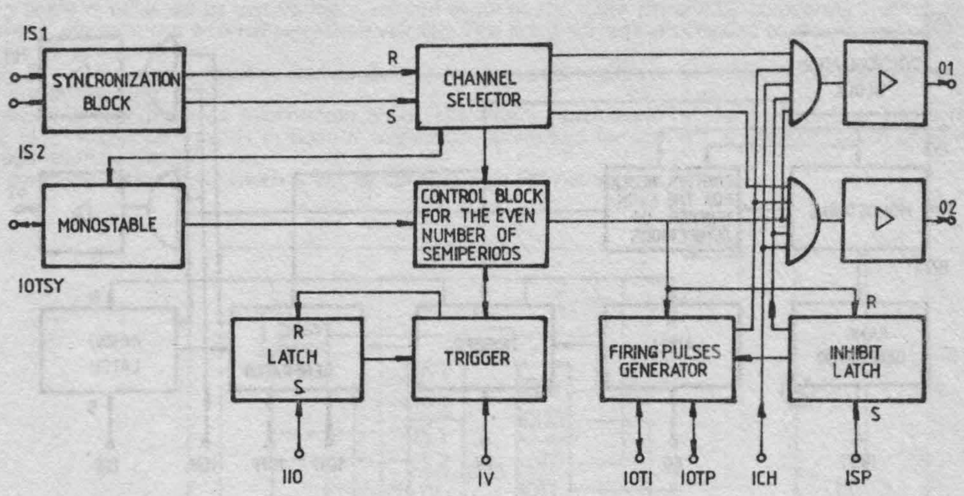


Fig.3b Block diagram in P010 program

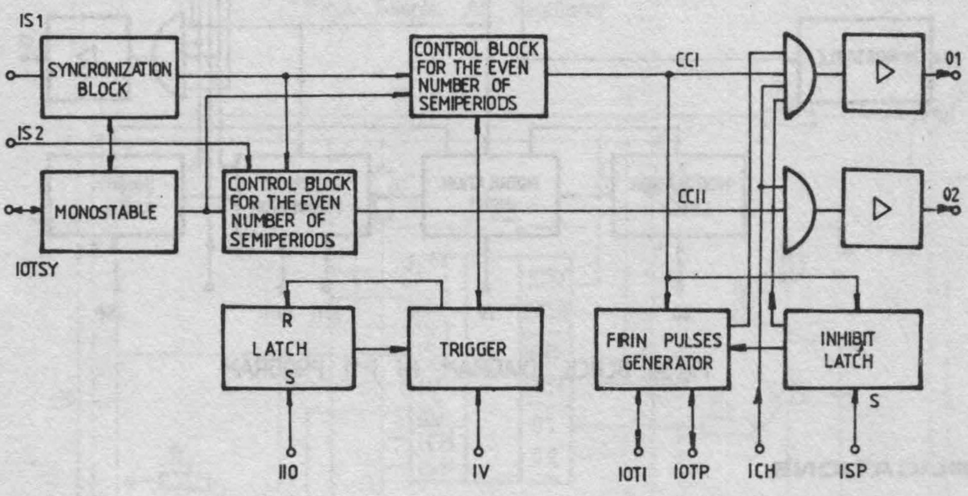


Fig.3c Block diagram in P011 program

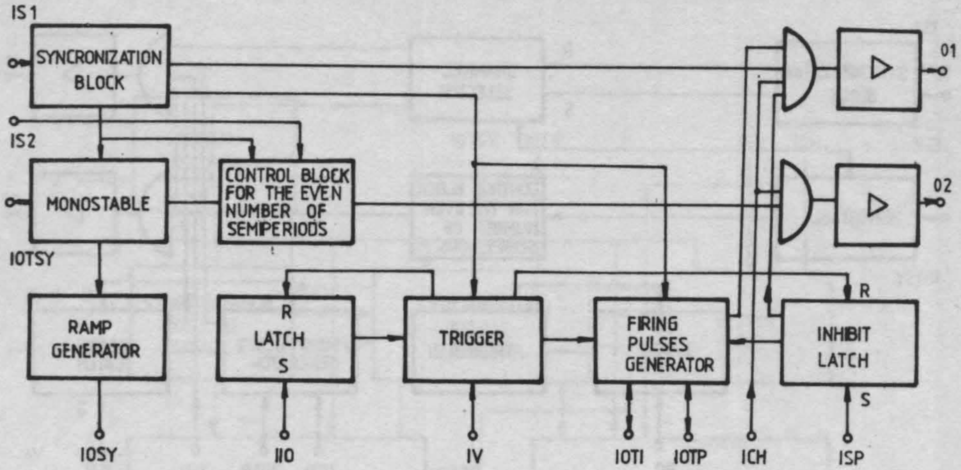


Fig. 3d. BLOCK DIAGRAM IN P10 PROGRAM

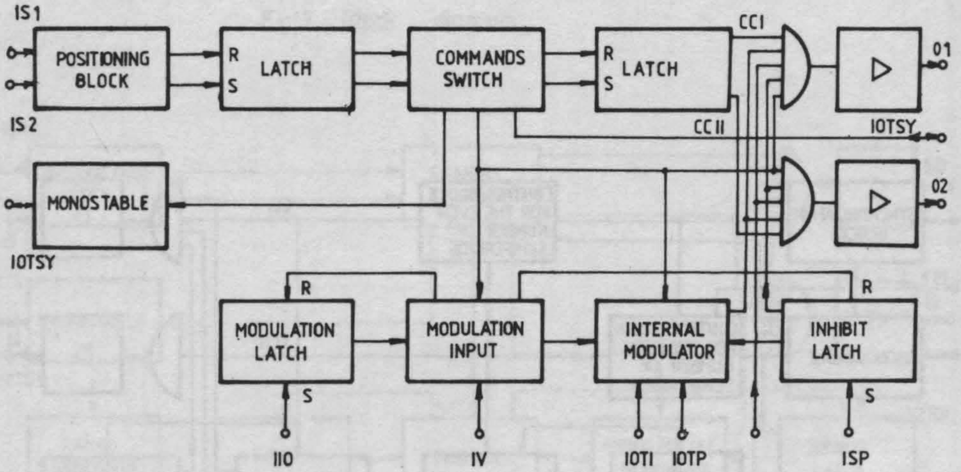


Fig.3e. BLOCK DIAGRAM IN P11 PROGRAM

APPLICATIONS

MMP 708 can be used in the power electronic circuits control. Some possible applications are:
- monophased rectifiers with switching off by network
- triphased rectifiers with switching off by network
- electronic protection
- AC regulators
- adjustable-speed DC motor drivers
- static inverters
- simultaneous driving of two independent loads

In fig. 4—8 are presented some simple diagrams using the MMP 708 integrated circuit. The recommended values for the supply voltages and some possible values of passive components are shown in table 3.

In fig. 4 is presented a AC regulator. The RC network from the IOTI pin sets the firing pulse width. The firing angle is obtained by generating a voltage slope at the IOSY pin and by comparing the voltage level at the I_v pin with the internal reference voltage. The firing current is provided by a limiting resistor. The output O2 is not used.
In fig. 5 is presented a small power speed regulator. In this regulator an inhibit pulse appears at the power supply applying.
A tahogenerator provides information about the motor revolutions by the voltage $U_{(n)}$. The error voltage $U_{ref} - U_{(n)}$ commands in base a transistor connected for current generator, which provides the voltage slope at the IOSY pin.
The synchronization pulse width is set by connecting a RC network at IOSY.

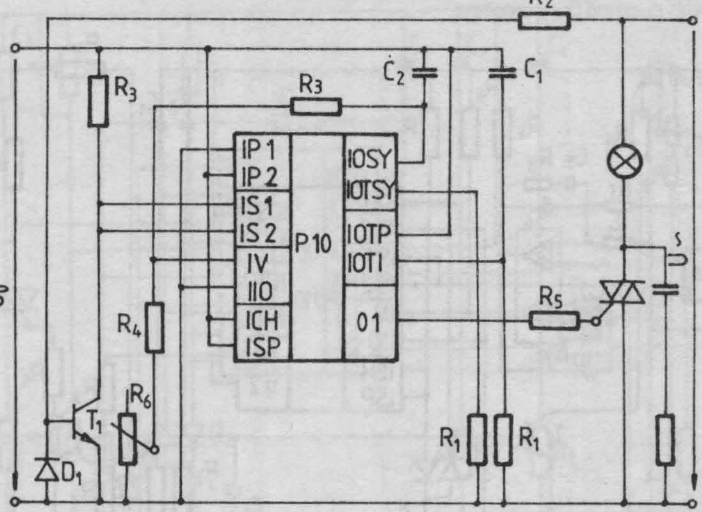


Fig.4 Simple AC regulator

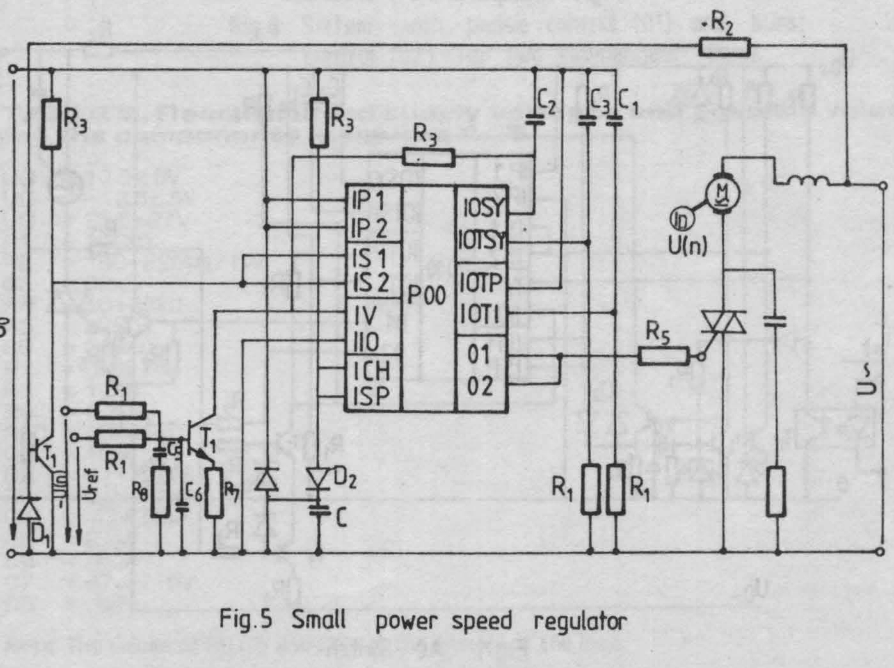


Fig.5 Small power speed regulator

In fig. 6 is presented a temperature stabilizer. Since temperature control requires long time constants complete mains periods are used.
MMP 708 takes over the following functions: generating of the inhibit pulse at power on, synchronization and generating of firing pulses when the control voltage at the IV pin has a proper level. The circuit β 555 delivers at the pin 7 a voltage slope synchronized with the mains with a duration,

$$t = nT \text{ mains}$$

adjustable by a RC network
The circuit βM 393 contains two comparators. In the first one the reaction voltage obtained by means of a thermistor is compared with a reference voltage, thus an error voltage is obtained at the output. This error voltage is compared in the second comparator with a voltage slope generated by the circuit βM 393. The comparison result drives the circuit MMP 708 at the pin IV.
In fig. 7 is presented a AC switch for comanding the low power asynchronous motors or other loads that require a high current consumption.

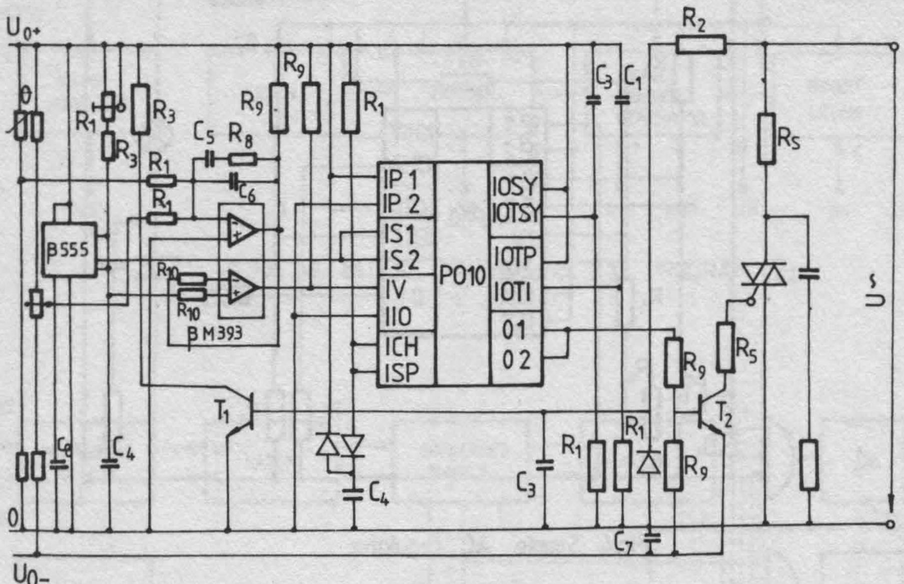


Fig.6 Temperature stabilizer

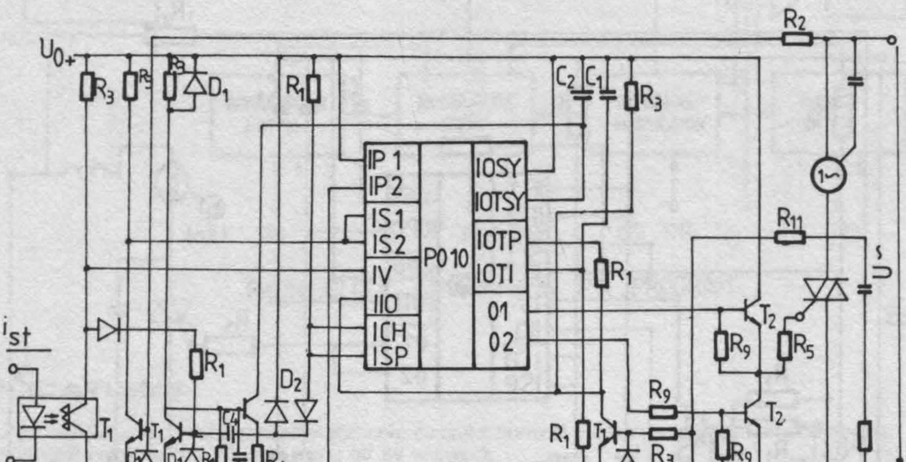


Fig.7 AC Switch

The advantages of this circuit are the following:
- noise immunity
- no overshoots and DC components on the mains, although at start the triac is commanded in phase
- extension of the starting pulse until the certain firing of the traic
- occurance of an inhibit pulse at power on

In fig. 8 is presented a control system for two independent loads. The synchronization is performed on the edges of the signal applied to the IS_1 pin. At the 01 output is obtained phase controlled signal. Therefore this output could be used for controlling a motor by means of a triac. At the 02 output is delivered a command signal active an even number of mains semiperiods, when the command voltage at the IV pin has the proper level. Thus both the power dissipated by the resistor and the fan rotation speed in a heating system could be controlled.

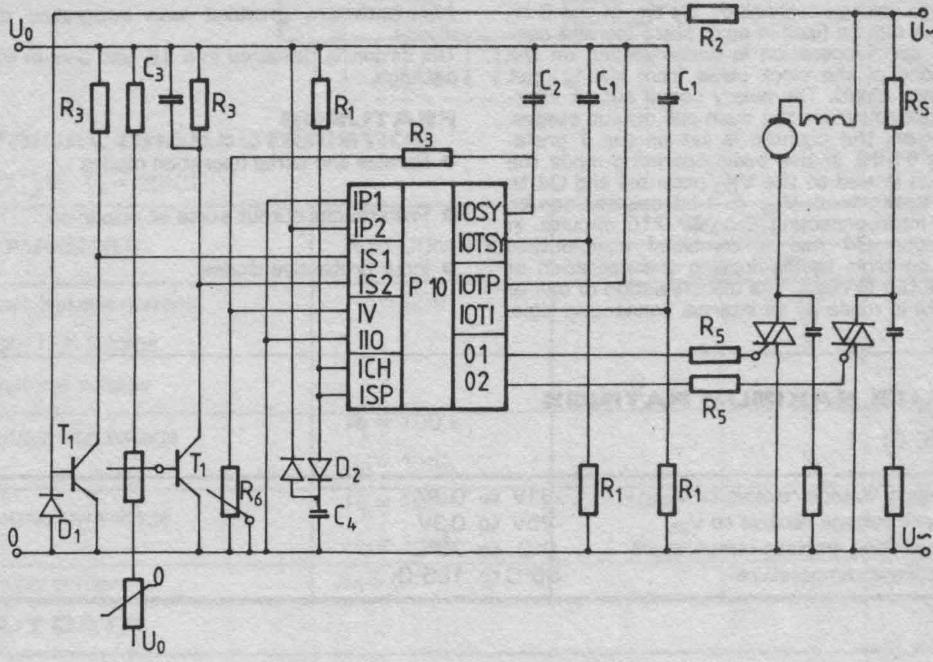


Fig.8 Sistem with phase control (01) and burst control (02) for two independent loads

TABLE 3. Recommended supply voltages and possible values for the components in figures 4...8.

UO+ = 13.5±.5V
UO− = −13.5±.5V
UO = 25.5+27V
R1 = 100kΩ
R2 = 180+220kΩ/1W
R3 = 33kΩ
R4 = 10+33kΩ
R5 = 270Ω
R6 = 2.5MΩ
R7 = .1+4.7kΩ
R8 = 1...kΩ
R9 = 4.7kΩ
R10 = 10+20kΩ
C1 = 10nF
C2 = 47+100nF
C3 = 2.2+4.7nF
C4 = .47+3.3µF
C5 = 2...µF
C6 = .1...µF
C7 = 47µF/16V
C8 = .1µF

Note: The values of R8,C5 and C6 set the answer of the loop.

8 CHANNEL TOUCH CONTROL CIRCUIT FOR TV PROGRAM SELECTION

GENERAL DESCRIPTION

The MMP 710 circuit is used as input circuit together with the MMP 711 decoder circuit for electronic touch plate switching of 8 or 16 channels for TV program selection.
The MMP 710 circuit contains a 3 bit counter in p-channel high voltage technology. By any of the 8 inputs I_1 to I_8 it can be fixed in each state (parallel operation). The serial operation is accomplished on the H-L transitions of the clock pulse from the I_S input (clock impulses input). The binary coded output information is obtained from the push-pull output stages. When power-on, the counter is set on the 1 preferential state (HHH). In this basic operating mode the I_{CL} connection is tied to the V_{DD} potential and O4 to that of the background, V_{SS}. A 4 bit counter can be obtained by interconnecting 2 MMP 710 circuits. In this connection O4 has a combined input-output function. It controls by flip-flopping the operation of the 2 connected circuits. The disconnection of one of the 2 circuits is made by an internal connecting logic.
In this situation the I_{CL} connection of the first circuit is tied to the V_{DD} potential while that of the second circuit is tied to the background. The O1 ... O4 outputs and the I_S inputs of the 2 circuits are connected together.
All inputs are provided with integrated protective diodes.
The circuit is delivered in a 16 lead dual-in line plastic package..

FEATURES

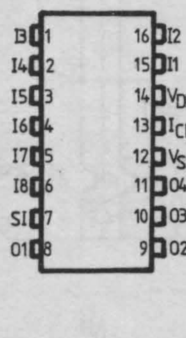
- Parallel and serial operation modes
- Preferencial output state at power-on
- Input protective diodes

ABSOLUTE MAXIMUM RATINGS

(T_A = 0 to 70°C)

V_{DD}	Supply voltage relative to V_{SS}	-31V to 0.3V
V_I	Input voltage relative to V_{SS}	-25V to 0.3V
T	Operating ambient temperature	0°C to 70°C
T	Storage temperature	-55°C to 125°C

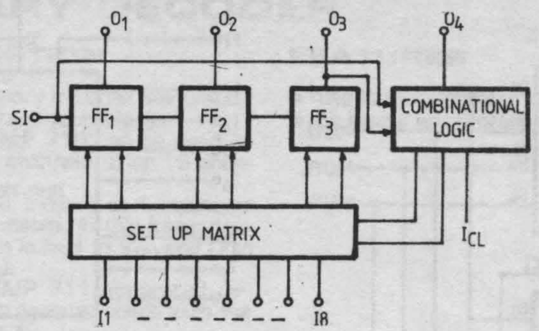
PIN CONNECTIONS



PIN NAMES

I1 I8	PARALLEL INPUTS
SI	SERIAL INPUT
O1 O4	OUTPUTS
ICL	INTERNAL CONNECTING LOGIC CONTROL
V_{DD}	POWER SUPPLY $(-27^{-1}_{+2}$ V)
V_{SS}	GROUND

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

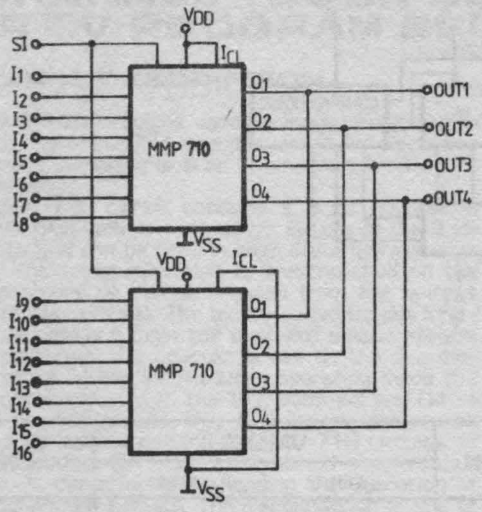
$(-V_{DD} = 27^{+1}_{-2}\,V,\ T_A = 25°C)$

PARAMETER	TEST CONDITION	VALUES min	VALUES max	UNIT
$-I_I$ Input leakage current	$-V_I = 25V$		10	"A
$-V_{IH}$ Input high voltage			2	V
$-V_{IL}$ Input low voltage		9		V
$-V_{OH}$ Output high voltage	$R_L = 100\,k$		1	V
V_{OH}	$-I_O = 1\,mA$		3	V
$-V_{OL}$ Output low voltage	$R_L = 100\,k$	10		V
V_{OL}	$-I_O = 1\,mA$	9		V
$-I_1$ Supply current	$I_O = 0$		2.3	mA

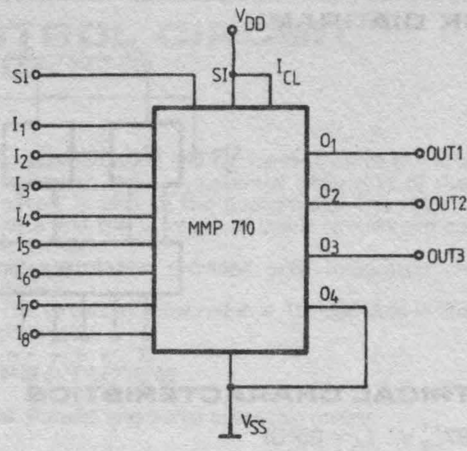
OUTPUT DATA

STATE	OUTPUT DATA O_1	O_2	O_3	O_4
1	H	H	H	H
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

TYPICAL APPLICATIONS

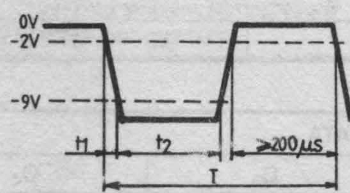


4 BITS COUNTER



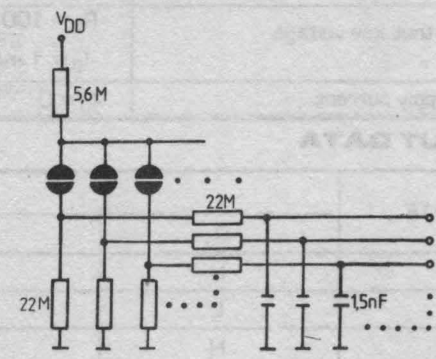
3 BITS COUNTER

CLOCK PULSE CHARACTERISTICS



$t_1 \leqslant 50 \mu s$
$t_2 = 60 \dots 200 \mu s$
pause width $\geqslant 200 \mu s$

INPUT CONNECTING TO TOUCH PLATES



1 OF 8 BINARY DECODER

GENERAL DESCRIPTION

The MMP 711 is a 1 of 8 binary decoder manufactured in PMOS-Al gate high voltage technology.
MMP 711 together with MMP 710 can be used as output circuit for TV switch channels (8 or 16 channels).
The binary input information from the 4 inputs is transferred to the decoding matrix. In this basic operation mode the I_{CL} connexion is tied to V_{DD} and I_4 to the background potential (V_{SS}).
Assembling together two MMP 711 integrated circuits to form a 1 of 16 binary decoder needs with the proper connection of the input I_{CL}.
In this case the input I_{CL} of the first circuit (1...8) is tied to V_{DD} and the input I_{CL} of the second circuit (9...16) to the background potential (V_{SS}).
The inputs I_1...I_4 of both circuits are tied together.
The MMP 711 is supplied in a 16 lead dual in line plastic package.

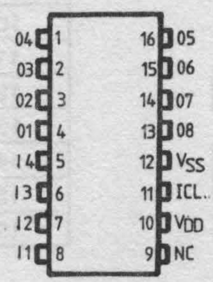
FEATURES

- The outputs consist of open drain transistors.
- All inputs are protected against static charge.

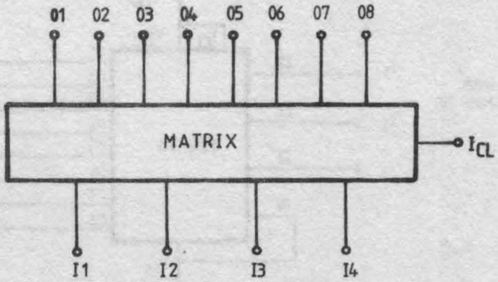
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply Voltage	-31 ... +0.3	V
V_I	Input Voltage	-25 ... +0.3	V
I_O	DC Output Current	- 3	mA
T_A	Operating Ambient Temperature	0 ... +70	°C
T_{stg}	Storage Temperature	-55 ... +125	°C

PIN CONNECTIONS



BLOCK DIAGRAM



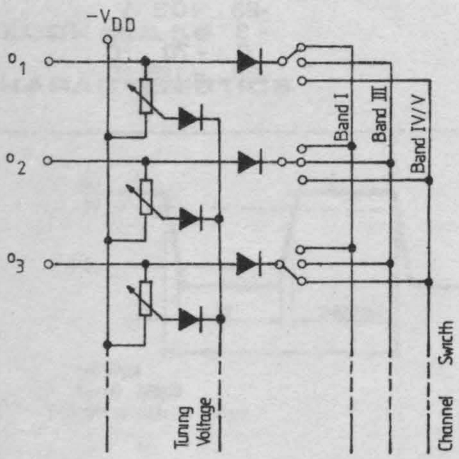
ELECTRICAL CHARACTERISTICS

($-V_{DD} = 27^{+1}_{-2}$ V, $T_A = 25°C$) unless otherwise specified

	PARAMETER	TEST CONDITION	VALUES min	VALUES max	UNIT
$-V_{IH}$	Input High Voltage			2	V
$-V_{IL}$	Input Low Voltage		9		V
$-V_{OH}$	Output High Voltage	$R_L = 100$ K		0.5	V
$-V_{OH}$		$-I_0 = 3$ mA		2	V
$-I_{DD}$	V_{DD} Supply Current	$I_0 = 0$		0.6	mA
$\frac{\Delta(V_{DD}-V_{OH})}{\Delta T_A}$	Output High Voltage Differential Drift	$T_A = 10...50°C$, $R_L = 100$ K		1	$\frac{mV}{°C}$

OUTPUT CONNECTING

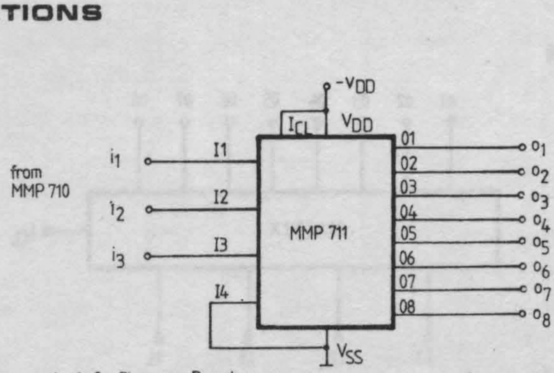
Used together with the MMP 710 for electronic touch plate switching of programs for television receivers.



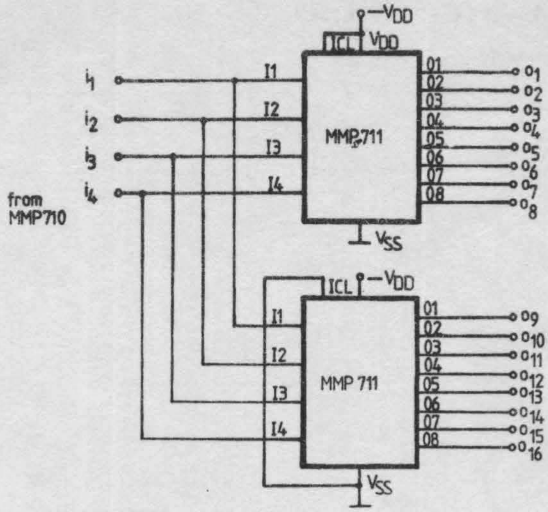
DECODER INPUT DATA

STATE	OUTPUT DATA I_1	I_2	I_3	I_4
1	H	H	H	H
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

TYPICAL APPLICATIONS



1 of 8 Binary Decoder



1 of 16 Binary Decoder

Tiparul executat la Combinatul poligrafic
„Casa Scînteii" sub comanda nr. 80511